Telecom Design Solutions

TELTONE

TELTONE®

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Teltone Limited / 3375-14th Avenue, Markham, Ontario, Canada L3R 2L6   Phone: 416-475-0837   Fax: 416-474-9151   Envoy User Name: TTL.HQ

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8. TELECOM SOLUTIONS

9. APPLICATION NOTES

Section 1

Customer Information

TELTONE CORPORATION

Teltone, a Seattle-area company, has been developing innovative products to meet the needs of the telecommunications industry since it was founded in 1968. Our Telecom Components division offers a wide spectrum of telecommunications components, including state-of-the-art tone receivers, detectors, and other signaling products.

An early product area, DTMF-to-rotary dial conversion equipment, brought us leadership status in subscriber dialing and has resulted in the development of a complete family of tone receivers for use by manufacturers of PBXs, security and control devices, and many other types of equipment. Our experience with signaling technology in our own conversion, remote access, and service evaluation products has made Teltone components performance leaders in the domestic and international markets.

Over the years, Teltone has gained a reputation for commitment to quality, reliability, and customer service. The accumulation of more than 20 years' experience working with telephone companies, interconnects, government agencies, and large and small businesses, has taught us the importance of being responsive to the demands and problems of a variety of customers.

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TERMS AND CONDITIONS

PRICE
All prices contained herein are list prices, F.O.B. Teltone Corporation, Kirkland, Washington.

Prices are subject to change without notice and are exclusive of applicable taxes, duty, export or special packing, insurance, etc. Invoiced prices will be those in effect at time of shipment.

MINIMUM BILLING
Any order amounting to less than One Hundred Dollars ($100.00) net, shall be billed at One Hundred Dollars ($100.00).

TERMS
Net 30 days.

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Seller warrants that the Software will perform substantially in accordance with the accompanying written manuals and specifications for a period of twelve (12) months from the date of delivery. Seller will correct any errors present in the software at the time of delivery that significantly affect performance in accordance with the specifications in written manuals. This warranty is contingent upon the Buyer promptly notifying the Seller of such errors. Such notification must be in writing and must be received by the Seller within the 12 months period following delivery. Any changes made to the Software shall be warranted as provided herein for the remainder of the original warranty period or for ninety (90) days, whichever is longer, calculated from the date the changes are received by Buyer.

EQUIPMENT
Seller warrants that all equipment sold pursuant to the agreement is free from defects in material or workmanship at the time of delivery. If Seller receives written notice of any such defects within 12 months of delivery, and if the defect is not the result of improper usage, service, maintenance, or installation by someone other than the Seller or its authorized representative, and the equipment has not been damaged or abused after delivery, or altered or modified by anyone other than an authorized employee or representative of Seller, Seller shall replace or repair (at its sole option) the defective part or parts of equipment in accordance with the following:

1.Any such defective Material shall be returned prepaid by Buyer to Sellers plant (or to any other repair facility designated by Seller), and if Seller, in its sole discretion, determines on examination that the part or parts returned contain a defect in Material or workmanship covered by this warranty, Seller shall repair or replace Material at its expense, and return ship such Material, freight prepaid. If Seller determines on examination that there is a defect in the Material returned, but that the defect

is not covered by this warranty, Seller shall notify the Buyer of the cost incurred to diagnose the defect and of the estimated cost of correcting the defect and, if requested to do so by Buyer, will correct such defect, return ship such Material, freight prepaid, and bill Buyer for cost of repair and freight.

2.Seller will, on request, furnish qualified service personnel to repair or replace under warranty any Material at any location(s) designated by Buyer. Buyer shall pay Seller for all expenses of such personnel including transportation, room, board and other travel expenses.

Any replacement or repair performed by Seller shall be warranted, as provided herein, for the remainder of the original warranty period or for ninety (90) days, whichever is longer, calculated from the date the repair is completed or the date the repair or replacement Material is delivered, as applicable. Any repair or replacement completed on-site by Seller shall be warranted, as provided herein, for the remainder of the original warranty, or ninety (90) days, whichever is longer.

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SELLER SHALL NOT BE LIABLE FOR ANY INCIDENTIAL OR CONSEQUENTIAL DAMAGES INCURRED AS A RESULT OF ANY DEFECT IN ANY SOFTWARE LICENSED OR EQUIPMENT SOLD HEREUNDER. SELLERS ENTIRE LIABILITY AND BUYERS EXCLUSIVE REMEDY FOR SOFTWARE AND EQUIPMENT COVERED BY THIS WARRANTY SHALL BE, AT THE SELLERS OPTION, REPAIR, REPLACEMENT OR A REFUND OF THE PRICE PAID BY THE BUYER.

THE WARRANTIES SET FORTH HEREIN ARE THE ONLY WARRANTIES, ORAL OR WRITTEN, MADE BY SELLER AND ARE IN LIEU OF AND REPLACE ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING THE WARRANTY OF MERCHANTABILITY AND THE WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE.

RETURNS
Equipment returned in new and unused condition in the original containers within 60 days will be subject to a restocking charge of 20%. Contact Teltone Repair Order Entry for a Material Return Authorization (MRA) number. Unauthorized returns will be subject to a $50.00 surcharge and may be delayed due to the extra processing required.

INSPECTION
Seller may inspect any of the equipment furnished hereunder at any time during the warranty period. For specific product warranty periods refer to product price sheets.

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Teltone's experienced Product Support engineers are available for assistance in meeting your application needs.

Teltone cannot assume responsibility for use of any circuitry herein described other than circuitry entirely embodied in a Teltone proprietary product. No other circuit patent licenses are implied. Teltone reserves the right to change, without notice, any circuitry or specifications.

Prices and technical data are subject to change without notice.

CAUTION

MOS DEVICE. MAY BE
DAMAGED BY STATIC DISCHARGE.
OBSERVE HANDLING PRECAUTIONS.

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Selection Guides

DTMF RECEIVERS AND TRANSMITTERS

	M-957-01 (page 3-1)	M-957-02 (page 3-9)	M-8870 (page 3-17)	M-8880 (page 3-25)	M-8888 (page 3-37)
PACKAGE					
Monolithic IC	•	•	•	•	•
Pin count	22	22	18	20	20
CERDIP	•	•	•	•	•
Plastic	•	•	•	•	•
CMOS technology	•	•	•	•	•
OPERATION					
12 V	•				
5 V	•	•	•	•	•
DTMF in	•	•	•	•	•
DTMF out				•	•
Dial tone immune	•	•	•	•	•
Call progress out				•	•
INPUT					
Differential AC			•	•	•
Single-Ended AC	•	•			
Adjustable receiver timing			•	•	•
OUTPUT					
Binary	•	•	•	•	•
Binary code 2-of-8	•	•			
Tone				•	•

CALL PROGRESS TONE RECEIVERS AND TRANSMITTERS

	M-980 (page 4-1)	M-981 (page 4-7)	M-982 (page 4-11)	M-984 (page 4-15)	M-991 (page 4-19)
PACKAGE					
Monolithic IC	•	•	•	•	•
Pin count	8	22	22	14	14
CMOS	•	•	•	•	•
CERDIP	•			•	•
Plastic	•	•	•	•	•
OPERATION					
5 V	•	•	•	•	•
Special Information Tones (S.I.T.)				•	
Discriminators (Hz)	1	4	4	4	
Dynamic range (dB)	40	30	38	30	
Call progress tones	•	•	•	•	•
INPUT					
Single-ended AC	•	•	•	•	
Binary					•
OUTPUT					
Logic	•				
1-of-4				•	
Tone					•
Any of 4		•	•		

MF RECEIVERS AND TRANSMITTERS

	M-986-1R1 (page 5-1)	M-986-2R1 (page 5-1)	M-986-1R2 (page 5-3)	M-986-2R2 (page 5-3)	M-993 (page 5-15)
PACKAGE					
Monolithic IC	•	•	•	•	•
Pin count	40	40	40	40	14
Coprocessor port	•	•	•	•	
Ceramic	•	•	•	•	
CERDIP					•
Plastic	TBA*	TBA	TBA	TBA	•
Flat pack	TBA	TBA	TBA	TBA	
OPERATION					
5 V	•	•	•	•	•
Single channel	•		•		•
Dual channel		•		•	
STANDARDS					
CCITT R1	•	•			•
CCITT R2			•	•	
INPUT					
A-law PCM digital			•	•	
μ-law PCM digital	•	•			
OUTPUT					
Linear (analog)					•
CCITT R1 MF tone					•
A-law PCM digital			•	•	
μ-law PCM digital	•	•			
Tone					•
DATA FORMAT					
Binary	•	•	•	•	
2-of-6	•	•	•	•	

*To be announced.

DC SIGNAL SENSORS

	M-949-01 (page 6-1)	M-949-02 (page 6-3)	M-949-03 (page 6-5)	M-949-06 (page 6-7)	M-949-10 (page 6-9)	M-959 (page 6-11)
PACKAGE						
Line sense relay (1 Form A)	•	•	•	•	•	
Monolithic IC						•
Pin count	6	6	6	6	6	14
Magnetic shielding	•	•	•	•	•	
OPERATION						
Line current	•	•	•	•	•	
5 V						•
Minimum pickup current (mA)	20	15	20	15	17.5	
Line current sense range (mA)	20-125	15-170	20-125	15-170	17.5-125	
Max. closure time (ms)	1	1	1	1	1	
Typical longitudinal balance(dB)	63	70	63	70	63	
Resistance (ohms/coil)	20	20	9	9	20	
Coil-to-contact isolation(VRMS)	1500	3750	1500	2250	1500	
STANDARDS						
U.S. FCC Part 68	•				•	
International (IEC/VDE)		•				
Canadian (DOC/CSA)			•	•		
INPUT						
DC logic	•	•	•	•	•	•
10 pps pulse	•	•	•	•	•	•
20 pps pulse	•	•	•	•	•	•
OUTPUT						
Binary						•
Relay contact	•	•	•	•	•	

DTMF Receivers and Transmitters

M-957-01 DTMF RECEIVER

The Teltone® M-957-01 (see Figure 1) combines switched-capacitor and digital frequency measuring techniques to decode Dual-Tone Multifrequency (DTMF) signals to four-bit binary data. Dial tone rejection and 60-Hz noise rejection filters are built in. Fabricated as a monolithic integrated circuit using low-power CMOS processing, the M-957-01 is packaged in a 22-pin DIP and operates from a wide 5-through-12-volt DC supply. An inexpensive 3.58-MHz television crystal and resistor are the only external components required. High system density may be achieved by using the clock output of one crystal-connected receiver to drive the time bases of additional receivers.

The SIGNAL IN input to the M-957 (see Figure 2) interfaces readily to telephone lines, radio receivers, tape players, and other DTMF signal sources. Inputs A and B control sensitivity to a maximum of -38 dBm at 5 V, while the 12/16 input determines the signals to be detected. The preprocessing stages of the M-957 filter out dial tone and noise, split the signal into its high- and low-frequency components, and hard-limit each component to provide automatic gain control. Four discriminators in each group then detect the individual tones. Postprocessing stages of the M-957 time the tone durations and store binary data for outputting as determined by the HEX input. The STROBE output is activated by the

presence of valid data in the output register and cleared by the detection of a valid end-of-signal pause or by the CLEAR input. An early signal presence indicator, BD, facilitates applications requiring tone blocking. The data outputs operate with simple logic circuits or microprocessors, and are three-state enabled to facilitate bus-oriented architectures.

Features

* Complete DTMF receiver in 22-pin DIP (plastic or CerDIP)
* Decodes all 16 DTMF digits
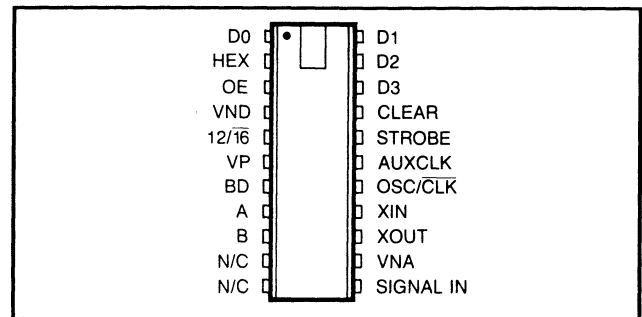* Excellent dial tone and speech immunity
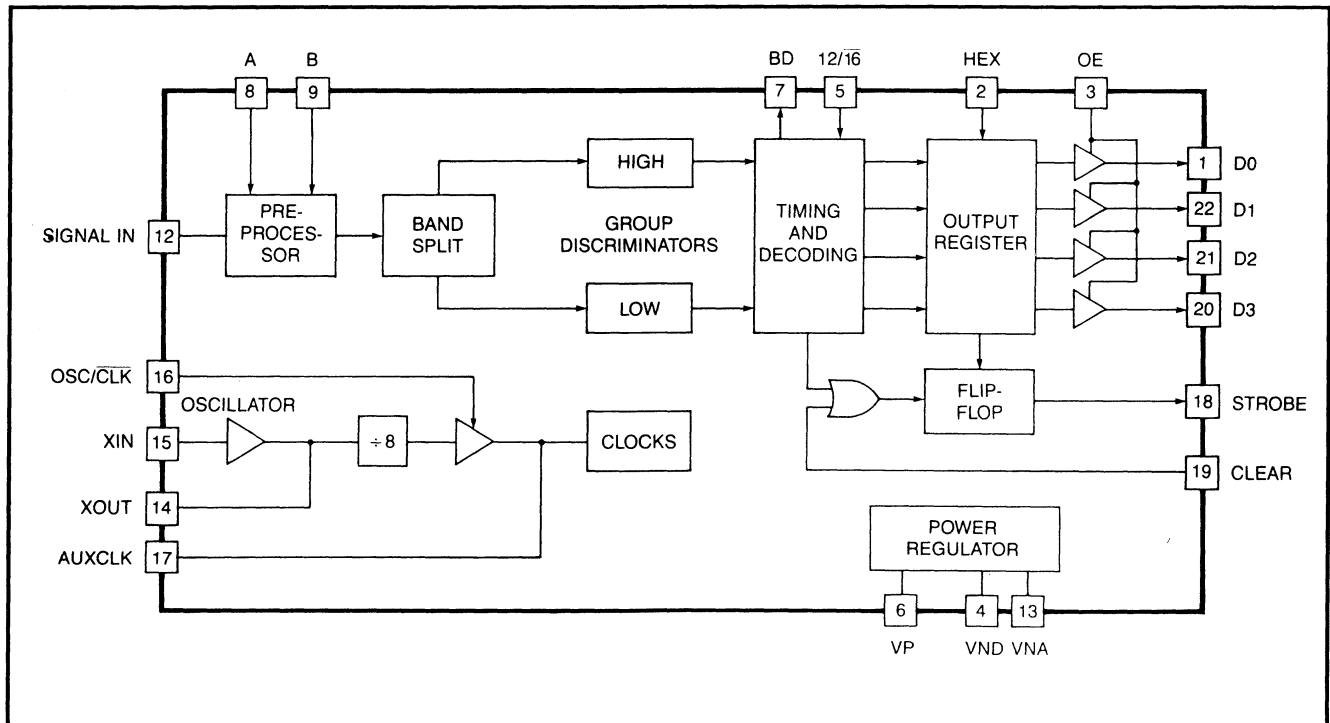

Figure 1 Pin Diagram

Figure 2 Block Diagram

- Meets telephone impulse noise immunity standards
- Digitally selectable sensitivity to -38 dBm
- Selectable 4-bit hexadecimal or binary coded 2 of 8 output
- Fabricated using low-power CMOS technology
- Operates on single DC supply
- Uses inexpensive 3.58-MHz crystal
- Three-state outputs
- 5- through 12-volt supply

Applications
- Central office products
- PBX and key systems
- Radio telephones
- Remote control and monitoring devices
- Computer data entry systems

Table 1 Pin Functions

Pin	Function
SIGNAL IN	DTMF input. Timings are shown in Figure 3. Internally biased so that the input signal may be AC coupled, SIGNAL IN also permits DC coupling as long as the input voltage does not exceed the positive supply. Proper coupling is shown in Figure 5. See Table 2 for the frequency pairs associated with each DTMF signal.
12/$\overline{16}$	DTMF signal detection control. When 12/$\overline{16}$ is at logic "1", the M-957 detects the 12 most commonly used DTMF signals (1 through #). When 12/$\overline{16}$ is at logic "0", the M-957 detects all 16 DTMF signals (1 through D).
A, B	Binary DTMF signal sensitivity control inputs. A and B select the sensitivity of the SIGNAL IN input to a maximum of -31 dBm.
D3, D2, D1, D0	Data outputs. When enabled by the OE input, the data outputs provide the code corresponding to the detected digit in the format programmed by the HEX pin. See Table 2. The data outputs become valid after a tone pair has been detected and are cleared when a valid pause is timed. Timings are shown in Figure 3.
OE	Output enable. When OE is at logic "1", the data outputs are in the CMOS push/pull state and represent the contents of the output register (see Figure 2). When OE is driven to logic "0", the data outputs are forced to the high-impedance or "third" state. Timings are shown in Figure 3.
HEX	Binary output format control. When HEX is at logic "1", the output of the M-957 is full, 4-bit binary. When HEX is at logic "0", the output is binary coded 2-of-8. Table 2 shows the output codes.
STROBE	Valid data indication. STROBE goes to logic "1" after a valid tone pair is sensed and decoded at the data outputs. STROBE remains at logic "1" until a valid pause occurs or the CLEAR input is driven to logic "1", whichever is earlier. Timings are shown in Figure 3.
CLEAR	STROBE control. Driving CLEAR to logic "1" forces the STROBE output to logic "0". When CLEAR is at logic "0", STROBE is forced to logic "0" only when a valid pause is detected. Tie to VNA or VND when not used.
BD	Early signal presence output. BD indicates that a possible signal has been detected and is being validated. As shown in Figure 3, BD precedes STROBE and the data outputs.
XIN, XOUT	Crystal connections. When an auxiliary clock is used, XIN should be tied to logic "1". See Figure 6.
OSC/$\overline{CLK}$	Time base control. When OSC/$\overline{CLK}$ is at logic "1", the output of the M-957's internal oscillator is selected as the time base. When OSC/$\overline{CLK}$ is at logic "0" and XIN is at logic "1", the AUXCLK input is selected as the time base.
AUXCLK	Auxiliary clock input. When OSC/$\overline{CLK}$ is at logic "0" and XIN is at logic "1", the AUXCLK input is selected as the M-957's time base. The auxiliary input must be 3.58 MHz divided by 8 for the M-957 to operate to specifications. If unused, AUXCLK should be left open.
VNA, VND	Negative analog and digital power supply connections. Separated on the chip for greater system flexibility, VNA and VND should be at equal potential.
VP	Positive power supply connection.
N/C	Not connected. These pins have no internal connection and may be left floating.

Table 2 DTMF to Binary Decoding

SIGNAL	LOW-FREQUENCY COMPONENT (Hz)	HIGH-FREQUENCY COMPONENT (Hz)	HEX OUTPUT FORMAT	2-OF-8 OUTPUT FORMAT
			3 2 1 0	3 2 1 0
1	697	1209	0 0 0 1	0 0 0 0
2	697	1336	0 0 1 0	0 0 0 1
3	697	1477	0 0 1 1	0 0 1 0
4	770	1209	0 1 0 0	0 1 0 0
5	770	1336	0 1 0 1	0 1 0 1
6	770	1477	0 1 1 0	0 1 1 0
7	852	1209	0 1 1 1	1 0 0 0
8	852	1336	1 0 0 0	1 0 0 1
9	852	1477	1 0 0 1	1 0 1 0
0	941	1336	1 0 1 0	1 1 0 1
*	941	1209	1 0 1 1	1 1 0 0
#	941	1477	1 1 0 0	1 1 1 0
A	697	1633	1 1 0 1	0 0 1 1
B	770	1633	1 1 1 0	0 1 1 1
C	852	1633	1 1 1 1	1 0 1 1
D	941	1633	0 0 0 0	1 1 1 1

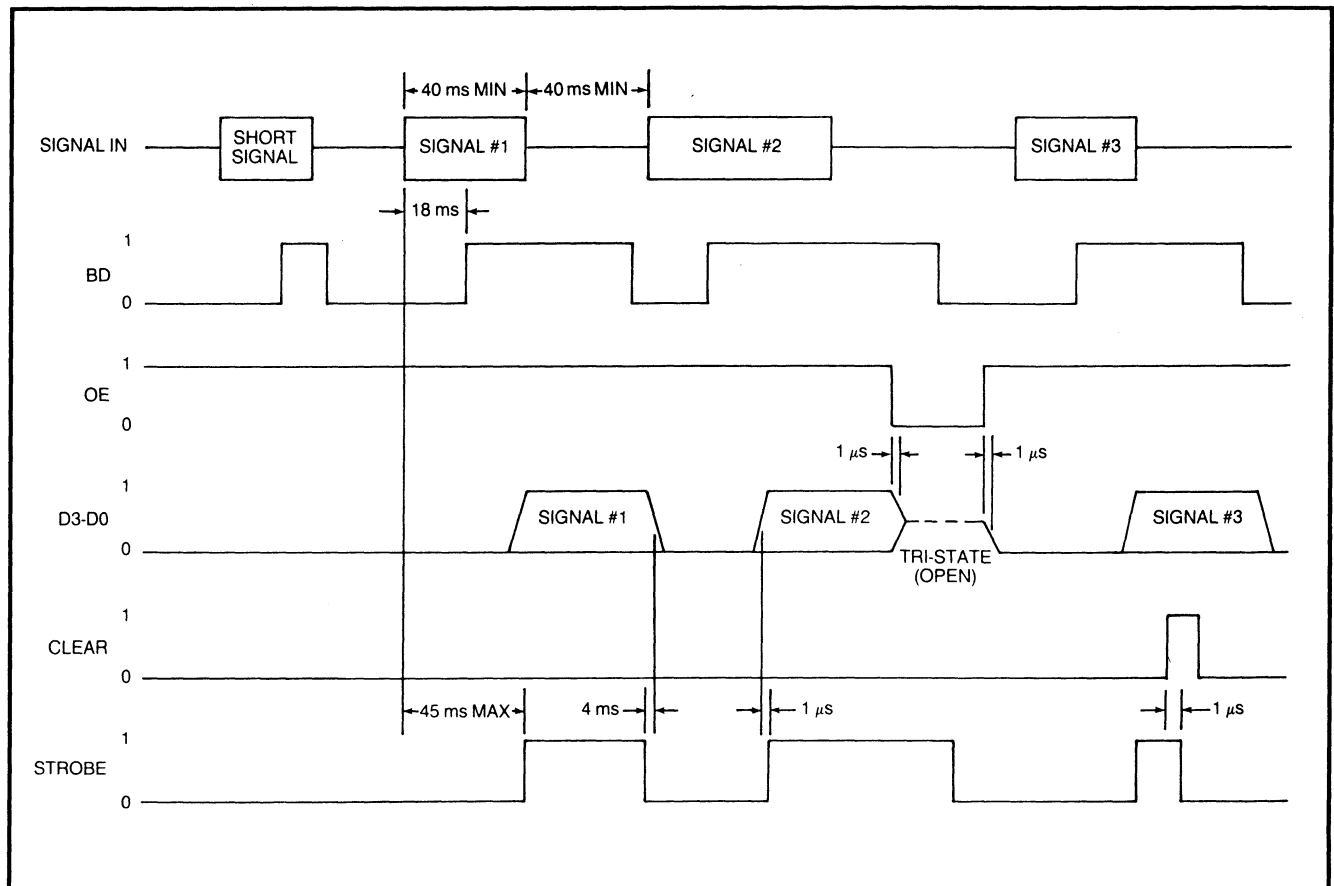Note: The M-957 detects signals A through D only when the 12/16 input is at logic "0".
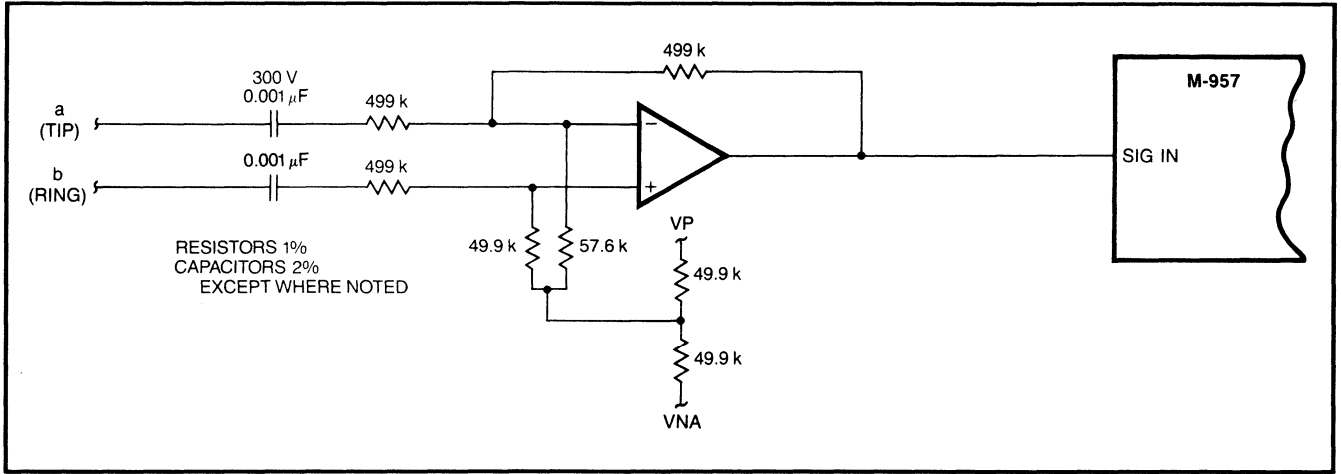

Figure 3 Timing Diagram

Figure 4 Telephone Line Differential Input Interface

NOTE: COUPLING CAPACITOR TO BE USED WHEN VIN IS GREATER THAN VP.

Figure 5 Input Signal Configuration

Table 3 Absolute Maximum Ratings (Note 1)

DC Supply Voltage (Note 2). . . . . VNA 16.0 V
Voltage on SIGNAL IN. . . . . (VP + 0.5 V) to (VNA − 22 V)
Voltage on Any Pin Except SIGNAL IN. . . . . (VP + 0.5 V) to (VND − 0.5 V)
Storage Temperature Range. . . . . −40° to 85° C
Operating Temperature Range. . . . . −40° to 70° C
Lead Soldering Temperature. . . . . 260° C for 5 seconds
Power Dissipation. 1W

Notes:

1. Exceeding these ratings may permanently damage the M-957.
2. VP referenced to VND. VND should be at equal potential to VNA. VND/VNA may be at ground.

Figure 6 Multiple Receiver/Microprocessor Interface

Figure 7 Test Circuit

Table 4 Specifications

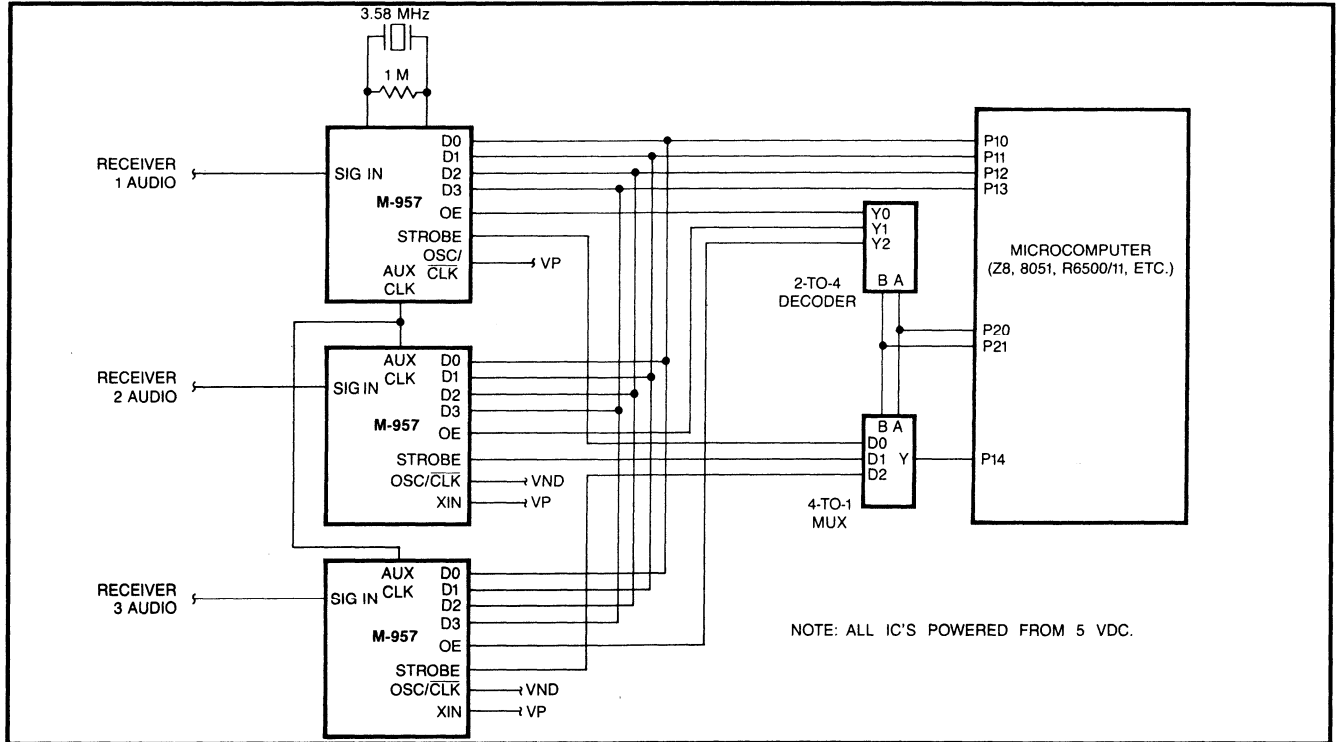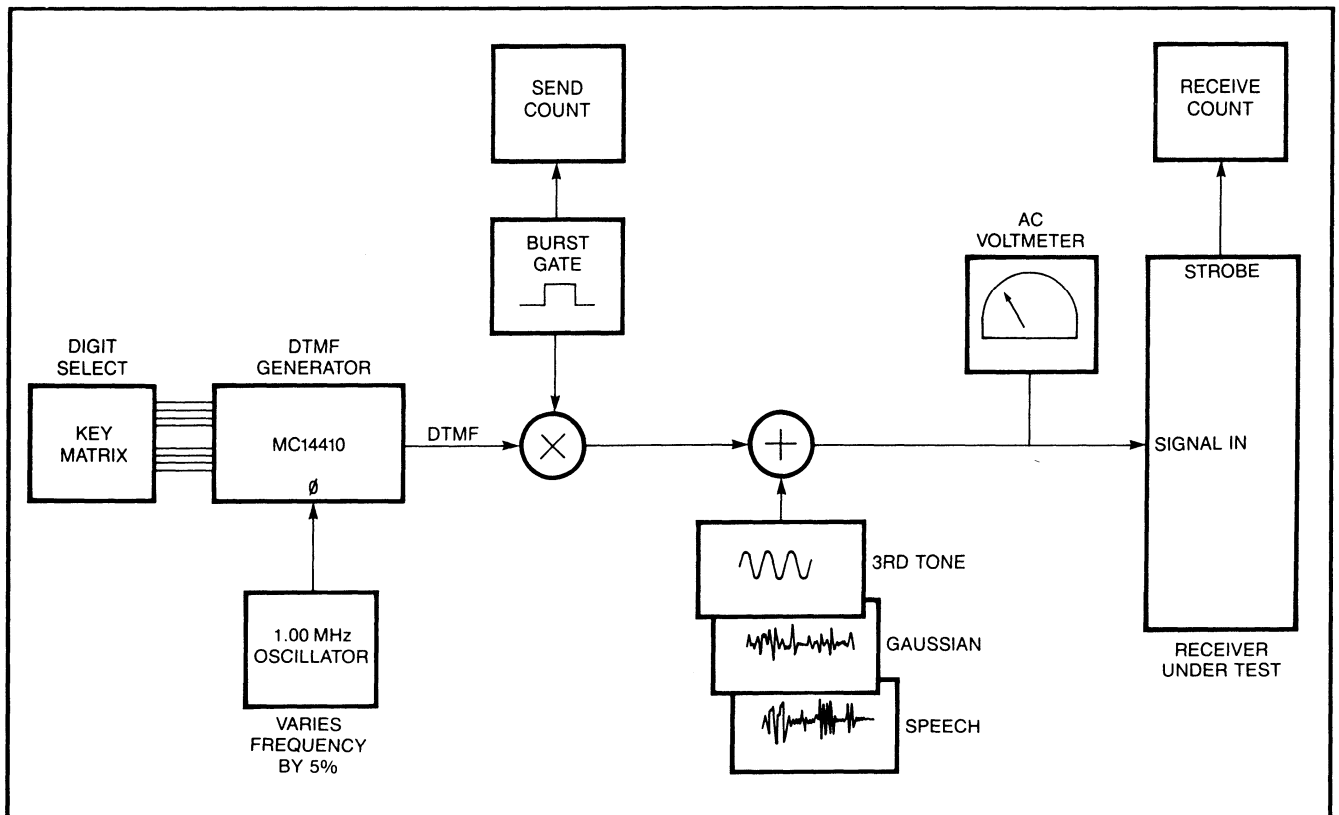| Parameter		Conditions	Min	Typ	Max	Units	Notes
SIGNAL IN Input Requirements	Signal Level (per tone)	VP = 12V					
		A = 0, B = 0	−24	—	+6	dBm	1
		A = 1, B = 0	−27	—	+3	dBm	1
		A = 0, B = 1	−30	—	0	dBm	1
		A = 1, B = 1	—	−32	—	dBm	1
		VP = 5V					
		A = 0, B = 0	−32	—	−2	dBm	1
		A = 1, B = 0	−35	—	−5	dBm	1
		A = 0, B = 1	−38	—	−8	dBm	1
		A = 1, B = 1	—	−40	—	dBm	1
	Signal Duration	—	40	—	—	ms	
	Interval Between Signals	—	40	—	—	ms	
	Signal Present Without Detection	—	—	—	20	ms	
	Interruption of Signal Without Redetection	—	—	—	20	ms	
	Signal Frequency Deviation With Detection	—	—	±2.5%	±(1.5% + 2)	Hz	
	Signal Frequency Deviation Without Detection	—	±3.5%	±3.0%	—	Hz	
	Twist	—	—	—	±10	dB	2
	Gaussian Noise	—	—	12	A − 7	dB	3
	Dial Tone Level (per tone, F ≤ 480 Hz)	—	—	—	A + 22	dB	4
Digital Input Requirements	Logic 0 Voltage	VP = 12V	0	—	3.6	V	5
		VP = 5V	0	—	1.5	V	5
	Logic 1 Voltage	VP = 12V	8.4	—	12.0	V	5
		VP = 5V	3.5	—	5.0	V	5
Digital Output Characteristics	Logic 0 Voltage	VP = 12V, I_O = 1.0 mA	0	—	1.2	V	5
		VP = 5V, I_O = 0.4 mA	0	—	0.5	V	5
	Logic 1 Voltage	VP = 12V, I_O = −0.5 mA	10.8	—	12.0	V	5
		VP = 5V, I_O = −0.2 mA	4.5	—	5.0	V	5
	Tri-State Leakage	—	—	—	10.0	uA	
Miscellaneous Characteristics	CMOS Latch-up Voltage	—	20	—	—	V	6
	SIGNAL IN Input Impedance	F = 1 kHz, paralleled with 15 pF	100k	—	—	ohms	
Power Requirements	Supply Current	VP = 12V	—	17	40	mA	
		VP = 5V	—	6	18	mA	
	Power Dissipation (Outputs Open)	VP = 12V	—	204	480	mW	7
		VP = 5V	—	30	90	mW	7
	Power Supply Wide Band Noise (A = 0, B = 0)	—	—	—	10	mVpp	

Notes:

1. With an ambient temperature of 25°C, the signal duration and signal interval at minimum, and the signal frequency deviation and twist at maximum. The unit "dBm" refers to decibels above or below a reference power of one milliwatt into a 600-ohm load. (For example, −24 dBm equals 49 mVrms.)

2. Twist is defined as the ratio of the level of the high-frequency DTMF component to the level of the low-frequency DTMF component.

3. With an ambient temperature of 25°C, the signal level at A + 5, the signal frequency deviation and twist at 0, and the signal applied 50 ms off and 50 ms on. The A level is the minimum detect level selected.

4. With the signal duration and signal interval at minimum, and the signal frequency deviation and twist at maximum. The A level is the minimum detect level selected.

5. Logic levels shown are referenced to VND.

6. Power supply excursions above this value can cause device damage.

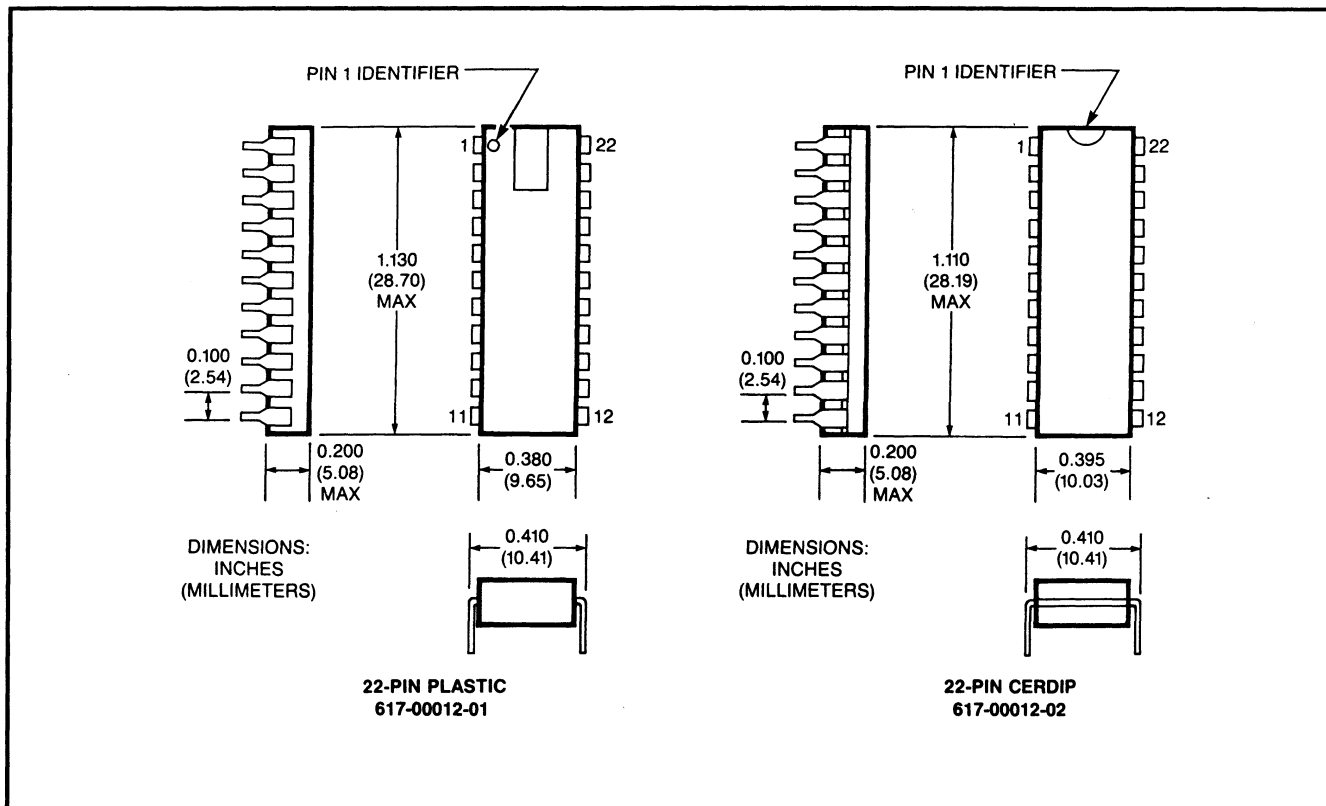7. For an ambient temperature of 25°C.

Figure 8 Package Dimensions

M-957-02 DTMF RECEIVER

The Teltone® M-957-02 (see Figure 1) combines switched-capacitor and digital frequency measuring techniques to decode Dual-Tone Multifrequency (DTMF) signals to four-bit binary data. Dial tone rejection and 60-Hz noise rejection filters are built in. Fabricated as a monolithic integrated circuit using low-power CMOS processing, the M-957-02 is packaged in a 22-pin DIP and operates from a single 5-volt DC supply, as distinguished from the M-957-01 which operates from a wide 5- through 12-volt supply. An inexpensive 3.58-MHz television crystal and resistor are the only external components required. High system density may be achieved by using the clock output of one crystal-connected receiver to drive the time bases of additional receivers.

The SIGNAL IN input to the M-957 (see Figure 2) interfaces readily to telephone lines, radio receivers, tape players, and other DTMF signal sources. Inpus A and B control sensitivity to a maximum of -38 dBm at 5 V, while the 12/16 input determines the signals to be detected. The input stages of the M-957 filter out dial tone and noise, split the signal into its high- and low-frequency components, and hard-limit each component to provide automatic gain control. Four discriminators in each group then detect the individual tones. Postprocessing stages of the M-957 time the tone durations and store binary data for outputting as determined by the HEX

input. The STROBE output is activated by the presence of valid data in the output register and cleared by the detection of a valid end-of-signal pause or by the CLEAR input. An early signal presence indicator, BD, facilitates applications requiring tone blocking. The data outputs operate with simple logic circuits or microprocessors, and are three-state enabled to facilitate bus-oriented architectures.

Features
* Complete DTMF receiver in 22-pin DIP (plastic or CerDIP)
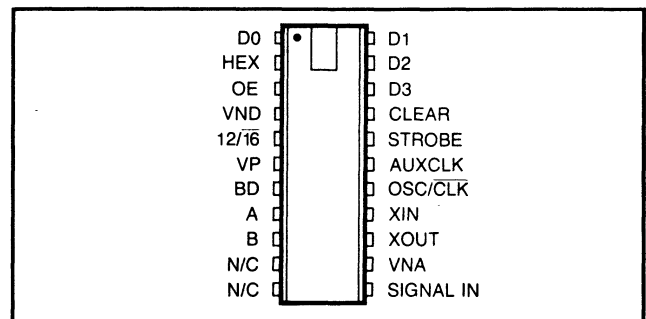* Decodes all 16 DTMF digits
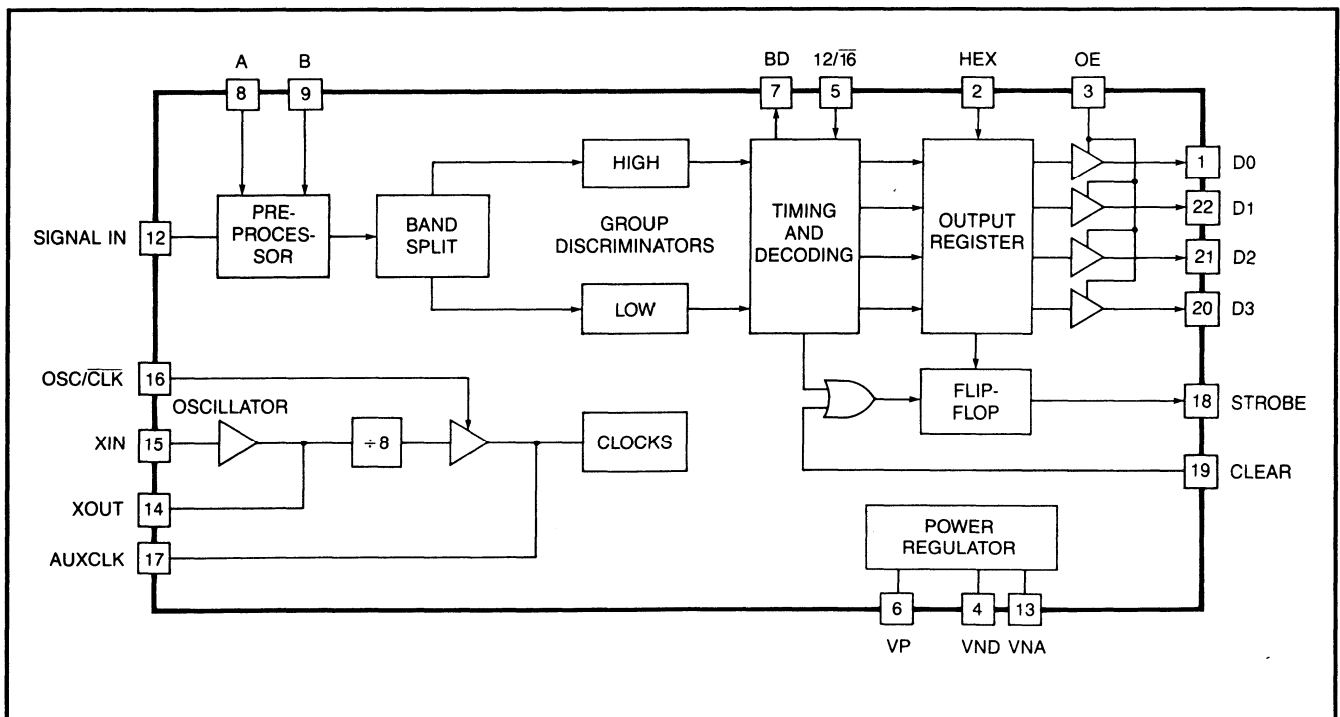

Figure 1 Pin Diagram

Figure 2 Block Diagram

- Excellent dial tone and speech immunity
- Meets telephone impulse noise immunity standards
- Digitally selectable sensitivity to -38 dBm
- Selectable 4-bit hexadecimal or binary coded 2 of 8 output
- Fabricated using low-power CMOS technology
- Operates on single DC supply
- Uses inexpensive 3.58-MHz crystal
- Three-state outputs

Applications

- Central office products
- PBX and key systems
- Radio telephones
- Remote control and monitoring devices
- Computer data entry systems

Table 1 Pin Functions

Pin	Function
SIGNAL IN	DTMF input. Timings are shown in Figure 3. Internally biased so that the input signal may be AC coupled, SIGNAL IN also permits DC coupling as long as the input voltage does not exceed the positive supply. Proper coupling is shown in Figure 5. See Table 2 for the frequency pairs associated with each DTMF signal.
12/$\overline{16}$	DTMF signal detection control. When 12/$\overline{16}$ is at logic "1", the M-957 detects the 12 most commonly used DTMF signals (1 through #). When 12/$\overline{16}$ is at logic "0", the M-957 detects all 16 DTMF signals (1 through D).
A, B	Binary DTMF signal sensitivity control inputs. A and B select the sensitivity of the SIGNAL IN input to a maximum of -31 dBm.
D3, D2, D1, D0	Data outputs. When enabled by the OE input, the data outputs provide the code corresponding to the detected digit in the format programmed by the HEX pin. See Table 2. The data outputs become valid after a tone pair has been detected and are cleared when a valid pause is timed. Timings are shown in Figure 3.
OE	Output enable. When OE is at logic "1", the data outputs are in the CMOS push/pull state and represent the contents of the output register (see Figure 2). When OE is driven to logic "0", the data outputs are forced to the high-impedance or "third" state. Timings are shown in Figure 3.
HEX	Binary output format control. When HEX is at logic "1", the output of the M-957 is full, 4-bit binary. When HEX is at logic "0", the output is binary coded 2-of-8. Table 2 shows the output codes.
STROBE	Valid data indication. STROBE goes to logic "1" after a valid tone pair is sensed and decoded at the data outputs. STROBE remains at logic "1" until a valid pause occurs or the CLEAR input is driven to logic "1", whichever is earlier. Timings are shown in Figure 3.
CLEAR	STROBE control. Driving CLEAR to logic "1" forces the STROBE output to logic "0". When CLEAR is at logic "0", STROBE is forced to logic "0" only when a valid pause is detected. Tie to VNA or VND when not used.
BD	Early signal presence output. BD indicates that a possible signal has been detected and is being validated. As shown in Figure 3, BD precedes STROBE and the data outputs.
XIN, XOUT	Crystal connections. When an auxiliary clock is used, XIN should be tied to logic "1". See Figure 6.
OSC/$\overline{CLK}$	Time base control. When OSC/$\overline{CLK}$ is at logic "1", the output of the M-957's internal oscillator is selected as the time base. When OSC/$\overline{CLK}$ is at logic "0" and XIN is at logic "1", the AUXCLK input is selected as the time base.
AUXCLK	Auxiliary clock input. When OSC/$\overline{CLK}$ is at logic "0" and XIN is at logic "1", the AUXCLK input is selected as the M-957's time base. The auxiliary input must be 3.58 MHz divided by 8 for the M-957 to operate to specifications. If unused, AUXCLK should be left open.
VNA, VND	Negative analog and digital power supply connections. Separated on the chip for greater system flexibility, VNA and VND should be at equal potential.
VP	Positive power supply connection.
N/C	Not connected. These pins have no internal connection and may be left floating.

Table 2 DTMF to Binary Decoding

SIGNAL	LOW-FREQUENCY COMPONENT (Hz)	HIGH-FREQUENCY COMPONENT (Hz)	HEX OUTPUT FORMAT	2-OF-8 OUTPUT FORMAT
			3 2 1 0	3 2 1 0
1	697	1209	0 0 0 1	0 0 0 0
2	697	1336	0 0 1 0	0 0 0 1
3	697	1477	0 0 1 1	0 0 1 0
4	770	1209	0 1 0 0	0 1 0 0
5	770	1336	0 1 0 1	0 1 0 1
6	770	1477	0 1 1 0	0 1 1 0
7	852	1209	0 1 1 1	1 0 0 0
8	852	1336	1 0 0 0	1 0 0 1
9	852	1477	1 0 0 1	1 0 1 0
0	941	1336	1 0 1 0	1 1 0 1
*	941	1209	1 0 1 1	1 1 0 0
#	941	1477	1 1 0 0	1 1 1 0
A	697	1633	1 1 0 1	0 0 1 1
B	770	1633	1 1 1 0	0 1 1 1
C	852	1633	1 1 1 1	1 0 1 1
D	941	1633	0 0 0 0	1 1 1 1

Note: The M-957 detects signals A through D only when the 12/16 input is at logic "0".

Figure 3 Timing Diagram

Figure 4 Telephone Line Differential Input Interface

NOTE: COUPLING
CAPACITOR TO BE USED
WHEN VIN IS GREATER
THAN VP.

Figure 5 Input Signal Configuration

Table 3 Absolute Maximum Ratings (Note 1)

DC Supply Voltage (Note 2).	VNA 7 V
Voltage on SIGNAL IN.	(VP + 0.5 V) to (VNA − 22 V)
Voltage on Any Pin Except SIGNAL IN.	(VP + 0.5 V) to (VND − 0.5 V)
Storage Temperature Range.	−40° to 85° C
Operating Temperature Range.	−40° to 70° C
Lead Soldering Temperature.	260° C for 5 seconds
Power Dissipation.	1W

Notes:

1. Exceeding these ratings may permanently damage the M-957.

2. VP referenced to VND. VND should be at equal potential to VNA. VND/VNA may be at ground.

Figure 6 Multiple Receiver/Microprocessor Interface

Figure 7 Test Circuit

Table 4 Specifications

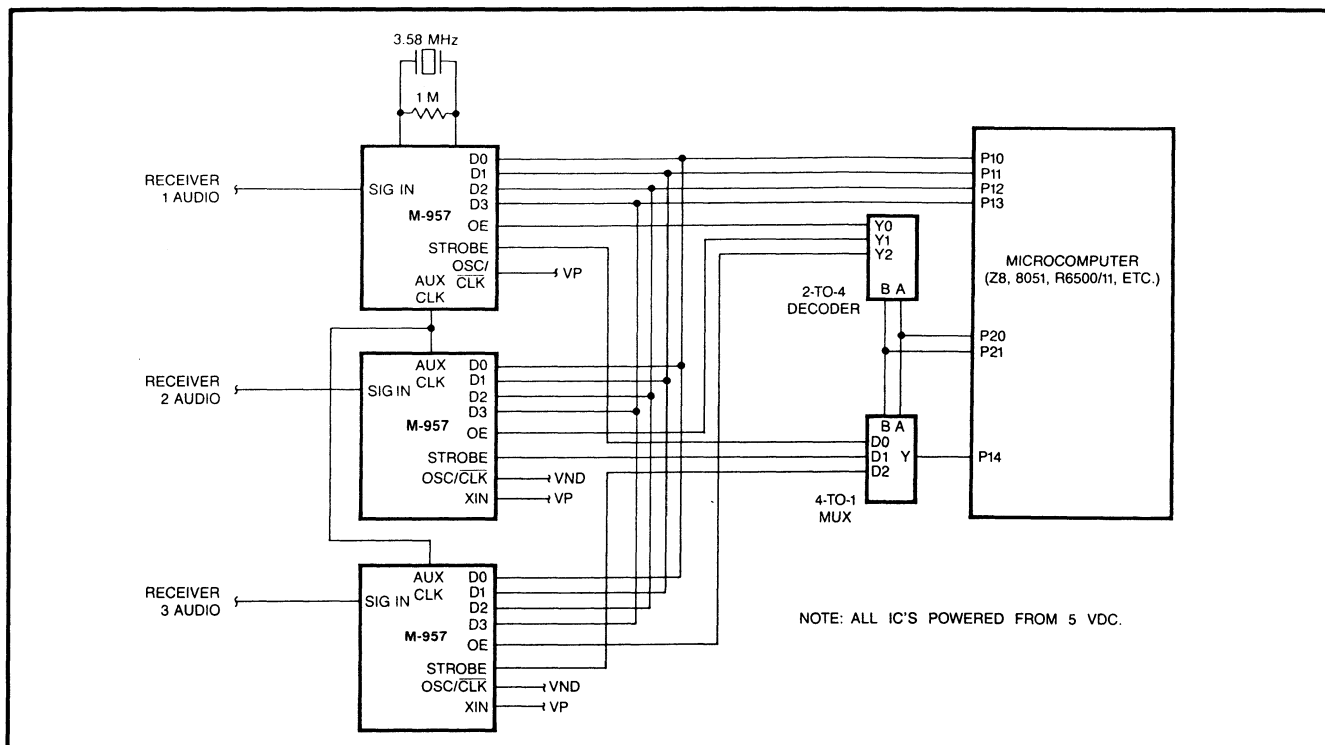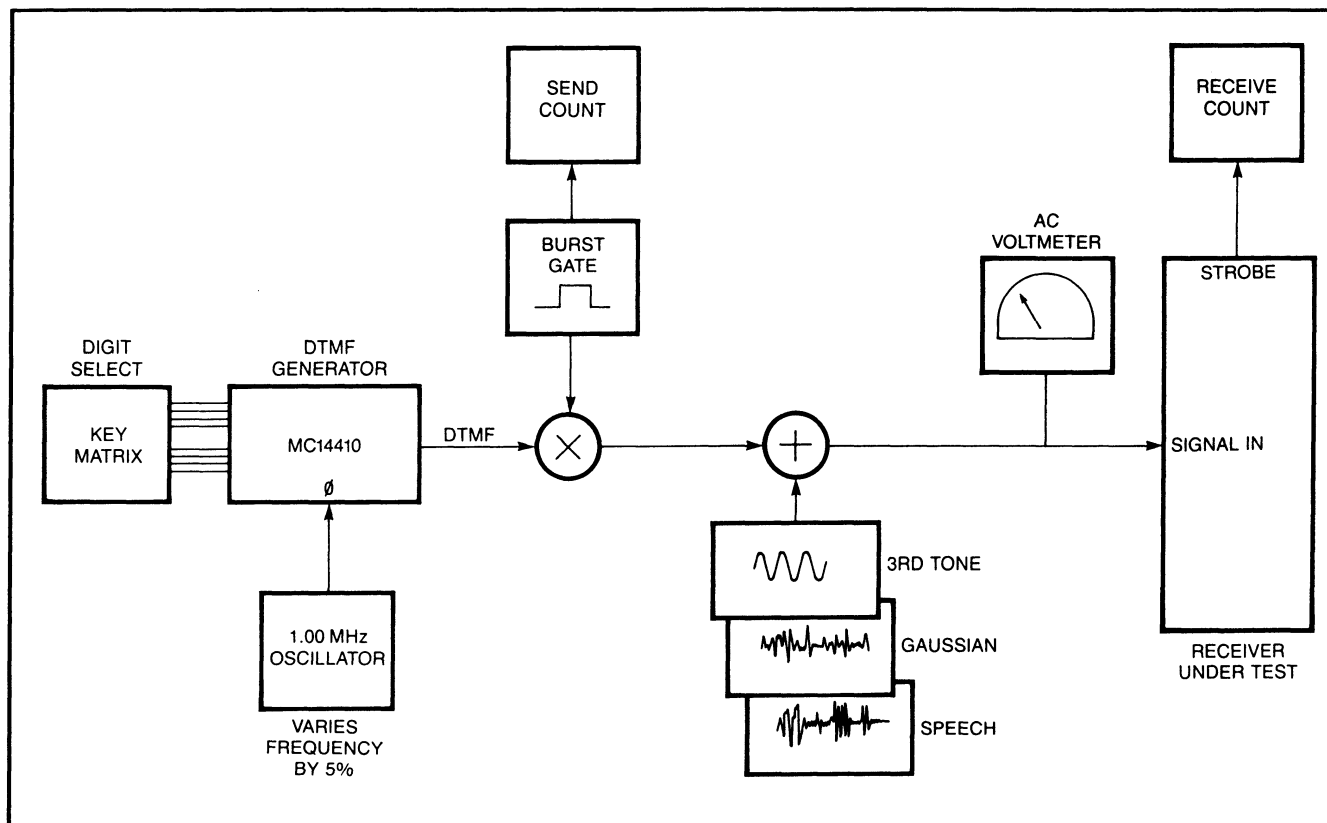|	Parameter	Conditions	Min	Typ	Max	Units	Notes
SIGNAL IN Input Requirements	Signal Level (per tone)	VP = 5 V					
		A = 0, B = 0	−32	—	−2	dBm	1
		A = 1, B = 0	−35	—	−5	dBm	1
		A = 0, B = 1	−38	—	−8	dBm	1
		A = 1, B = 1	—	−40	—	dBm	1
	Signal Duration	—	40	—	—	ms	
	Interval Between Signals	—	40	—	—	ms	
	Signal Present Without Detection	—	—	—	20	ms	
	Interruption of Signal Without Redetection	—	—	—	20	ms	
	Signal Frequency Deviation With Detection	—	—	±2.5%	±(1.5% + 2)	Hz	
	Signal Frequency Deviation Without Detection	—	±3.5%	±3.0%	—	Hz	
	Twist	—	—	—	±10	dB	2
	Gaussian Noise	—	—	12	A − 7	dB	3
	Dial Tone Level (per tone, F ≤ 480 Hz)	—	—	—	A + 22	dB	4
Digital Input Requirements	Logic 0 Voltage		0	—	1.5	V	5
	Logic 1 Voltage		3.5	—	5.0	V	5
Digital Output Characteristics	Logic 0 Voltage	VP = 5 V, I_O = 0.4 mA	0	—	0.5	V	5
	Logic 1 Voltage	VP = 5 V, I_O = −0.2 mA	4.5	—	5.0	V	5
	Tri-State Leakage	—	—	—	10.0	uA	
Miscellaneous Characteristics	CMOS Latch-up Voltage	—	20	—	—	V	7
	SIGNAL IN Input Impedance	F = 1 kHz, paralleled with 15 pF	100k	—	—	ohms	
Power Requirements	Supply Current	VP = 5 V	—	6	18	mA	
	Power Dissipation (Outputs Open)	VP = 5 V	—	30	90	mW	6
	Power Supply Wide Band Noise (A = 0, B = 0)	—	—	—	10	mVpp	

Notes:

1. With an ambient temperature of 25 ° C, the signal duration and signal interval at minimum, and the signal frequency deviation and twist at maximum. The unit "dBm" refers to decibels above or below a reference power of one milliwatt into a 600-ohm load. (For example, − 24 dBm equals 49 mVrms.)

2. Twist is defined as the ratio of the level of the high-frequency DTMF component to the level of the low-frequency DTMF component.

3. With an ambient temperature of 25 ° C, the signal level at A + 5, the signal frequency deviation and twist at 0, and the signal applied 50 ms off and 50 ms on. The A level is the minimum detect level selected.

4. With the signal duration and signal interval at minimum, and the signal frequency deviation and twist at maximum. The A level is the minimum detect level selected.

5. Logic levels shown are referenced to VND.

6. For an ambient temperature of 25 ° C.

7. Power supply excursions above this value can cause device damage.
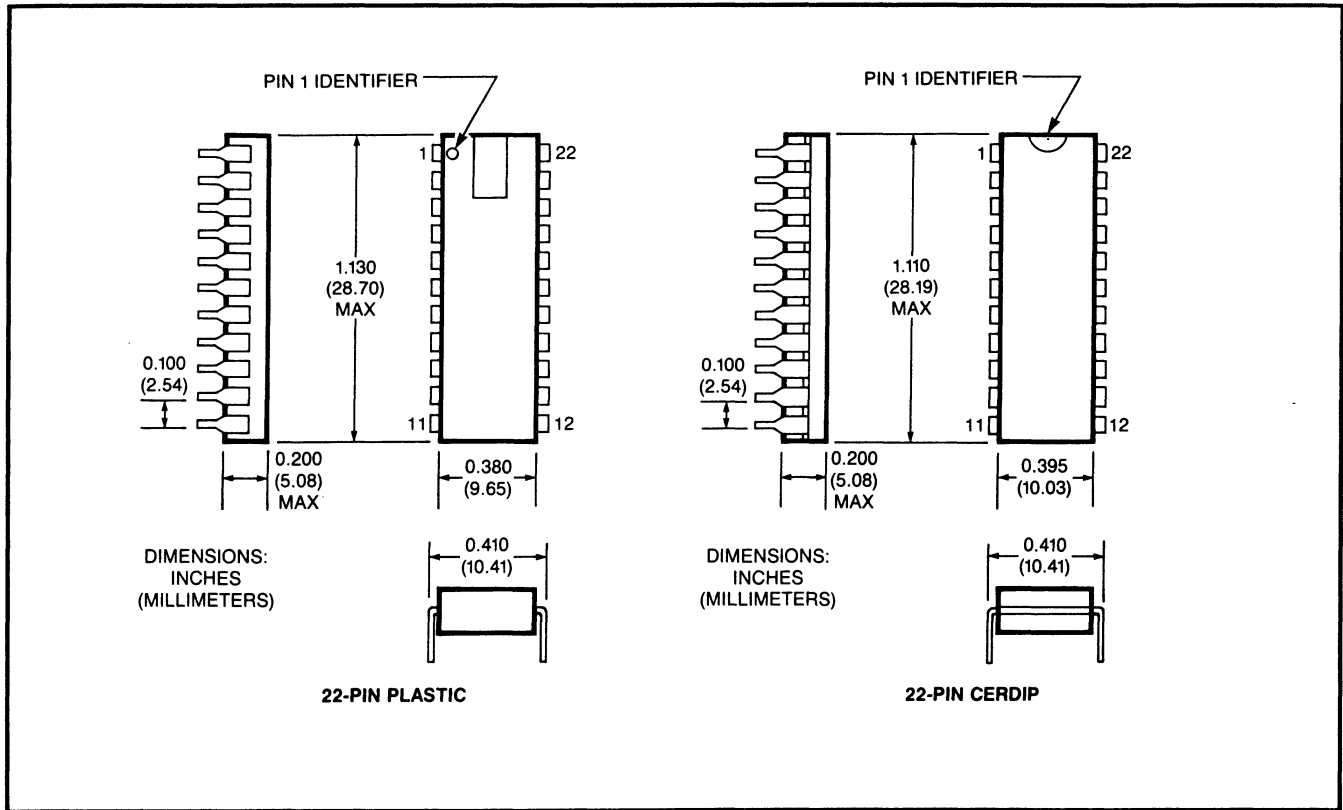
Figure 8 Package Dimensions

M-8870 DTMF RECEIVER

The Teltone® M-8870 is a full DTMF Receiver that integrates both bandsplit filter and decoder functions into a single 18-pin DIP. Manufactured using state-of-the-art CMOS process technology, the M-8870 offers low power consumption (35 mW max) and precise data handling. Its filter section uses switched capacitor technology for both the high and low group filters and for dial tone tone rejection. Its decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by provision of an on-chip differential input amplifier, clock generator, and latched three-state interface bus. The only external component required is a low-cost 3.579545 MHz color burst crystal for the clock generator.

Features

- Low power consumption
- High and low group DTMF filtering
- Adjustable acquisition and release times
- Dial tone suppression
- Integrated bandsplit filter and digital decoder
- Central office quality and performance
- Single 5 volt power supply

Applications

- PBXs
- Central office
- Key systems
- Mobile radio
- Remote control
- Remote data entry

Figure 1 Pin Connections
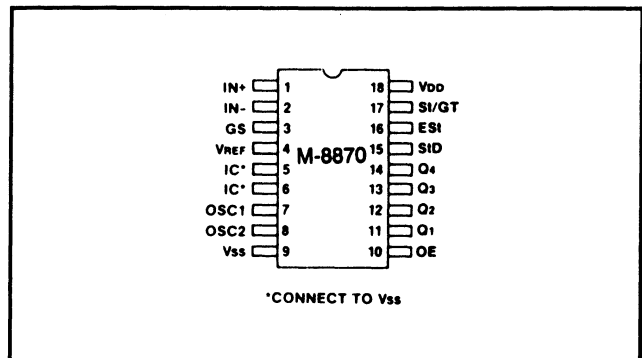
Figure 2 Block Diagram
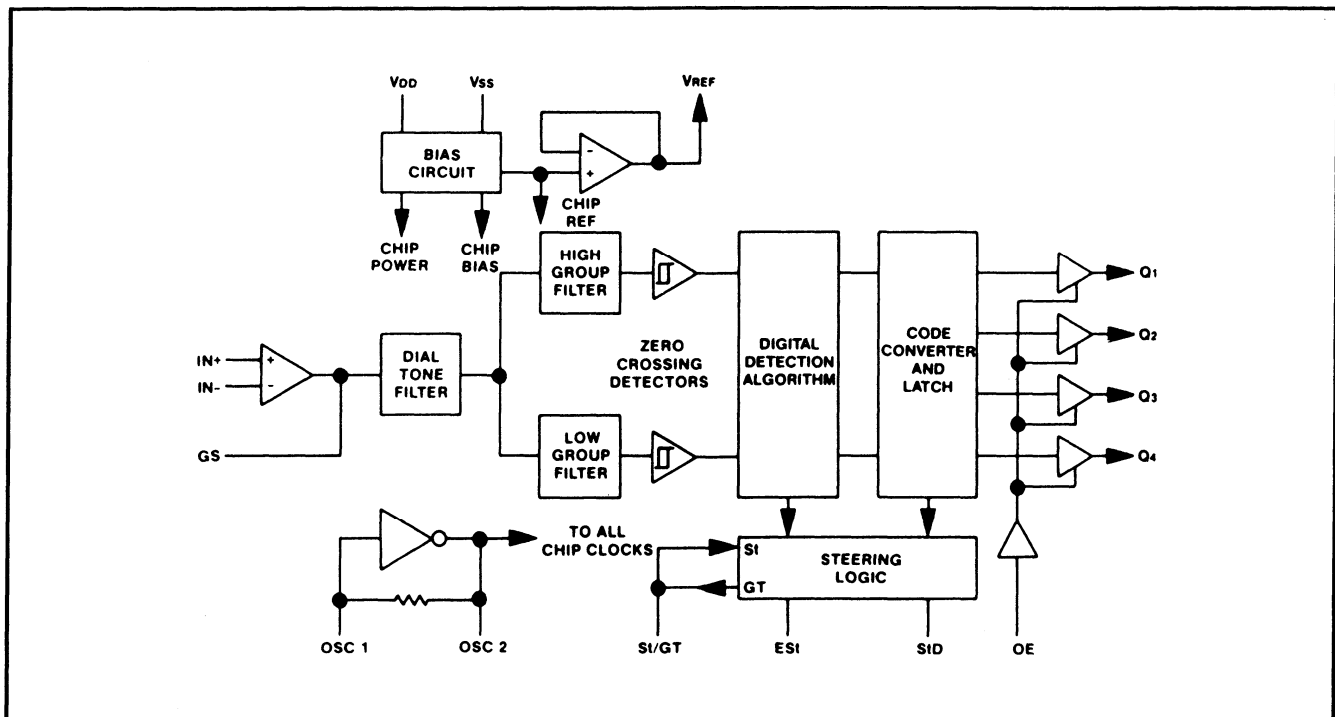
Figure 3 Timing Diagram
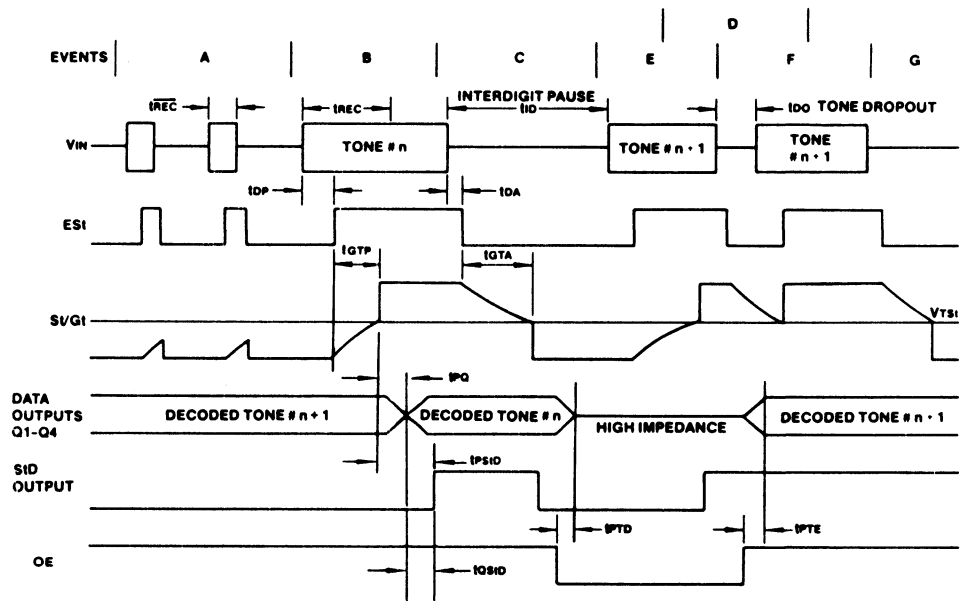
Explanation of Events

(A) Tone bursts detected, tone duration invalid, outputs not updated.

(B) Tone #n detected, tone duration valid, tone decoded and latched in outputs.

(C) End of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.

(D) Outputs switched to high impedance state.

(E) Tone #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).

(F) Acceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.

(G) End of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

Explanation of Symbols

VIN	DTMF composite input signal.
ESt	Early steering output. Indicates detection of valid tone frequencies.
St/GT	Steering input/guard time output. Drives external RC timing circuit.
Q1 - Q4	4-bit decoded tone output.
StD	Delayed steering output. Indicates that valid frequencies have been present/absent for the required guard time, thus constituting a valid signal.
OE	Output enable (input). A low level shifts Q1 - Q4 to its high impedance state.
$t_{\overline{REC}}$	Maximum DTMF signal duration not detected as valid.
t_{REC}	Minimum DTMF signal duration required for valid recognition.
t_{ID}	Minimum time between valid DTMF signals.
t_{DO}	Maximum allowable dropout during valid DTMF signal.
t_{DP}	Time to detect the presence of valid DTMF signals.
t_{DA}	Time to detect the absence of valid DTMF signals.
t_{GTP}	Guard time, tone present.
t_{GTA}	Guard time, tone absent.

FUNCTIONAL DESCRIPTION

M-8870 operating functions (see Figure 2) include a bandsplit filter that separates the high and low tones of the received pair, and a digital decoder that verifies both the frequency and duration of the received tones before passing the resulting 4-bit code to the output bus.

Filter

The low and high group tones are separated by applying the dual-tone signal to the inputs of two 9th order switched capacitor bandpass filters with bandwidths that correspond to the bands enclosing the low and high group tones. The filter also incorporates notches at 350 and 440 Hz, providing excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor section that smooths the signals prior to limiting. Signal limiting is performed by high-gain comparators provided with hysteresis to prevent detection of unwanted low-level signals and noise. The comparator outputs provide full-rail logic swings at the frequencies of the incoming tones.

Decoder

The M-8870 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while tolerating small frequency variations. The algorithm ensures an optimum combination of immunity to talkoff and tolerance to interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the Early Steering flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

Steering Circuit

Before a decoded tone pair is registered, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes V_C (see Figure 4) to rise as the capacitor discharges. Provided that signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (see Table 6) into the output latch. At this point, the GT output is activated and drives V_C to V_{DD}. GT continues to drive high as lsong as ESt remains high. Finally, after a short delay to allow the output latch to settle, the "delayed steering" output flag (StD) goes high, signaling that a received tone pair has been registered. The contents of

$$t_{GTA} = RC \ln\left(\frac{V_{DD}}{V_{TSt}}\right)$$

$$t_{GTP} = (RC) \ln\left(\frac{V_{DD}}{V_{DD} - V_{TSt}}\right)$$
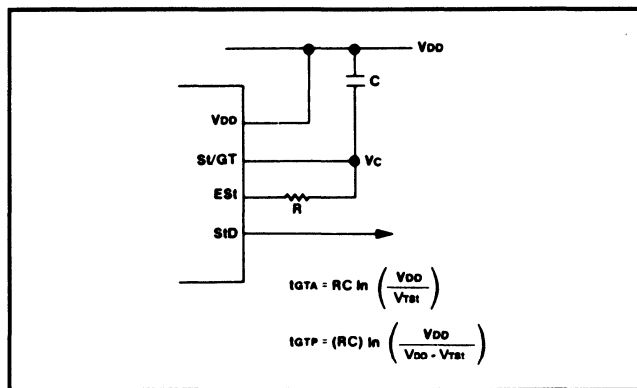
Figure 4 Basic Steering Circuit

All resistors are ±1% tolerance.
All capacitors are ±5% tolerance.

Figure 5 Single-Ended Input Configuration

$$t_{GTP} = (R_1 C) \ln\left(\frac{V_{DD}}{V_{DD} - V_{TSt}}\right)$$

$$t_{GTA} = (R_P C) \ln\left(\frac{V_{DD}}{V_{TSt}}\right)$$

$$R_P = \frac{R_1 R_2}{R_1 + R_2}$$

a) Decreasing t_{GTA} ($t_{GTP} > t_{GTA}$)

$$t_{GTP} = (R_p C) \ln\left(\frac{V_{DD}}{V_{DD} - V_{TSt}}\right)$$

$$t_{GTA} = (R_1 C) \ln\left(\frac{V_{DD}}{V_{TSt}}\right)$$

$$R_P = \frac{R_1 R_2}{R_1 + R_2}$$

b) Decreasing t_{GTP} ($t_{GTP} < t_{GTA}$)
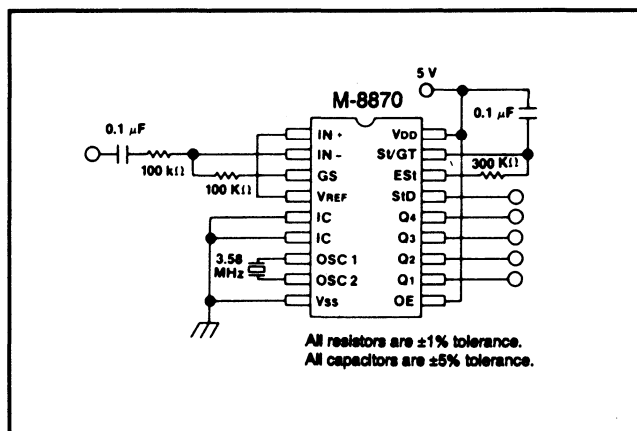
Figure 6 Guard Time Adjustment

the output latch are made available on the 4-bit output bus by raising the three-state control input (OE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropouts) too short to be considered a valid pause. This capability, together with the ability to select the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

Where independent selection of receive and pause are not required, the simple steering circuit of Figure 4 is applicable. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{GTP} \approx 0.67\,RC$$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40 ms would be 300 K ohm. A typical circuit using this steering configuration is shown in Figure 5. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guard times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specifications that place both accept and reject limits on both tone duration and interdigit pause.

Guard time adjustment also allows the designer to tailor system parameters such as talkoff and noise immunity. Increasing t_{REC} improves talkoff performance, since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast
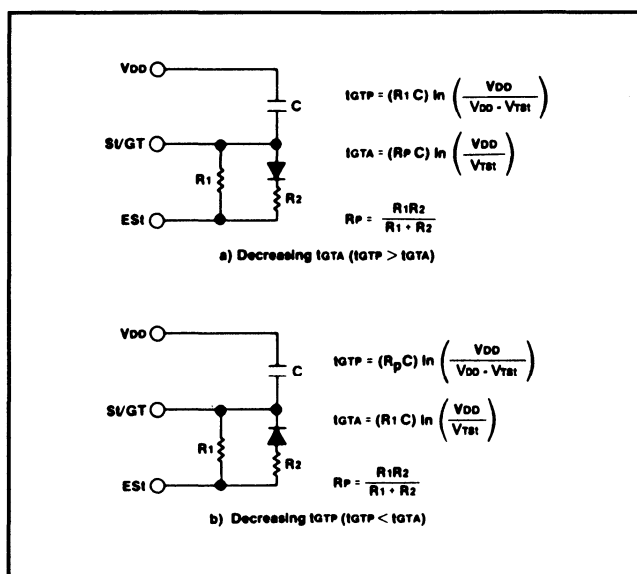
acquisition time and immunity to dropouts would be required. Design information for guard time adjustment is shown in Figure 6.

Input Configuration

The input arrangement of the M-8870 provides a differential input operational amplifier as well as a bias source (V_{REF}) to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for gain adjustment.

In a single-ended configuration, the input pins are connected as shown in Figure 5 with the op-amp connected for unity gain and V_{REF} biasing the input at $1/2V_{DD}$. Figure 7 shows the differential configuration, which permits gain adjustment with the feedback resistor R5.

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard 3.579545 MHz television color burst crystal. The crystal can be connected to a single M-8870 as shown in Figure 5, or to a series of M-8870s. As illustrated in Figure 8, a single crystal can be used to connect a series of M-8870s by coupling the oscillator output of each M-8870 through a 30 pF capacitor to the oscillator input of the next M-8870.
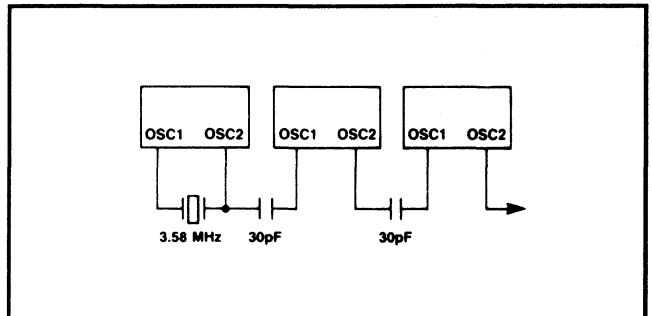
Figure 8 Common Crystal Connection

Figure 7 Differential Input Configuration
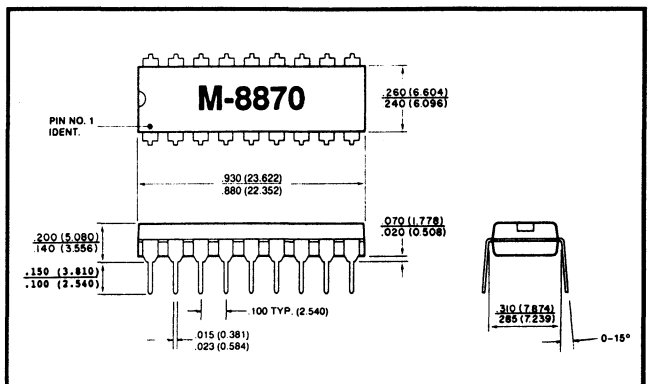
Figure 9 Package Dimensions

Table 1 Absolute Maximum Ratings

Parameter	Ssymbol	Value
Power supply voltage (V_{DD} - V_{SS})	V_{DD}	6.0 V max
Voltage on any pin	V_{dc}	V_{SS} -0.3, V_{DD} +0.3
Current on any pin	I_{DD}	10 mA max
Operating temperature	T_A	-40 °C to +85 °C
Storage temperature	T_S	-65 °C to +150 °C

Note: Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Table 2 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test conditions
Operating supply voltage	V_{DD}	4.75		5.25	V	
Operating supply current	I_{DD}		3.0	7.0	mA	
Power consumption	P_O		15	35	mW	f = 3.579 MHz, V_{DD} = 5.0 V
Low level input voltage	V_{IL}			1.5	V	
High level input voltage	V_{IH}	3.5			V	
Input leakage current	I_{IH}/I_{IL}			0.1	μA	V_{IN} = V_{SS} or V_{DD}
Pullup (source) current on OE	I_{SO}		6.5	15.0	μA	OE = 0 V
Input impedance, signal inputs 1, 2	R_{IN}	8	10		M Ω	@ 1 kHz
Steering threshold voltage	V_{TSt}	2.2		2.5	V	
Low level output voltage	V_{OL}			0.03	V	No load
High level output voltage	V_{OH}	4.97			V	No load
Output low (sink) current	I_{OL}	1.0	2.5		mA	V_{OUT} = 0.4 V
Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6 V
Output voltage V_{REF}	V_{REF}	2.4		2.7	V	No load
Output resistance V_{REF}	R_{OR}			10	kΩ	

All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0V, V_{SS} = 0 V, T_A = 25 °C

Table 3 Operating Characteristics—Gain Setting Amplifier

Parameter	Symbol	Min	Typ	Max	Units	Test conditions
Input leakage current	I_{IN}			±100	nA	V_{SS} < V_{IN} < V_{DD}
Input resistance	R_{IN}	10			MΩ	
Input offset voltage	V_{OS}		±25		mV	
Power supply rejection	PSRR	50			dB	1 kHz
Common mode rejection	CMRR	55			dB	-3.0 V < V_{IN} < 3.0 V
DC open loop voltage gain	A_{VOL}	60			dB	
Open loop unity gain bandwidth	f_C	1.2	1.5		MHz	
Output voltage swing	V_O	3.5			V_{P-P}	R_L ≥ 100 kΩ to V_{SS}
Tolerable capacitive load (GS)	C_L			100	pF	
Tolerable resistive load (GS)	R_L			50	kΩ	
Common mode range	V_{CM}	2.5			V_{P-P}	No load

All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0 V, V_{SS} = 0 V, T_A = 25 °C.

Table 4 AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Notes
Valid input signal levels (each tone of composite signal)		-29		+1	dBm	1,2,3,4,5,8
		27.5		869	mVRMS	
Positive twist accept				10	dB	2,3,4,8
Negative twist accept				10	dB	
Frequency deviation accept limit				1.5% ±2 Hz	Nom.	2,3,5,8,10
Frequency deviation reject limit		±3.5%			Nom.	2,3,5
Third tone tolerance		-25	-16		dB	2,3,4,5,8,9,13,14
Noise tolerance			-12		dB	2,3,4,5,6,8,9
Dial tone tolerance		+18	+22		dB	2,3,4,5,7,8,9
Tone present detection time	t_{DP}	5	8	14	ms	See Figure 3
Tone absent detection time	t_{DA}	0.5	3	8.5	ms	
Minimum tone duration accept	t_{REC}			40	ms	User adjustable (times shown are obtained with circuit in Figure 5)
Maximum tone duration reject	$\overline{t_{REC}}$	20			ms	
Minimum interdigit pause accept	t_{ID}			40	ms	
Maximum interdigit pause reject	t_{DO}	20			ms	
Propagation delay (St to Q)	t_{PQ}		6	11	µs	OE = V_{DD}
Propagation delay (St to StD)	t_{PStD}		9		µs	
Output data setup (Q to StD)	t_{QStD}		4.0		ms	
Propagation delay (OE to Q), enable	t_{PTE}		50	60	ns	R_L = 10kΩ, C_L = 50 pF
Propagation delay (OE to Q), disable	t_{PTD}		300		ns	
Crystal clock frequency	f_{CLK}	3.5759	3.5795	3.5831	MHz	
Clock output (OSC2), capacitive load	C_{LO}			30	pF	

All voltages referenced to VSS unless otherwise noted. VDD = 5.0 V, VSS = 0 V, TA = 25 °C, fCLK = 3.579545 MHz using circuit in Figure 5.

Notes:
1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 ms. Tone pause = 40 ms.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3 kHz) Gaussian noise.
7. The precise dial tone frequencies are (350 and 440 Hz) ± 2%.
8. For an error rate of better than 1 in 10,000.
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. Input pins defined as IN+, IN-, and OE.
12. External voltage source used to bias VREF.
13. This parameter also applies to a third tone injected onto the power supply.
14. Referenced to Figure 5. Input DTMF tone level at -28 dBm.

Table 5 Pin Functions

Name	Description	
IN+	Non-inverting input	Connections to the front-end differential amplifier
IN-	Inverting input	
GS	Gain select. Gives access to output of front-end amplifier for connection of feedback resistor.	
V_{REF}	Reference voltage output (nominally $V_{DD}/2$). May be used to bias the inputs at mid-rail.	
IC	Internal connection. Must be tied to V_{SS}.	
IC	Internal connection. Must be tied to V_{SS}.	
OSC1	Clock input	3.579545 MHz crystal connected between these pins completes internal oscillator.
OSC2	Clock output	
V_{SS}	Negative power supply (normally connected to 0 V).	
OE	Three-state output enable (input). Logic high enables the outputs Q1 - Q4. Internal pullup.	
Q1, Q2, Q3, Q4	Three-state outputs. When enabled by OE, provides the code corresponding to the last valid tone pair received (see Table 6.)	
StD	Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below V_{TSt}.	
ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.	
St/GT	Steering input/guard time output (bidirectional). A voltage greater than VTSt detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than VTSt frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant, and its state is a function of ESt and the voltage on St. (See Table 6).	

Table 6 Tone Decoding

F_{LOW}	F_{HIGH}	KEY (ref.)	OE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
ANY	ANY	ANY	L	Z	Z	Z	Z

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M-8880 DTMF TRANSCEIVER

The M-8880 is a complete DTMF Transmitter/Receiver that features adjustable guard time, automatic tone burst mode, call progress mode, and a fully compatible 6500/6800 microprocessor interface. The receiver portion is based on the industry standard M-8870 DTMF Receiver, while the transmitter uses a switched-capacitor digital-to-analog converter for low-distortion, highly accurate DTMF signaling. Tone bursts can be transmitted with precise timing by making use of the automatic tone burst mode. To analyze call progress tones, a call progress filter can be selected by an external microprocessor.

Features

* Advanced CMOS technology for low power consumption and increased noise immunity
* Complete DTMF transmitter/receiver in a single chip
* Standard 6500/6800 series microprocessor port
* Central office quality and performance
* Adjustable guard time
* Automatic tone burst mode
* Call progress mode
* Single +5 Volt power supply
* 20-pin DIP
* 2 MHz microprocessor port operation
* No continuous $\phi2$ clock required, only strobe

Applications

* Paging systems
* Repeater systems/mobile radio
* Interconnect dialers
* PBX systems
* Computer systems
* Fax machines
* Pay telephones
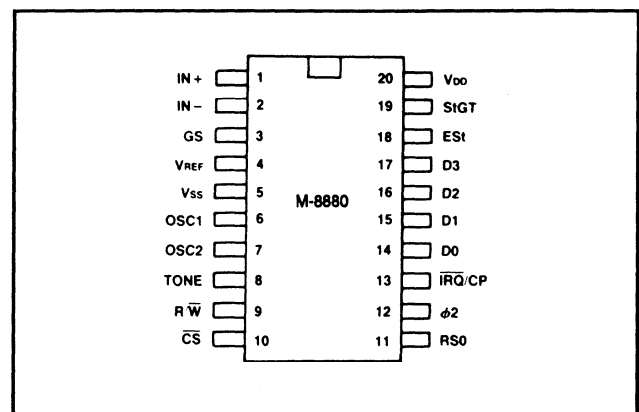* Credit card verification
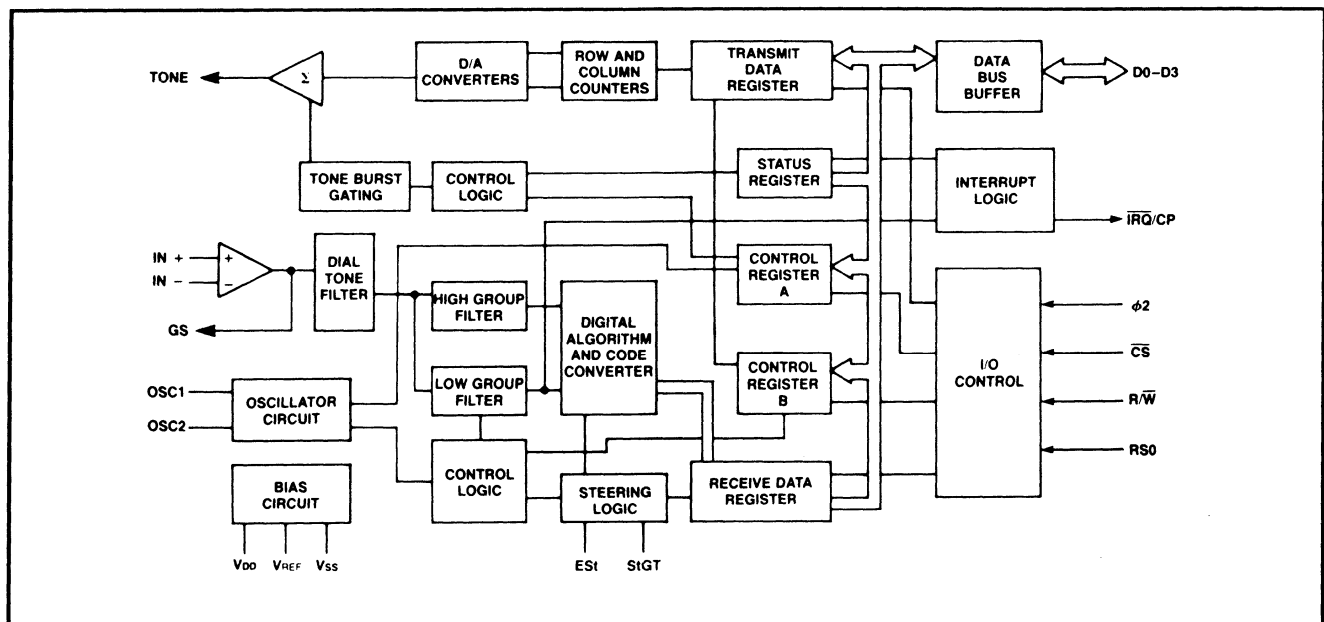

Figure 1 Pin Connections

Figure 2 Block Diagram

A. General Transceiver Timing

Explanation of Events

A	Tone bursts detected, tone duration invalid, RX data register not updated.
B	Tone #n detected, tone duration valid, tone decoded and latched in RX data register.
C	End of tone #n detected, tone absent duration valid, information in RX data register retained until next valid tone pair.
D	Tone #n + 1 detected, tone duration valid, tone decoded and latched in RX data register.
E	Acceptable dropout of tone #n + 1, tone absent duration invalid, data remains unchanged.
F	End of tone #n + 1 detected, tone absent duration valid, information in RX data register retained until next valid tone pair.

Explanation of Symbols

V_{IN}	DTMF composite input signal.
ESt	Early steering output. Indicates detection of valid tone frequencies.
St/GT	Steering input/guard time output. Drives external RC timing circuit.
RX_0-RX_3	4-bit decoded data in receive data register.
b_3	Delayed steering. Indicates that valid frequencies have been present/absent for the required guard time thus constituting a valid signal. Active low for the duration of a valid DTMF signal.
b_2	Indicates that valid data is in the receive data register. The bit is cleared after the status register is read.
$\overline{IRQ}$/CP	Interrupt is active indicating that new data is in the RX data register. The interrupt is cleared after the status register is read.
$\overline{t_{REC}}$	Maximum DTMF signal duration not detected as valid.
t_{REC}	Minimum DTMF signal duration required for valid recognition.
t_{ID}	Minimum time between valid sequential DTMF signals.
t_{DO}	Maximum allowable dropout during valid DTMF signal.
t_{DP}	Time to detect valid frequencies present.
t_{DA}	Time to detect valid frequencies absent.
t_{GTP}	Guard time, tone present.
t_{GTA}	Guard time, tone absent.

Figure 3 Timing Diagrams

B. Microprocessor Read Cycle

C. Microprocessor Write Cycle

Figure 3 Timing Diagrams (concluded)

A. Test load for D0—D3 pins

B. Test load for IRQ/CP pin
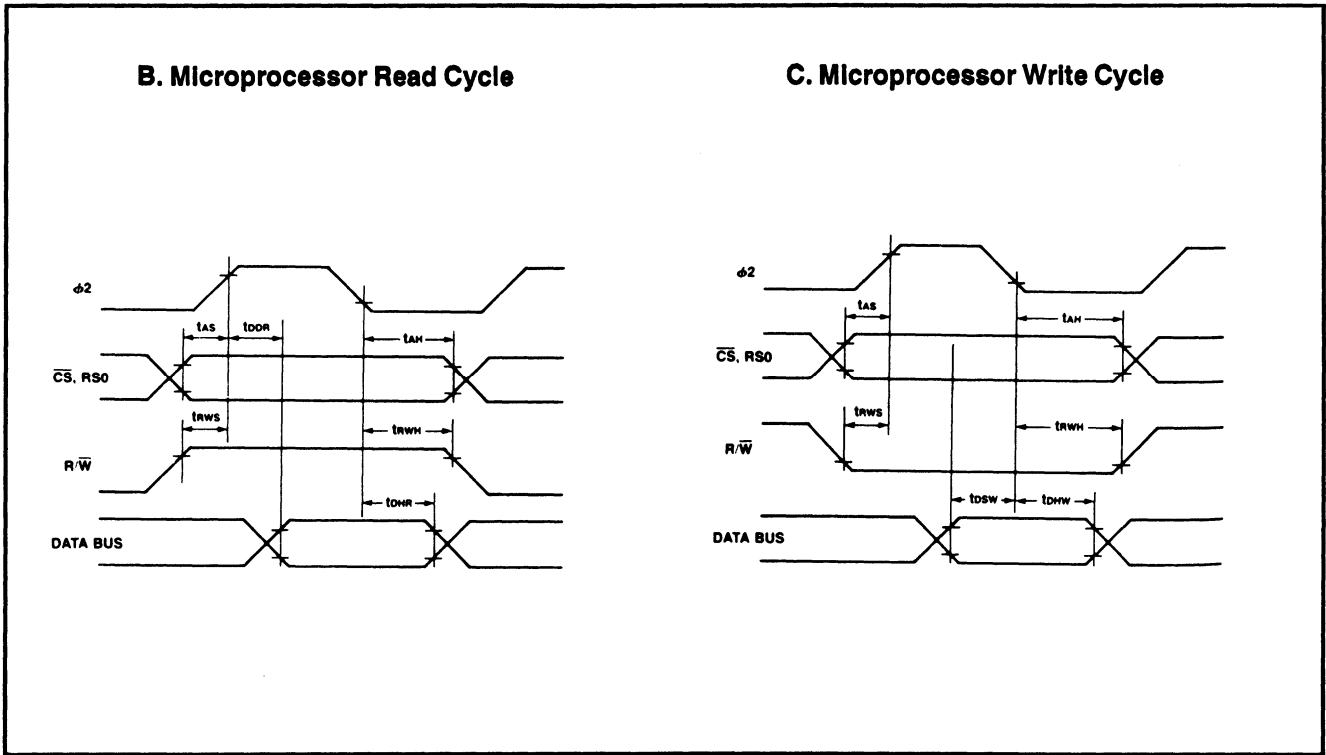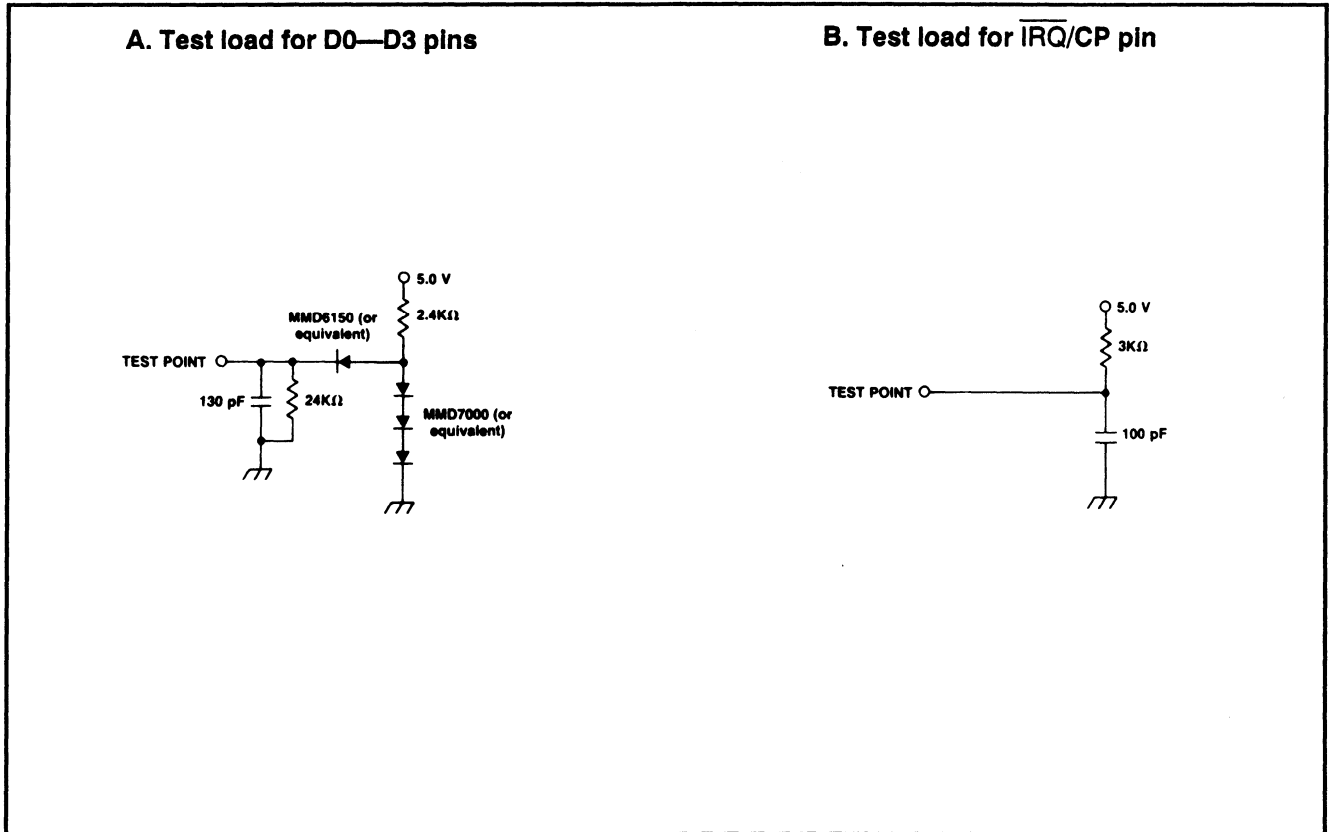

Figure 4 Test Loads

FUNCTIONAL DESCRIPTION

M-8880 functions consist of a high-performance DTMF receiver with an internal gain setting amplifier and a DTMF generator that contains a tone burst counter for generating precise tone bursts and pauses. The call progress mode, when selected, allows the detection of call progress tones. A standard 6500/6800 series microprocessor interface allows access to an internal status register, two control registers, and two data registers.

Input Configuration

The input arrangement consists of a differential input operational amplifier and bias sources (V_{REF}) for biasing the amplifier inputs at $V_{DD}/2$. Provisions are made for the connection of a feedback resistor to the op-amp output (GS) for gain adjustment. In a single-ended configuration, the input pins should be connected as shown in Figure 5. Figure 6 shows the necessary connections for a differential input configuration.
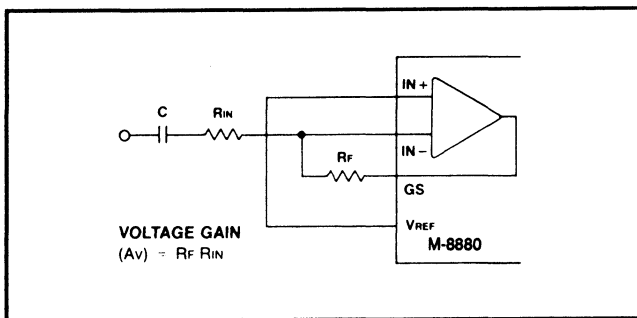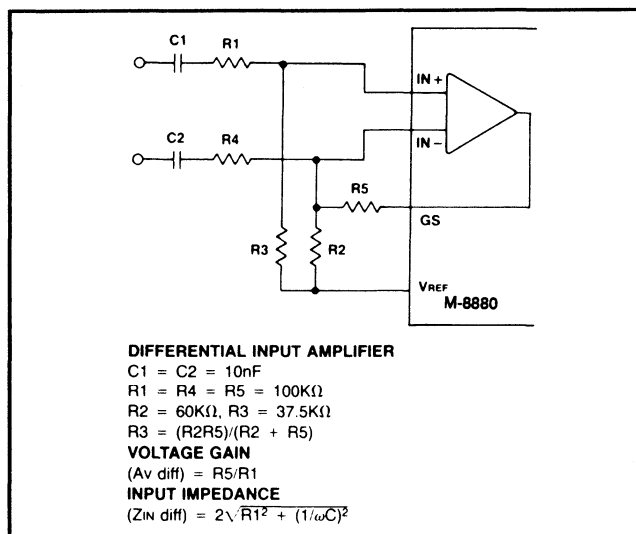

Figure 5 Single-Ended Input Configuration

DIFFERENTIAL INPUT AMPLIFIER
C1 = C2 = 10nF
R1 = R4 = R5 = 100KΩ
R2 = 60KΩ, R3 = 37.5KΩ
R3 = (R2R5)/(R2 + R5)
VOLTAGE GAIN
(Av diff) = R5/R1
INPUT IMPEDANCE
(Zin diff) = $2\sqrt{R1^2 + (1/\omega C)^2}$

Figure 6 Differential Input Configuration

Receiver Section

The low and high group tones are separated by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters with bandwidths that correspond to the low and high group frequencies listed in Table 1. The low group filter incorporates notches at 350 and 440 Hz, providing excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor filter that smooths the signals prior to limiting. Limiting is performed by high-gain comparators with hysteresis to prevent detection of unwanted low-level signals. The comparator outputs provide full-rail logic swings at the incoming DTMF signal frequencies.

A decoder employs digital counting techniques to determine the frequencies of the incoming tones, and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals (such as voice), while tolerating small deviations in frequency. The algorithm provides an optimum combination of immunity to talkoff with tolerance to interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (referred to as "signal condition"), the early steering (ESt) output goes to an active

Table 1 Tone Encoding/Decoding						
F_{LOW}	F_{HIGH}	DIGIT	D3	D2	D1	D0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0
0 = logic low, 1 = logic high						

state. Any subsequent loss of signal condition will cause ESt to assume an inactive state.

Steering Circuit: Before a decoded tone pair is registered, the receiver checks for a valid signal duration (referred to as "character recognition condition"). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes V_C (see Figure 7) to rise as the capacitor discharges. Provided that the signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the receive data register.
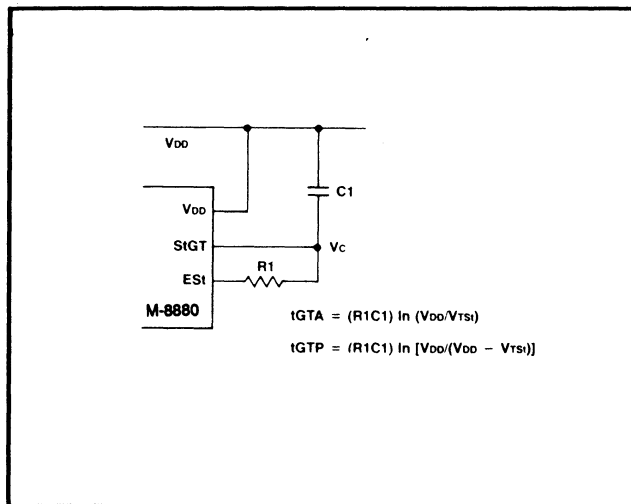
Figure 7 Basic Steering Circuit

$t_{GTA} = (R1C1) \ln (V_{DD}/V_{TSt})$

$t_{GTP} = (R1C1) \ln [V_{DD}/(V_{DD} - V_{TSt})]$

a) decreasing t_{GTP} $(t_{GTP} < t_{GTA})$

$t_{GTP} = (R_PC1) \ln [V_{DD}/(V_{DD} - V_{TSt})]$

$t_{GTA} = (R1C1) \ln (V_{DD}/V_{TSt})$

$R_P = (R1R2)/(R1 + R2)$

b) decreasing t_{GTA} $(t_{GTP} > t_{GTA})$

$t_{GTP} = (R_1C1) \ln [V_{DD}/(V_{DD} - V_{TSt})]$

$t_{GTA} = (R_PC1) \ln (V_{DD}/V_{TSt})$

$R_P = (R1R2)/(R1 + R2)$

Figure 8 Guard Time Adjustment

At this point the GT output is activated and drives V_C to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag goes high, signaling that a received tone pair has been registered. It is possible to monitor the status of the delayed steering flag by checking the appropriate bit in the status register. If interrupt mode has been selected, the IRQ/CP pin will pull low when the delayed steering flag is active.

The contents of the output latch are updated on an active delayed steering transition. This data is presented to the 4-bit bidirectional data bus when the receive data register is read. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropout) too short to be considered a valid pause. This capability, together with the ability to select the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment: The simple steering circuit shown in Figure 7 is adequate for most applications. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$T_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 µF is recommended for most applications, leaving R to be selected by the designer. Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications that place both accept and reject limits on both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameters such as talkoff and noise immunity. Increasing t_{REC} improves talkoff performance since it reduces the probability that tones simulated by speech will

Figure 9 Call Progress Response

maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone dropouts are required. Design information for guard time adjustment is shown in Figure 8.

Call Progress Filter

A call progress (CP) mode can be selected, allowing the detection of various tones that identify the progress of a telephone call on the network. The call progress tone input and DTMF input are common; however, call progress tones can only be detected when the CP mode has been selected. DTMF signals cannot be detected if the CP mode has been selected (see Table 2). Figure 9 indicates the useful detect bandwidth of the call progress filter. Frequencies presented to the input (IN+ and IN-) that are within the "accept" bandwidth limits of the filter are hard-limited by a high-gain

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Table 2 Control Register A Description

Bit	Name	Function	Description
b0	TOUT	Tone output	A logic 1 enables the tone output. This function can be implemented in either the burst mode or nonburst mode.
b1	CP/$\overline{\text{DTMF}}$	Mode control	In DTMF mode (logic 0), the device is capable of generating and receiving DTMF signals. When the call progress (CP) mode is selected (logic 1), a 6th-order bandpass filter is enabled to allow call progress tones to be detected. Call progress tones within the specified bandwidth will be presented at the $\overline{\text{IRQ}}$/CP pin in rectangular wave format if the IRQ bit has been enabled (b2 = 1). Also, when the CP mode and burst mode have both been selected, the transmitter will issue DTMF signals with a burst and pause of 102 ms (typ) duration. This signal duration is twice that obtained from the DTMF transmitter, if DTMF mode had been selected. Note that DTMF signals cannot be decoded when the CP mode has been selected.
b2	IRQ	Interrupt enable	A logic 1 enables the interrupt mode. When this mode is active and the DTMF mode has been selected (b1 = 0), the $\overline{\text{IRQ}}$/CP pin will pull to a logic 0 condition when either (1) a valid DTMF signal has been received and has been present for the guard time or (2) the transmitter is ready for more data (burst mode only).
b3	RSEL	Register select	A logic 1 selects control register B on the next write cycle to the control register address. Subsequent write cycles to the control register are directed back to control register A.

Table 3 Control Register B Description

Bit	Name	Function	Description
b0	BURST	Burst mode	A logic 0 enables the burst mode. When this mode is selected, data corresponding to the desired DTMF tone pair can be written to the transmit data register, resulting in a tone burst of a specific duration (see Table 13). Subsequently, a pause of the same duration is induced. Immediately following the pause, the status register is updated indicating that the transmit data register is ready for further instructions, and an interrupt will be gneerated if the interrupt mode has been enabled. Additionally, if call progress (CP) mode has been enabled, the burst and pause duration is increased by a factor of two. When the burst mode is not selected (logic 1), tone bursts of any desired duration may be generated.
b1	TEST	Test mode	By enabling the test mode (logic 1), the $\overline{\text{IRQ}}$/CP pin will present the delayed steering (inverted) signal from the DTMF receiver. Refer to Figure 3A (b3 waveform) for details concerning the output waveform. DTMF mode must be selected (CRA b1 = 0) before test mode can be implemented.
b2	S/$\overline{\text{D}}$	Single/dual tone generation	A logic 0 will allow DTMF signals to be produced. If single-tone generation is enabled (logic 1), either now or column tones (low or high group) can be generated depending on the state of b3 in control register B.
b3	C/$\overline{\text{R}}$	Column/row tones	When used in conjunction with b2 (above), the transmitter can be made to generate single-row or single-column frequencies. A logic 0 will select row frequencies and a logic 1 will select column frequencies.

comparator with the IRQ/CP pin serving as the output. The square wave output obtained from the schmitt trigger can be analyzed by a microprocessor or counter arrangement to determine the nature of the call progress tone being detected. Frequencies in the "reject" area will not be detected, and consequently there will be no activity on IRQ/CP as a result of these frequencies.

DTMF Generator

The DTMF transmitter used in the M-8880 is capable of generating all 16 standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.58 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor digital-to-analog converters. The row and column tones are mixed and filtered, providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal, data conforming to the encoding format shown in Table 1 must be written to the transmit data register. Note that this is the same as the receiver output code. The individual tones that are generated (f_{LOW} and f_{HIGH}) are referred to as low-group and high-group tones. Typically, the high-group to low-group amplitude ratio (twist) is 2 dB to compensate for high-group attenuation on long loops.

Operation: During write operations to the transmit data register, 4-bit data on the bus is latched and converted to a 2 of 8 code for use by the programmable divider circuitry to

$$THD(\%) = 100 \frac{\sqrt{V^2{}_{2f} + V^2{}_{3f} + V^2{}_{4f} + ...V^2{}_{nf}}}{V_{fundamental}}$$

Equation 1. THD(%) for a Single Tone

$$THD(\%) = 100 \frac{\sqrt{V^2{}_{2L} + V^3{}_{3L} + ...V^2{}_{nL} + V^2{}_{2H} + V^2{}_{3H} + ...V^2{}_{nH} + V^2{}_{IMD}}}{\sqrt{V^2{}_{L} + V^2{}_{H}}}$$

Equation 2. THD(%) for a Dual Tone

The M-8880 is initialized on powerup sequence with DTMF mode and burst mode selected.

Single-Tone Generation: A single-tone mode is available whereby individual tones from the low group or high group can be generated. This mode can be used for DTMF test equipment applications, acknowledgement tone generation, and distortion measurements. Refer to Table 3 for details.

Distortion Calculations: The M-8880 is capable of producing precise tone bursts with minimal error in frequency (see Table 4). The internal summing amplifier is followed by a first-order low-pass switched capacitor filter to minimize harmonic components and intermodulation products. The total harmonic distortion for a *single* tone can be calculated using Equation 1, which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage. The Fourier components of the tone output correspond to V2f... Vnf as measured on the output waveform. The total harmonic distortion for a *dual* tone can be calculated using Equation 2.

V_L and V_H correspond to the low-group and high-group amplitude, respectively, and $V^2{}_{IMD}$ is the sum of all the intermodulation components. The internal switched capacitor filter following the D/A converter keeps distortion products down to a very low level.

specify a time segment length that will ultimately determine the tone frequency. The number of time segments is fixed at 32, but the frequency is varied by varying the segment length. When the divider reaches the appropriate count as determined by the input code, a reset pulse is issued and the counter starts again. The divider output clocks another counter that addresses the sinewave lookup ROM. The lookup table contains codes used by the switched capacitor D/A converter to obtain discrete and highly accurate DC voltage levels. Two identical circuits are used to produce row and column tones, which are then mixed using a low-noise summing amplifier. The oscillator described needs no "startup" time as in other DTMF generators, since the crystal oscillator is running continuously, thus providing a high degree of tone burst accuracy. When there is no tone output signal, the TONE pin assumes a DC level of 2.5 volts (typically). A bandwidth limiting filter is incorporated to attenuate distortion products above 4 kHz.

Burst Mode: Certain telephony applications require that generated DTMF signals be of a specific duration, determined either by the application or by any of the existing exchange transmitter specifications. Standard DTMF signal timing can be accomplished by making use of the burst mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is 51 ms ± 1 ms, a standard interval for autodialer and central office applications. After the burst/pause has been issued, the appropriate bit is set in the status register, indicating that the transmitter is ready for more data.

The timing described above is available when the DTMF mode has been selected. However, when call progress (CP) mode is selected, a secondary burst/pause time is available that extends this interval to 102 ms ± 2 ms. The extended interval is useful when precise tone bursts of longer than 51 ms duration and 51 ms pause are desired. Note that when CP mode and burst mode have been selected, DTMF tones may be transmitted only and *not* received. In applications where a nonstandard burst/pause time is desirable, a software timing loop or external timer can be used to provide the timing pulses when the burst mode is disabled by enabling and disabling the transmitter.

Table 4 Actual Frequencies vs Standard Requirements			
Active cell	Output frequency (Hz)		% error
	Specified	Actual	
L1	697	699.1	+ 0.30
L2	770	766.2	- 0.49
L3	852	847.4	- 0.54
L4	941	948.0	+ 0.74
H1	1209	1215.9	+ 0.57
H2	1336	1331.7	- 0.32
H3	1447	1471.9	- 0.35
H4	1633	1645.0	+ 0.73

Figure 10 Common Crystal Connection

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard 3.579545 MHz television color burst crystal. A number of M-8880 devices can be connected as shown in Figure 10 using only one crystal.

Table 5 Internal Register Functions

RS0	R/$\overline{\text{W}}$	Function
0	0	Write to transmitter
0	1	Read from receiver
1	0	Write to control register
1	1	Read from status register

Table 6 CRA Bit Positions

b3	b2	b1	b0
RSEL	IRQ	CP/$\overline{\text{DTMF}}$	TOUT

Table 7 CRB Bit Positions

b3	g2	b1	b0
C/R	S/D	TEST	BURST

Microprocessor Interface

The M-8880 uses a microprocessor interface that allows precise control of transmitter and receiver functions. Five internal registers are associated with the microprocessor interface, which can be subdivided into three categories: data transfer, transceiver control, and transceiver status. Two registers are associated with data transfer operations. The receive data register, a read-only register, contains the output code of the last valid DTMF tone pair to be decoded. The data entered in the transmit data register determines which tone pair is to be generated (see Table 1). Data can only be written to the transmit data register. Transceiver control is accomplished with two control registers (CRA and CRB) that occupy the same address space. A write operation to CRB can be executed by setting the appropriate bit in CRA. The following write operation to the same address will then be directed to CRB, and subsequent write cycles will then be redirected to CRA. Internal reset circuitry clears the control registers on powerup; however, as a precautionary measure the initialization software should include a routine to clear the registers. Refer to Tables 2 and 3 for details on the control registers. The IRQ/CP pin can be programmed to provide an interrupt request signal on validation of DTMF signals, or when the transmitter is ready for more data (burst mode only). The IRQ/CP pin is configured as an open-drain output device and as such requires a pullup resistor (see Figure 11).

Notes:
R1, R2 = 100KΩ 1%
R3 = 374KΩ 1%
R4 = 3KΩ 10%
RL = 10KΩ (min)
C1 = 100 nF 5%
C2 = 100 nF 5%
C3 = 100 nF 10%*
X1 = 3.579545 MHz

Microprocessor-based systems can inject undesirable noise into the supply rails. M-8880 performance can be optimized by keeping noise on the supply rails to a minimum. The decoupling capacitor (C3) should be connected close to the device and ground loops should be avoided.

Figure 11 Application Circuit (Single-Ended Input)

Table 8 Status Register Description

Bit	Name	Status Flag Set	Status Flag Cleared
b0	IRQ	Interrupt has occurred. Bit one (b1) and/or bit 2 (b2) is set.	Interrupt is inactive. Cleared after status register is read.
b1	Transmit data register empty (burst mode only)	Pause duration has terminated and transmitter is ready for new data.	Cleared after status register is read or when not in burst mode.
b2	Receive data register full	Valid data is in the receive data register.	Cleared after status register is read.
b3	$\overline{\text{Delayed steering}}$	Set on valid detection of the absence of a DTMF signal.	Cleared on detection of a valid DTMF signal.

Table 9 Pin Functions

Name	Description
IN+	Noninverting op-amp input.
IN-	Inverting op-amp input.
GS	Gain select. Gives access to output of front end differential amplifier for connection of feedback resistor.
V_{REF}	Reference voltage output. Nominally $V_{DD}/2$ is used to bias inputs at mid-rail.
V_{SS}	Negative power supply input.
OSC1	DTMF clock/oscillator input.
OSC2	Clock output. A 3.5795 MHz crystaal connected between OSC1 and OSC2 completes the internal oscillator circuit.
TONE	Dual tone multifrequency (DTMF) output.
$R/\overline{W}$	Read/write input. Controls the direction of data transfer to and from the microprocessor and the receiver/transmitter. TTL compatible.
$\overline{CS}$	Chip select. TTL input ($\overline{CS}$ = 0 to select the chip).
RS0	Register select input. See Table 5. TTL compatible.
$\phi 2$	System clock input. May be continuous or strobed only during read or write.TTL compatible.
$\overline{IRQ}$/CP	Interrupt request to microprocessor (open-drain output). Also, when call progress (CP) mode has been selected and interrupt enabled, the $\overline{IRQ}$/CP pin will output a rectangular wave signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the call progress filter. See Figure 9.
D0—D3	Microprocessor data bus. TTL compatible.
ESt	Early steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
St/GT	Steering input/guard time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
V_{DD}	Positive power supply input.

Table 10 Absolute Maximum Ratings

Parameter	Symbol	Value
Power supply voltage (V_{DD} - V_{SS})	V_{DD}	+ 6.0 V max
Voltage on any pin	V_{dc}	V_{SS} -0.3 V to V_{DD} + 0.3 V
Current on any pin	I_{DD}	10 mA max
Operating temperature	T_A	-40 ° C to +85 ° C
Storage temperature	T_S	-65 ° C to +150 ° C
Note: Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.		

Table 11 DC Characteristics

Parameter	Symbol	Min	Typ*	Max	Units
Operating supply voltage	V_{DD}	4.75	5.0	5.25	V
Operating supply current	I_{DD}	—		10	mA
Power consumption	P_O	—		52.5	mW
Inputs					
High-level input voltage, OSC1	V_{IHO}	3.5	—	—	V
Low-level input voltage, OSC1	V_{ILO}	—	—	1.5	V
Input impedance (@ 1 kHz), IN+, IN-	R_{IN}	—	10	—	MΩ
Steering threshold voltage	V_{TSt}	2.2	2.3	2.5	V
Outputs					
High-level output voltage (no load), OSC2	V_{OHO}	4.9	—	—	V
Low-level output voltage (no load), OSC2	V_{OLO}	—	—	0.1	V
Output leakage current (VOH = 2.4V), IRQ	I_{OZ}	—	1.0	10.0	μA
V_{REF} output voltage (no load)	V_{REF}	2.4	—	2.7	V
V_{REF} output resistance	R_{OR}	—		1.0	kΩ
Data Bus					
Low-level input voltage	V_{IL}	—	—	0.8	V
High-level input voltage	V_{IH}	2.0	—	—	V
Low-level output voltage (IOL = 1.6 mA)	V_{OL}	—	—	0.4	V
High-level output voltage (IOH = 400 μA)	V_{OH}	2.4	—	—	V
Input leakage current (VIN = 0.4 to 2.4 V)	I_{IZ}	—	—	10.0	μA

All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0 V ± 5%; f_C = 3.579545 MHz; T_A = -40 °C to +85 °C unless otherwise noted.
*Typical values are for use as design aids only, and are not guaranteed or subject to production testing.

Table 12 Electrical Characteristics —Gain Setting Amplifier

Parameter	Symbol	Min	Typ*	Max	Units
Input leakage current ($V_{SS} ≤ V_{IN} ≤ V_{DD}$)	I_{IN}	—	100	—	nA
Input resistance	R_{IN}	—	10	—	MΩ
Input offset voltage	V_{OS}	—	25	—	mV
Power supply rejection (1 kHz)	PSRR	—	60	—	dB
Common mode rejection (-3.0 V ≤ V_{IN} ≤ 3.0 V)	CMRR	—	60	—	dB
DC open-loop voltage gain	A_{VOL}	—	65	—	dB
Unity gain bandwidth	BW	—	1.5	—	MHz
Output voltage swing (RL ≥ 100 kΩ to V_{SS})	V_O	—	4.5	—	V_{PP}
Maximum capacitive load, GS	C_L	—	100	—	pF
Maximum resistive load, GS	R_L	—	50	—	kΩ
Common mode range (no load)	V_{CM}	—	3.0	—	V_{PP}

All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0 V; V_{SS} = 0 V; T_A = 25 °C
*Typical values are for use as design aids only, and are not guaranteed or subject to production testing.

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Table 13 AC Characteristics					
Parameter	Symbol	Min	Typ*	Max	Units
Receive signal conditions					
Valid input signal levels (each tone of composite signal; Notes 1, 2, 3, 5, 6, 9)		-29 / 27.5	— / —	+1 / 869	dBm / mV$_{RMS}$
Positive twist accept (Notes 2, 3, 6, 9)		—		6	dB
Negative twist accept (Notes 2, 3, 6, 9)		—		6	dB
Frequency deviation accept (Notes 2, 3, 5, 9)		± 1.5% ± 2 Hz	—	—	Nom.
Frequency deviation reject (Notes 2, 3, 5)		± 3.5%	—	—	Nom.
Third tone tolerance (Notes 2, 3, 4, 5, 9, 10)		—	-16	—	dB
Noise tolerance (Notes 2, 3, 4, 5, 7, 9, 10)		—	-12	—	dB
Dial tone tolerance (Notes 2, 3, 4, 5, 8, 9, 11)		—	+22	—	dB
Call progress					
Lower frequency (@ -25 dBm) accept	f_{LA}	—	320	—	Hz
Upper frequency (@ -25 dBm) accept	f_{HA}	—	510	—	Hz
Lower frequency (@ -25 dBm) reject	f_{LR}	—	290	—	Hz
Upper frequency (@ -25 dBm) reject	f_{HR}	—	540	—	Hz
Receive timing					
Tone present detect time	t_{DP}	5	11	14	ms
Tone absent detect time	t_{DA}	0.5	4	8.5	ms
Tone duration accept (ref. Figure 11)	t_{REC}	—	—	40	ms
Tone duration reject (ref. Figure 11)	$\overline{t_{REC}}$	20	—	—	ms
Interdigit pause accept (ref. Figure 11)	t_{ID}	—	—	40	ms
Interdigit pause reject (ref. Figure 11)	t_{DO}	20	—	—	ms
Delay St to b3	t_{PStb3}	—	13	—	µs
Delay St to RX$_0$—RX$_3$	t_{PStRX}	—	8	—	µs
Transmit timing					
Tone burst duration (DTMF mode)	t_{BST}	50	—	52	ms
Tone pause duration (DTMF mode)	t_{PS}	50	—	52	ms
Tone burst duration (extended, call progress mode)	t_{BSTE}	100	—	104	ms
Tone pause duration (extended, call progress mode)	t_{PSE}	100	—	104	ms
Tone output					
High group output level (R$_L$ = 10 kΩ)	V_{HOUT}	-6.1	—	-2.1	dBm
Low group output level (R$_L$ = 10 kΩ)	V_{LOUT}	-8.1	—	-4.1	dBm
Pre-emphasis (R$_L$ = 10 kΩ)	dB_P	0	2	3	dB
Output distortion (R$_L$ = 10 kΩ, 3.4 kHz bandwidth)	THD	—	-25	—	dB
Frequency deviation (f = 3.5795 MHz)	f_D	—	±0.7	±1.5	%
Output load resistance	R_{LT}	10	—	50	kΩ
Microprocessor interface					
φ2 cycle period	t_{CYC}	0.5	—	—	µs
φ2 high pulse width	t_{CH}	200	—	—	ns
φ2 low pulse width	t_{CL}	180	—	—	ns
φ2 rise and fall time	t_R, t_F	—	—	25	ns
Address, R/$\overline{W}$ hold time	t_{AH}, t_{RWH}	10	—	—	ns
Address, R/$\overline{W}$ setup time (prior to φ2)	t_{AS}, t_{RWS}	23	—	—	ns
Data hold time (read)	t_{DHR}	22	—	—	ns

Table 13 AC Characteristics (concluded)					
Parameter	Symbol	Min	Typ*	Max	Units
Microprocessor interface (continued)					
$\phi 2$ to valid data delay (read) (200 pF load)	t_{DDR}	—	—	150	ns
Data setup time (write)	t_{DSW}	45	—	—	ns
Data hold time (write)	t_{DHW}	10	—	—	ns
Input capacitance, D0—D3	C_{IN}	—	5	—	pF
Output capacitance, $\overline{IRQ}$/CP	$C/_{OUT}$	—	5	—	pF
DTMF clock					
Crystal clock frequency	f_C	3.5759	3.5795	3.5831	MHz
Clock input rise time (external clock)	t_{LHCL}	—	—	110	ns
Clock input fall time (external clock)	t_{HLCL}	—	—	110	ns
Clock input duty cycle (external clock)	DC_{CL}	40	50	60	%
Capacitive load, OSC2	C_{LO}	—	—	30	pF

All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0 V ± 5%; V_{SS} = 0 V; f_C = 3.579545 MHz; T_A = -40 °C to +85 °C

*Typical values are for use as design aids only, and are not guaranteed or subject to production testing.

Notes:
1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 ms. Tone pause = 40 ms.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. The tone pair is deviated by ± 1.5% ± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are 350 and 440 Hz (± 2%).
9. For an error rate of less than 1 in 10,000.
10. Referenced to the lowest amplitude tone in the DTMF signal.
11. Referenced to the minimum valid accept level.

M-8888 DTMF TRANSCEIVER

The Teltone® M-8888 is a complete DTMF Transmitter/Receiver that features adjustable guard time, automatic tone burst mode, call progress mode, and a fully compatible 8051, 8086/8 microprocessor interface. The receiver portion is based on the industry standard M-8870 DTMF Receiver, while the transmitter uses a switched-capacitor digital-to-analog converter for low-distortion, highly accurate DTMF signaling. Tone bursts can be transmitted with precise timing by making use of the automatic tone burst mode. To analyze call progress tones, a call progress filter can be selected by an external microprocessor.

Features

- Advanced CMOS technology for low power consumption and increased noise immunity
- Complete DTMF transmitter/receiver in a single chip
- Standard 8051, 8086/8 microprocessor port
- Central office quality and performance
- Adjustable guard time
- Automatic tone burst mode
- Call progress mode
- Single +5 Volt power supply
- 20-pin DIP
- 2-MHz microprocessor port operation

Applications

- Paging systems
- Repeater systems/mobile radio
- Interconnect dialers
- PBX systems
- Computer systems
- Fax machines
- Pay telephones
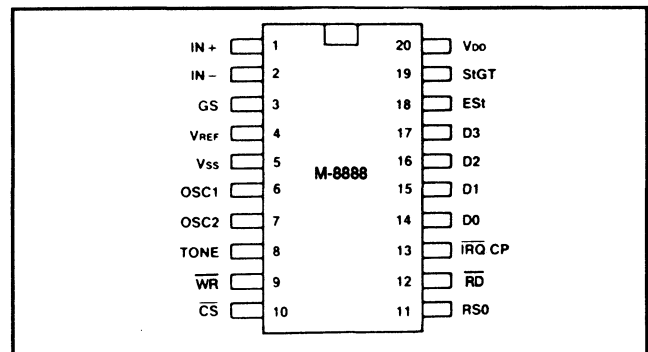- Credit card verification
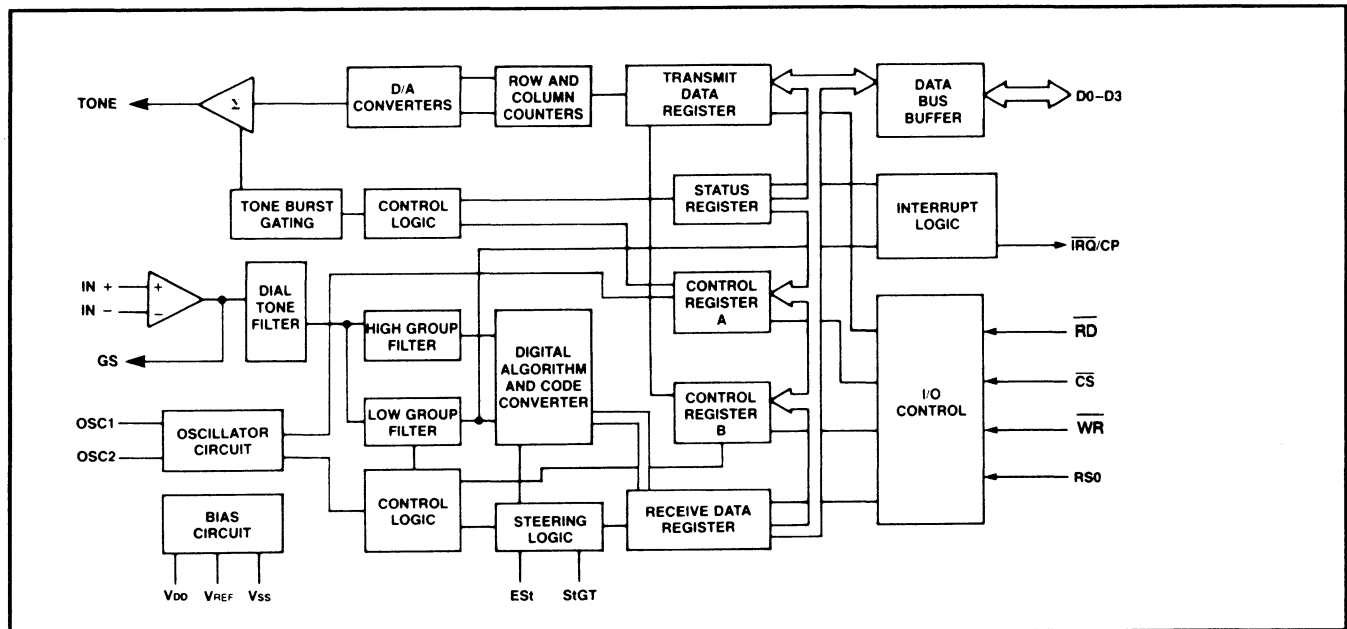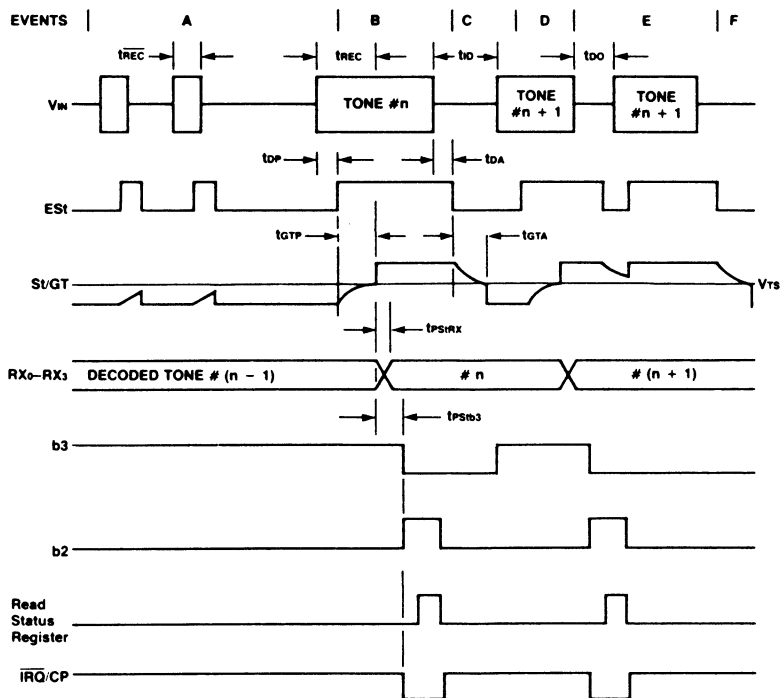

Figure 1 Pin Connections

Figure 2 Block Diagram

A. General Transceiver Timing

Explanation of Events

A	Tone bursts detected, tone duration invalid, RX data register not updated.
B	Tone #n detected, tone duration valid, tone decoded and latched in RX data register.
C	End of tone #n detected, tone absent duration valid, information in RX data register retained until next valid tone pair.
D	Tone #n + 1 detected, tone duration valid, tone decoded and latched in RX data register.
E	Acceptable dropout of tone #n + 1, tone absent duration invalid, data remains unchanged.
F	End of tone #n + 1 detected, tone absent duration valid, information in RX data register retained until next valid tone pair.

Explanation of Symbols

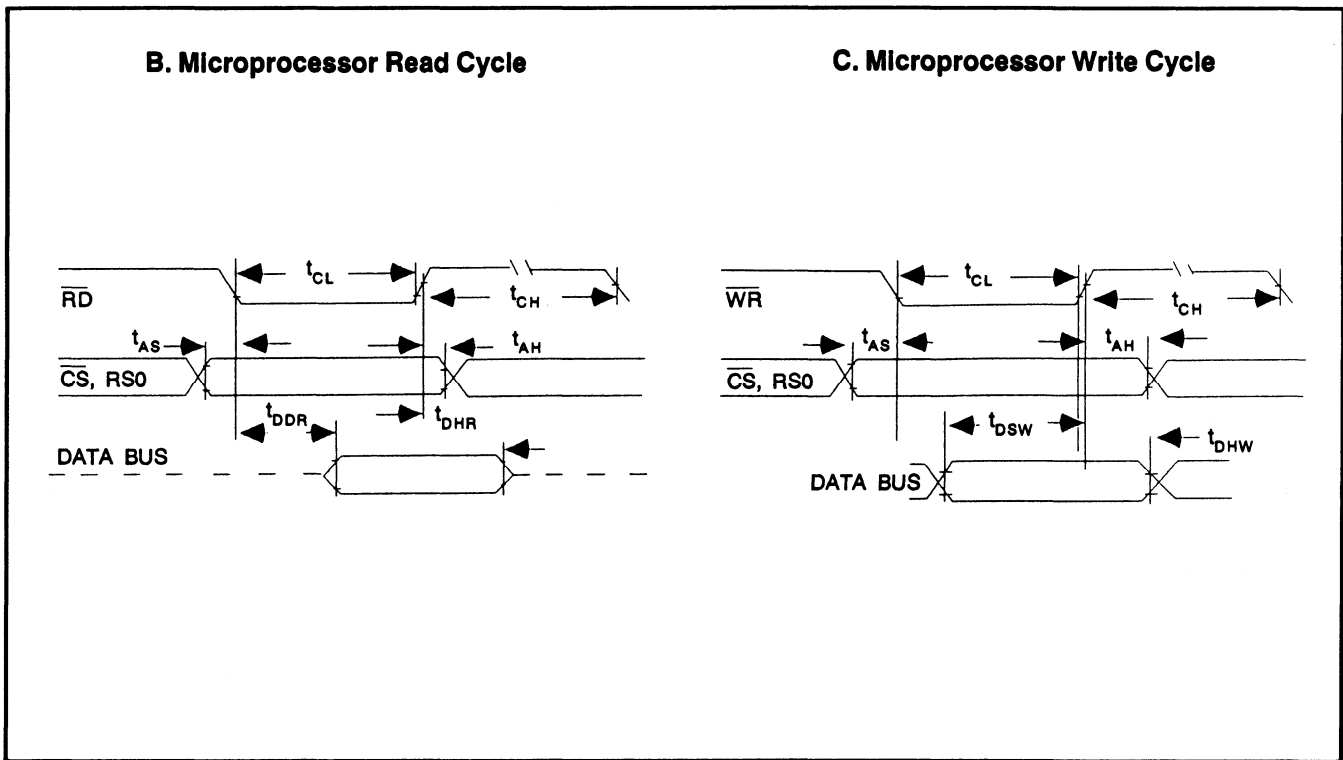|	
V_{IN}	DTMF composite input signal.
ESt	Early steering output. Indicates detection of valid tone frequencies.
St/GT	Steering input/guard time output. Drives external RC timing circuit.
RX_0-RX_3	4-bit decoded data in receive data register.
b_3	Delayed steering. Indicates that valid frequencies have been present/absent for the required guard time thus constituting a valid signal. Active low for the duration of a valid DTMF signal.
$\overline{b_2}$	Indicates that valid data is in the receive data register. The bit is cleared after the status register is read.
$\overline{IRQ}$/CP	Interrupt is active indicating that new data is in the RX data register. The interrupt is cleared after the status register is read.
$t_{\overline{REC}}$	Maximum DTMF signal duration not detected as valid.
t_{REC}	Minimum DTMF signal duration required for valid recognition.
t_{ID}	Minimum time between valid sequential DTMF signals.
t_{DO}	Maximum allowable dropout during valid DTMF signal.
t_{DP}	Time to detect valid frequencies present.
t_{DA}	Time to detect valid frequencies absent.
t_{GTP}	Guard time, tone present.
t_{GTA}	Guard time, tone absent.

Figure 3 Timing Diagrams

B. Microprocessor Read Cycle

C. Microprocessor Write Cycle

Figure 3 Timing Diagrams (concluded)

A. Test load for D0—D3 pins
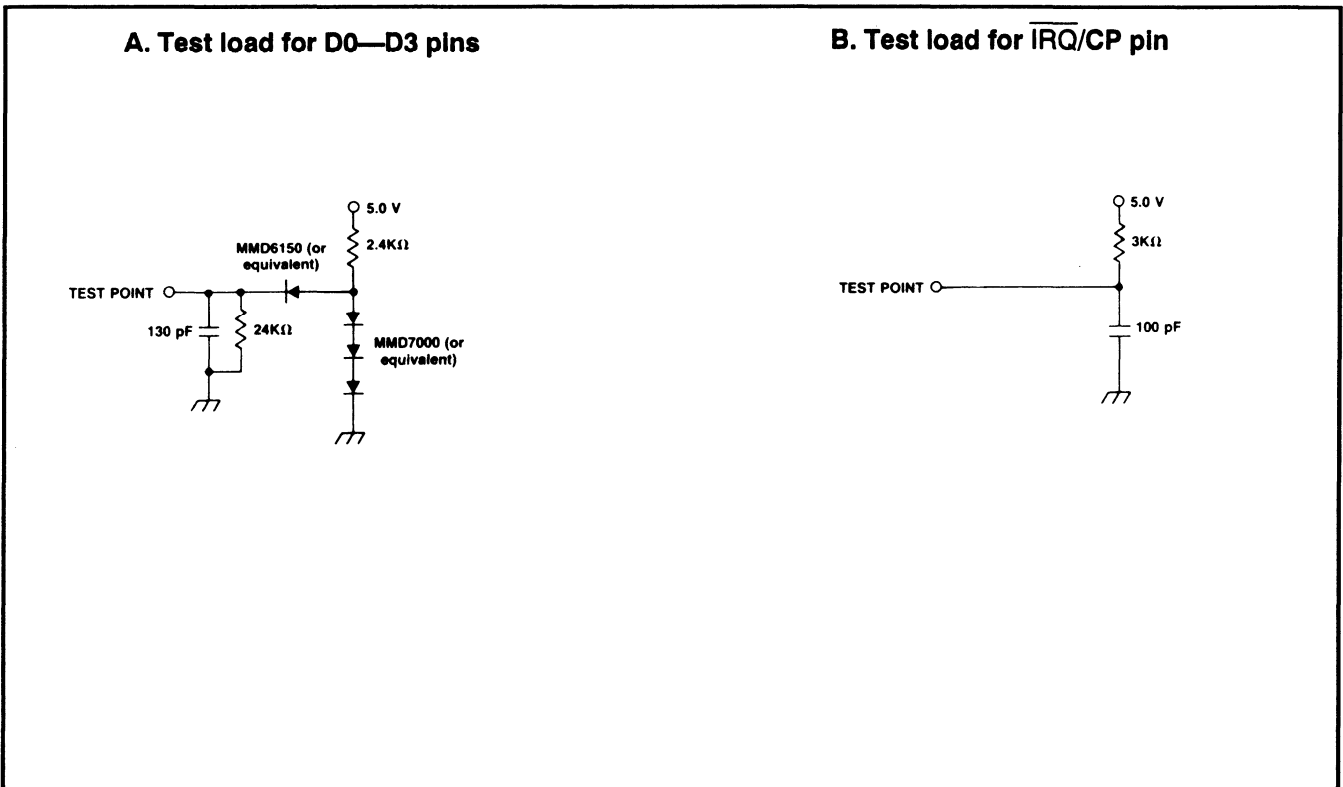
B. Test load for IRQ/CP pin

Figure 4 Test Loads

FUNCTIONAL DESCRIPTION

M-8888 functions consist of a high-performance DTMF receiver with an internal gain setting amplifier and a DTMF generator that contains a tone burst counter for generating precise tone bursts and pauses. The call progress mode, when selected, allows the detection of call progress tones. A standard 8051, 8086/8 series microprocessor interface allows access to an internal status register, two control registers, and two data registers.

Input Configuration

The input arrangement consists of a differential input operational amplifier and bias sources (V_{REF}) for biasing the amplifier inputs at $V_{DD}/2$. Provisions are made for the connection of a feedback resistor to the op-amp output (GS) for gain adjustment. In a single-ended configuration, the input pins should be connected as shown in Figure 5. Figure 6 shows the necessary connections for a differential input configuration.
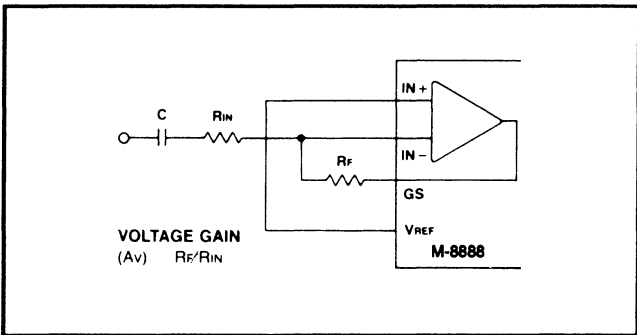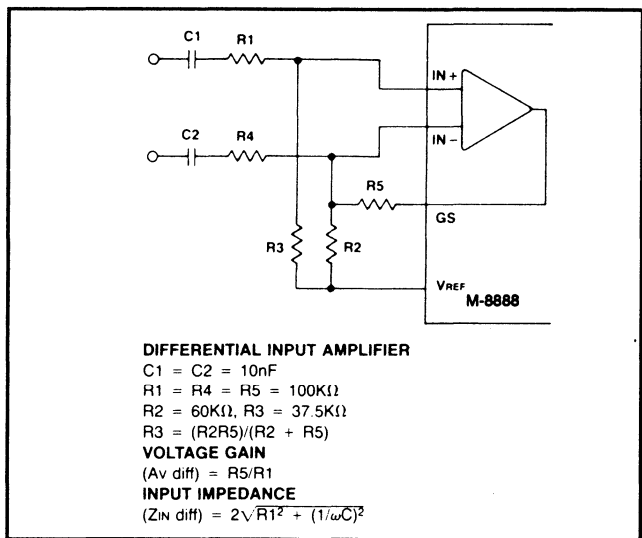
Figure 5 Single-Ended Input Configuration

Receiver Section

The low and high group tones are separated by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters with bandwidths that correspond to the low and high group frequencies listed in Table 1. The low group filter incorporates notches at 350 and 440 Hz, providing excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor filter that smooths the signals prior to limiting. Limiting is performed by high-gain comparators with hysteresis to prevent detection of unwanted low-level signals. The comparator outputs provide full-rail logic swings at the incoming DTMF signal frequencies.

A decoder employs digital counting techniques to determine the frequencies of the incoming tones, and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals (such as voice), while tolerating small deviations in frequency. The algorithm provides an optimum combination of immunity to talkoff with tolerance to interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (referred to as "signal condition"), the early steering (ESt) output goes to an active

Figure 6 Differential Input Configuration

Table 1 Tone Encoding/Decoding						
F_{LOW}	F_{HIGH}	DIGIT	D3	D2	D1	D0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0
0 = logic low, 1 = logic high						

state. Any subsequent loss of signal condition will cause ESt to assume an inactive state.

Steering Circuit: Before a decoded tone pair is registered, the receiver checks for a valid signal duration (referred to as "character recognition condition"). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes V_C (see Figure 7) to rise as the capacitor discharges. Provided that the signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the receive data register.
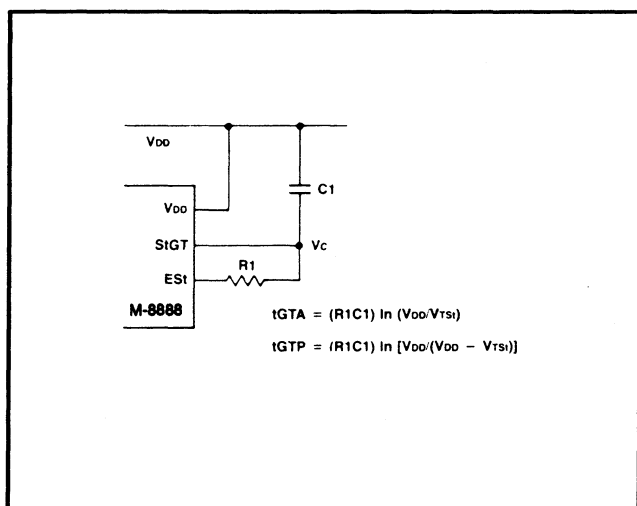
Figure 7 Basic Steering Circuit

$$tGTA = (R1C1) \ln (V_{DD}/V_{TSt})$$

$$tGTP = (R1C1) \ln [V_{DD}/(V_{DD} - V_{TSt})]$$

At this point the GT output is activated and drives V_C to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag goes high, signaling that a received tone pair has been registered. It is possible to monitor the status of the delayed steering flag by checking the appropriate bit in the status register. If interrupt mode has been selected, the IRQ/CP pin will pull low when the delayed steering flag is active.

The contents of the output latch are updated on an active delayed steering transition. This data is presented to the 4-bit bidirectional data bus when the receive data register is read. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropout) too short to be considered a valid pause. This capability, together with the ability to select the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment: The simple steering circuit shown in Figure 7 is adequate for most applications. Component values are chosen according to the formula:

$$tREC = tDP + tGTP$$

$$TID = tDA + tGTA$$

The value of tDP is a device parameter and $tREC$ is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μF is recommended for most applications, leaving R to be selected by the designer. Different steering arrangements may be used to select independently the guard times for tone present ($tGTP$) and tone absent ($tGTA$). This may be necessary to meet system specifications that place both accept and reject limits on both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameters such as talkoff and noise immunity. Increasing $tREC$ improves talkoff performance since it reduces the probability that tones simulated by speech will

Figure 8 Guard Time Adjustment

Figure 9 Call Progress Response

maintain signal condition long enough to be registered. Alternatively, a relatively short $tREC$ with a long tDO would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone dropouts are required. Design information for guard time adjustment is shown in Figure 8.

Call Progress Filter

A call progress (CP) mode can be selected, allowing the detection of various tones that identify the progress of a telephone call on the network. The call progress tone input and DTMF input are common; however, call progress tones can only be detected when the CP mode has been selected. DTMF signals cannot be detected if the CP mode has been selected (see Table 2). Figure 9 indicates the useful detect bandwidth of the call progress filter. Frequencies presented to the input (IN+ and IN-) that are within the "accept" bandwidth limits of the filter are hard-limited by a high-gain

Table 2 Control Register A Description

Bit	Name	Function	Description
b0	TOUT	Tone output	A logic 1 enables the tone output. This function can be implemented in either the burst mode or nonburst mode.
b1	CP/$\overline{DTMF}$	Mode control	In DTMF mode (logic 0), the device is capable of generating and receiving DTMF signals. When the call progress (CP) mode is selected (logic 1), a 6th-order bandpass filter is enabled to allow call progress tones to be detected. Call progress tones within the specified bandwidth will be presented at the $\overline{IRQ}$/CP pin in rectangular wave format if the IRQ bit has been enabled (b2 = 1). Also, when the CP mode and burst mode have both been selected, the transmitter will issue DTMF signals with a burst and pause of 102 ms (typ) duration. This signal duration is twice that obtained from the DTMF transmitter, if DTMF mode had been selected. Note that DTMF signals cannot be decoded when the CP mode has been selected.
b2	IRQ	Interrupt enable	A logic 1 enables the interrupt mode. When this mode is active and the DTMF mode has been selected (b1 = 0), the $\overline{IRQ}$/CP pin will pull to a logic 0 condition when either (1) a valid DTMF signal has been received and has been present for the guard time or (2) the transmitter is ready for more data (burst mode only).
b3	RSEL	Register select	A logic 1 selects control register B on the next write cycle to the control register address. Subsequent write cycles to the control register are directed back to control register A.

Table 3 Control Register B Description

Bit	Name	Function	Description
b0	BURST	Burst mode	A logic 0 enables the burst mode. When this mode is selected, data corresponding to the desired DTMF tone pair can be written to the transmit data register, resulting in a tone burst of a specific duration (see Table 13). Subsequently, a pause of the same duration is induced. Immediately following the pause, the status register is updated indicating that the transmit data register is ready for further instructions, and an interrupt will be gneerated if the interrupt mode has been enabled. Additionally, if call progress (CP) mode has been enabled, the burst and pause duration is increased by a factor of two. When the burst mode is not selected (logic 1), tone bursts of any desired duration may be generated.
b1	TEST	Test mode	By enabling the test mode (logic 1), the $\overline{IRQ}$/CP pin will present the delayed steering (inverted) signal from the DTMF receiver. Refer to Figure 3A (b3 waveform) for details concerning the output waveform. DTMF mode must be selected (CRA b1 = 0) before test mode can be implemented.
b2	S/$\overline{D}$	Single/dual tone generation	A logic 0 will allow DTMF signals to be produced. If single-tone generation is enabled (logic 1), either now or column tones (low or high group) can be generated depending on the state of b3 in control register B.
b3	C/$\overline{R}$	Column/row tones	When used in conjunction with b2 (above), the transmitter can be made to generate single-row or single-column frequencies. A logic 0 will select row frequencies and a logic 1 will select column frequencies.

comparator with the $\overline{IRQ}$/CP pin serving as the output. The square wave output obtained from the schmitt trigger can be analyzed by a microprocessor or counter arrangement to determine the nature of the call progress tone being detected. Frequencies in the "reject" area will not be detected, and consequently there will be no activity on IRQ/CP as a result of these frequencies.

DTMF Generator

The DTMF transmitter used in the M-8888 is capable of generating all 16 standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.58 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor digital-to-analog converters. The row and column tones are mixed and filtered, providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal, data conforming to the encoding format shown in Table 1 must be written to the transmit data register. Note that this is the same as the receiver output code. The individual tones that are generated (f_{LOW} and f_{HIGH}) are referred to as low-group and high-group tones. Typically, the high-group to low-group amplitude ratio (twist) is 2 dB to compensate for high-group attenuation on long loops.

Operation: During write operations to the transmit data register, 4-bit data on the bus is latched and converted to a 2 of 8 code for use by the programmable divider circuitry to

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$$THD(\%) = 100 \frac{\sqrt{V^2_{2f} + V^2_{3f} + V^2_{4f} + ...V^2_{nf}}}{V_{fundamental}}$$

Equation 1. THD(%) for a Single Tone

$$THD(\%) = 100 \frac{\sqrt{V^2_{2L} + V^3_{3L} + ...V^2_{nL} + V^2_{2H} + V^2_{3H} + ...V^2_{nH} + V^2_{IMD}}}{\sqrt{V^2_L + V^2_H}}$$

Equation 2. THD(%) for a Dual Tone

specify a time segment length that will ultimately determine the tone frequency. The number of time segments is fixed at 32, but the frequency is varied by varying the segment length. When the divider reaches the appropriate count as determined by the input code, a reset pulse is issued and the counter starts again. The divider output clocks another counter that addresses the sinewave lookup ROM. The lookup table contains codes used by the switched capacitor D/A converter to obtain discrete and highly accurate DC voltage levels. Two identical circuits are used to produce row and column tones, which are then mixed using a low-noise summing amplifier. The oscillator described needs no "startup" time as in other DTMF generators, since the crystal oscillator is running continuously, thus providing a high degree of tone burst accuracy. When there is no tone output signal, the TONE pin assumes a DC level of 2.5 volts (typically). A bandwidth limiting filter is incorporated to attenuate distortion products above 4 kHz.

Burst Mode: Certain telephony applications require that generated DTMF signals be of a specific duration, determined either by the application or by any of the existing exchange transmitter specifications. Standard DTMF signal timing can be accomplished by making use of the burst mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is 51 ms ± 1 ms, a standard interval for autodialer and central office applications. After the burst/pause has been issued, the appropriate bit is set in the status register, indicating that the transmitter is ready for more data.

The timing described above is available when the DTMF mode has been selected. However, when call progress (CP) mode is selected, a secondary burst/pause time is available that extends this interval to 102 ms ± 2 ms. The extended interval is useful when precise tone bursts of longer than 51 ms duration and 51 ms pause are desired. Note that when CP mode and burst mode have been selected, DTMF tones may be transmitted only and *not* received. In applications where a nonstandard burst/pause time is desirable, a software timing loop or external timer can be used to provide the timing pulses when the burst mode is disabled by enabling and disabling the transmitter.

The M-8888 is initialized on powerup sequence with DTMF mode and burst mode selected.

Single-Tone Generation: A single-tone mode is available whereby individual tones from the low group or high group can be generated. This mode can be used for DTMF test equipment applications, acknowledgement tone generation, and distortion measurements. Refer to Table 3 for details.

Distortion Calculations: The M-8888 is capable of producing precise tone bursts with minimal error in frequency (see Table 4). The internal summing amplifier is followed by a first-order low-pass switched capacitor filter to minimize harmonic components and intermodulation products. The total harmonic distortion for a *single* tone can be calculated using Equation 1, which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage. The Fourier components of the tone output correspond to V2f... Vnf as measured on the output waveform. The total harmonic distortion for a *dual* tone can be calculated using Equation 2.

V_L and V_H correspond to the low-group and high-group amplitude, respectively, and V^2_{IMD} is the sum of all the intermodulation components. The internal switched capacitor filter following the D/A converter keeps distortion products down to a very low level.

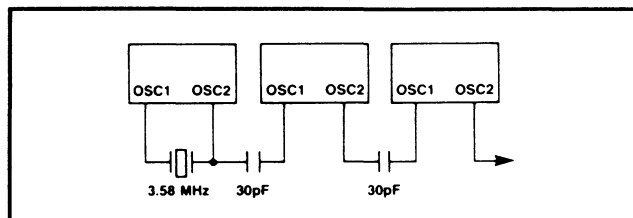| Table 4 Actual Frequencies vs Standard Requirements			
Active cell	Output frequency (Hz)		% error
	Specified	Actual	
L1	697	699.1	+ 0.30
L2	770	766.2	- 0.49
L3	852	847.4	- 0.54
L4	941	948.0	+ 0.74
H1	1209	1215.9	+ 0.57
H2	1336	1331.7	- 0.32
H3	1447	1471.9	- 0.35
H4	1633	1645.0	+ 0.73

Figure 10 Common Crystal Connection

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard 3.579545 MHz television color burst crystal. A number of M-8888 devices can be connected as shown in Figure 10 using only one crystal.

Table 5 Internal Register Functions

RS0	$\overline{RD}$	$\overline{WR}$	Function
0	1	0	Write to transmitter
0	0	1	Read from receiver
1	1	0	Write to control register
1	0	1	Read from status register

Table 6 CRA Bit Positions

b3	b2	b1	b0
RSEL	IRQ	CP/$\overline{DTMF}$	TOUT

Table 7 CRB Bit Positions

b3	b2	b1	b0
C/R	S/D	TEST	BURST

Microprocessor Interface

The M-8888 uses a microprocessor interface that allows precise control of transmitter and receiver functions. Five internal registers are associated with the microprocessor interface, which can be subdivided into three categories: data transfer, transceiver control, and transceiver status. Two registers are associated with data transfer operations. The receive data register, a read-only register, contains the output code of the last valid DTMF tone pair to be decoded. The data entered in the transmit data register determines which tone pair is to be generated (see Table 1). Data can only be written to the transmit data register. Transceiver control is accomplished with two control registers (CRA and CRB) that occupy the same address space. A write operation to CRB can be executed by setting the appropriate bit in CRA. The following write operation to the same address will then be directed to CRB, and subsequent write cycles will then be redirected to CRA. Internal reset circuitry clears the control registers on powerup; however, as a precautionary measure the initialization software should include a routine to clear the registers. Refer to Tables 2 and 3 for details on the control registers. The IRQ/CP pin can be programmed to provide an interrupt request signal on validation of DTMF signals, or when the transmitter is ready for more data (burst mode only). The IRQ/CP pin is configured as an open-drain output device and as such requires a pullup resistor (see Figure 11).

Notes:
R1, R2 = 100KΩ 1%
R3 = 374KΩ 1%
R4 = 3KΩ 10%
RL = 10KΩ (min)
C1 = 100 nF 5%
C2 = 100 nF 5%
C3 = 100 nF 10%*
X1 = 3.579545 MHz

Microprocessor-based systems can inject undesirable noise into the supply rails. M-8888 performance can be optimized by keeping noise on the supply rails to a minimum. The decoupling capacitor (C3) should be connected close to the device and ground loops should be avoided.
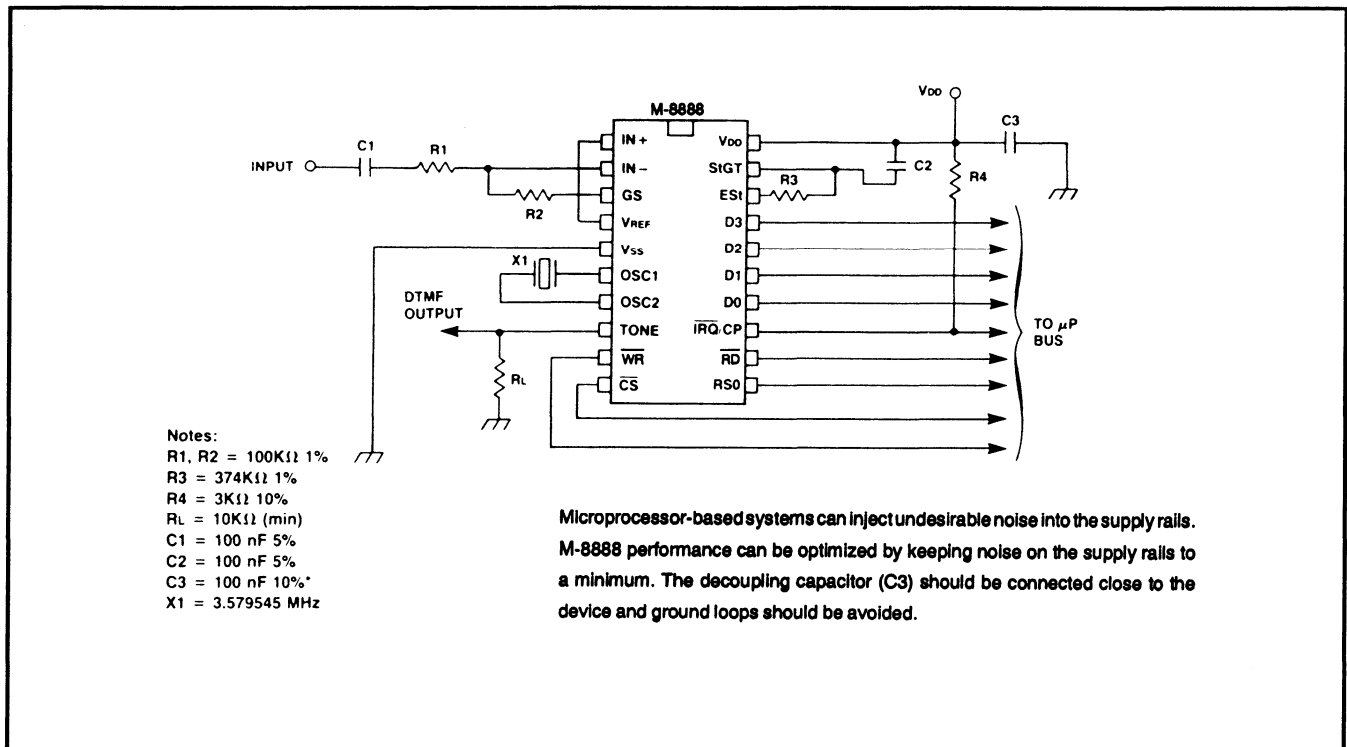
Figure 11 Application Circuit (Single-Ended Input)

Table 8 Status Register Description

Bit	Name	Status Flag Set	Status Flag Cleared
b0	IRQ	Interrupt has occurred. Bit one (b1) and/or bit 2 (b2) is set.	Interrupt is inactive. Cleared after status register is read.
b1	Transmit data register empty (burst mode only)	Pause duration has terminated and transmitter is ready for new data.	Cleared after status register is read or when not in burst mode.
b2	Receive data register full	Valid data is in the receive data register.	Cleared after status register is read.
b3	$\overline{\text{Delayed steering}}$	Set on valid detection of the absence of a DTMF signal.	Cleared on detection of a valid DTMF signal.

Table 9 Pin Functions

Name	Description
IN+	Noninverting op-amp input.
IN-	Inverting op-amp input.
GS	Gain select. Gives access to output of front end differential amplifier for connection of feedback resistor.
V_{REF}	Reference voltage output. Nominally $V_{DD}/2$ is used to bias inputs at mid-rail. (See Figure 11.)
V_{SS}	Negative power supply input.
OSC1	DTMF clock/oscillator input.
OSC2	Clock output. A 3.5795 MHz crystaal connected between OSC1 and OSC2 completes the internal oscillator circuit.
TONE	Dual tone multifrequency (DTMF) output.
$\overline{\text{WR}}$	Write input. A low on this pin when $\overline{\text{CS}}$ is low enables data transfer from the microprocessor. TTL compatible.
$\overline{\text{CS}}$	Chip select. TTL input ($\overline{\text{CS}}$ = 0 to select the chip).
RS0	Register select input. See Table 5. TTL compatible.
$\overline{\text{RD}}$	Read input. A low on this pin when $\overline{\text{CS}}$ is low enables data transfer to the microprocessor. TTL compatible..
$\overline{\text{IRQ}}$/CP	Interrupt request to microprocessor (open-drain output). Also, when call progress (CP) mode has been selected and interrupt enabled, the $\overline{\text{IRQ}}$/CP pin will output a rectangular wave signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the call progress filter. See Figure 9.
D0—D3	Microprocessor data bus. TTL compatible.
ESt	Early steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
St/GT	Steering input/guard time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
V_{DD}	Positive power supply input.

The $\overline{\text{IRQ}}$/CP pin is configured as an open-drain output device and as such requires a pullup resistor (see Figure 11).

Table 10 Absolute Maximum Ratings

Parameter	Symbol	Value
Power supply voltage (V_{DD} - V_{SS})	V_{DD}	+ 6.0 V max
Voltage on any pin	V_{dc}	V_{SS} -0.3 V to V_{DD} + 0.3 V
Current on any pin	I_{DD}	10 mA max
Operating temperature	T_A	-40 ° C to +85 ° C
Storage temperature	T_S	-65 ° C to +150 ° C
Note: Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.		

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Table 11 DC Characteristics					
Parameter	Symbol	Min	Typ*	Max	Units
Operating supply voltage	V_{DD}	4.75	5.0	5.25	V
Operating supply current	I_{DD}	—	—	10	mA
Power consumption	P_O	—		52.5	mW
Inputs					
High-level input voltage, OSC1	V_{IHO}	3.5	—	—	V
Low-level input voltage, OSC1	V_{ILO}	—	—	1.5	V
Input impedance (@ 1 kHz), IN+, IN-	R_{IN}	—	10	—	MΩ
Steering threshold voltage	V_{TSt}	2.2	2.3	2.5	V
Outputs					
High-level output voltage (no load), OSC2	V_{OHO}	4.9	—	—	V
Low-level output voltage (no load), OSC2	V_{OLO}	—	—	0.1	V
Output leakage current (VOH = 2.4V), IRQ	I_{OZ}	—	1.0	10.0	µA
V_{REF} output voltage (no load)	V_{REF}	2.4	—	2.7	V
V_{REF} output resistance	R_{OR}	—	—	1	kΩ
Data Bus (D0-D3, $\overline{RD}$, $\overline{WR}$, $\overline{RSO}$, $\overline{CS}$)					
Low-level input voltage	V_{IL}	—	—	0.8	V
High-level input voltage	V_{IH}	2.0	—	—	V
Low-level output voltage (IOL = 1.6 mA)	V_{OL}	—	—	0.4	V
High-level output voltage (IOH = 400 µA)	V_{OH}	2.4	—	—	V
Input leakage current (VIN = 0.4 to 2.4 V)	I_{IZ}	—	—	10.0	µA

All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0 V ± 5%; f_C = 3.579545 MHz; T_A = -40 °C to +85 °C unless otherwise noted.
*Typical values are for use as design aids only, and are not guaranteed or subject to production testing.

Table 12 Electrical Characteristics —Gain Setting Amplifier					
Parameter	Symbol	Min	Typ*	Max	Units
Input leakage current (V_{SS} ≤ V_{IN} ≤ V_{DD})	I_{IN}	—	100	—	nA
Input resistance	R_{IN}	—	10	—	MΩ
Input offset voltage	V_{OS}	—	25	—	mV
Power supply rejection (1 kHz)	PSRR	—	60	—	dB
Common mode rejection (-3.0 V ≤ V_{IN} ≤ 3.0 V)	CMRR	—	60	—	dB
DC open-loop voltage gain	A_{VOL}	—	65	—	dB
Unity gain bandwidth	BW	—	1.5	—	MHz
Output voltage swing (RL ≥ 100 kΩ to V_{SS})	V_O	—	4.5	—	V_{PP}
Maximum capacitive load, GS	C_L	—	100	—	pF
Maximum resistive load, GS	R_L	—	50	—	kΩ
Common mode range (no load)	V_{CM}	—	3.0	—	V_{PP}

All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0 V; V_{SS} = 0 V; T_A = 25 °C
*Typical values are for use as design aids only, and are not guaranteed or subject to production testing.

Table 13 AC Characteristics

Parameter	Symbol	Min	Typ*	Max	Units
Receive signal conditions					
Valid input signal levels (each tone of composite signal; Notes 1, 2, 3, 5, 6, 9)		-29 27.5	— —	+1 869	dBm mV$_{RMS}$
Positive twist accept (Notes 2, 3, 6, 9)		—	—	6	dB
Negative twist accept (Notes 2, 3, 6, 9)		—	—	6	dB
Frequency deviation accept (Notes 2, 3, 5, 9)		± 1.5% ± 2 Hz	—	—	Nom.
Frequency deviation reject (Notes 2, 3, 5)		± 3.5%	—	—	Nom.
Third tone tolerance (Notes 2, 3, 4, 5, 9, 10)		—	-16	—	dB
Noise tolerance (Notes 2, 3, 4, 5, 7, 9, 10)		—	-12	—	dB
Dial tone tolerance (Notes 2, 3, 4, 5, 8, 9, 11)		—	+22	—	dB
Call progress					
Lower frequency (@ -25 dBm) accept	f_{LA}	—	320	—	Hz
Upper frequency (@ -25 dBm) accept	f_{HA}	—	510	—	Hz
Lower frequency (@ -25 dBm) reject	f_{LR}	—	290	—	Hz
Upper frequency (@ -25 dBm) reject	f_{HR}	—	540	—	Hz
Receive timing					
Tone present detect time	t_{DP}	5	11	14	ms
Tone absent detect time	t_{DA}	0.5	4	8.5	ms
Tone duration accept (ref. Figure 11)	t_{REC}	—	—	40	ms
Tone duration reject (ref. Figure 11)	$\overline{t_{REC}}$	20	—	—	ms
Interdigit pause accept (ref. Figure 11)	t_{ID}	—	—	40	ms
Interdigit pause reject (ref. Figure 11)	t_{DO}	20	—	—	ms
Delay St to b3	t_{PStb3}	—	13	—	µs
Delay St to RX$_O$—RX$_3$	t_{PStRX}	—	8	—	µs
Transmit timing					
Tone burst duration (DTMF mode)	t_{BST}	50	—	52	ms
Tone pause duration (DTMF mode)	t_{PS}	50	—	52	ms
Tone burst duration (extended, call progress mode)	t_{BSTE}	100	—	104	ms
Tone pause duration (extended, call progress mode)	t_{PSE}	100	—	104	ms
Tone output					
High group output level (R$_L$ = 10 kΩ)	V_{HOUT}	-6.1		-2.1	dBm
Low group output level (R$_L$ = 10 kΩ)	V_{LOUT}	-8.1		-4.1	dBm
Pre-emphasis (R$_L$ = 10 kΩ)	dB_P	0	2	3	dB
Output distortion (R$_L$ = 10 kΩ, 3.4 kHz bandwidth)	THD	—	-25	—	dB
Frequency deviation (f = 3.5795 MHz)	f_D	—	±0.7	±1.5	%
Output load resistance	R_{LT}	10	—	50	kΩ
Microprocessor interface					
RD, WR low pulse width	t_{CL}	200	—	—	
RD, WR high pulse width	t_{CH}	180	—	—	ns
RD, WR rise and fall time	t_R, t_F	—	—	25	ns
Address hold time	t_{AH}	10	—	—	ns
Address setup time	t_{AS}	23	—	—	ns
Data hold time (read)	t_{DHR}	22	—	—	ns
RD to valid data delay (200 pF load)	t_{DDR}	—	—	150	ns

Table 13 AC Characteristics (concluded)					
Parameter	**Symbol**	**Min**	**Typ***	**Max**	**Units**
Microprocessor interface (continued)					
Data setup time (write)	t_{DSW}	45	—	—	ns
Data hold time (write)	t_{DHW}	10	—	—	ns
Input capacitance, D0—D3	C_{IN}	—	5	—	pF
Output capacitance, $\overline{IRQ}$/CP	C/$_{OUT}$	—	5	—	pF
DTMF clock					
Crystal clock frequency	f_C	3.5759	3.5795	3.5831	MHz
Clock input rise time (external clock)	t_{LHCL}	—	—	110	ns
Clock input fall time (external clock)	t_{HLCL}	—	—	110	ns
Clock input duty cycle (external clock)	DC_{CL}	40	50	60	%
Capacitive load, OSC2	C_{LO}	—	—	30	pF

All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0 V ± 5%; V_{SS} = 0 V; f_C = 3.579545 MHz; T_A = -40 °C to +85 °C

*Typical values are for use as design aids only, and are not guaranteed or subject to production testing.

Notes:
1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 ms. Tone pause = 40 ms.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. The tone pair is deviated by ± 1.5% ± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are 350 and 440 Hz (± 2%).
9. For an error rate of less than 1 in 10,000.
10. Referenced to the lowest amplitude tone in the DTMF signal.
11. Referenced to the minimum valid accept level.

Call Progress Tone Receivers and Transmitters

M-980 CALL PROGRESS TONE DETECTOR

The Teltone® M-980 is an integrated circuit tone detector for general purpose use in automatic following of switched telephone calls. The circuit uses low-power CMOS techniques to provide the complete filtering and control required for this function. The basic timing of the M-980 is designed to permit operation with almost any progress tone system.

The use of integrated circuit techniques allows the M-980 to pack the complete frequency and amplitude portion of call progress following into a single 8-pin DIP. A 3.58 MHz crystal-controlled time base guarantees accuracy and repeatability.

Features

- Covers the 340 to 640 Hz range (common call progress)
- Sensitivity to -38 dBm
- Dynamic range over 36 dB
- 40 ms minimum detect (50 ms to output)
- 8-pin DIP
- Single supply CMOS (low power)
- Supply range 4.5 to 5.5 VDC
- Inexpensive 3.58-MHz time base

Applications

- Automatic dialers
- Dialing modems
- Traffic measurement equipment
- Test equipment
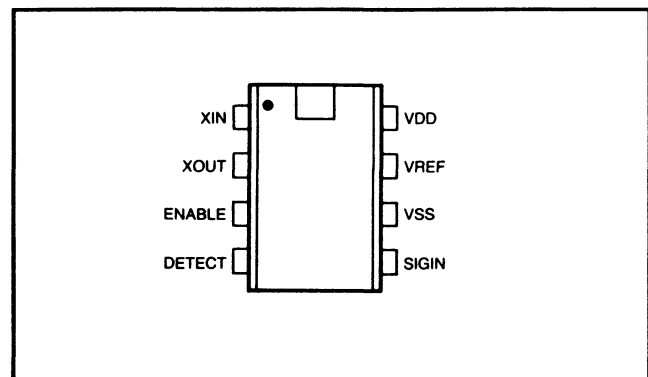- Service evaluation
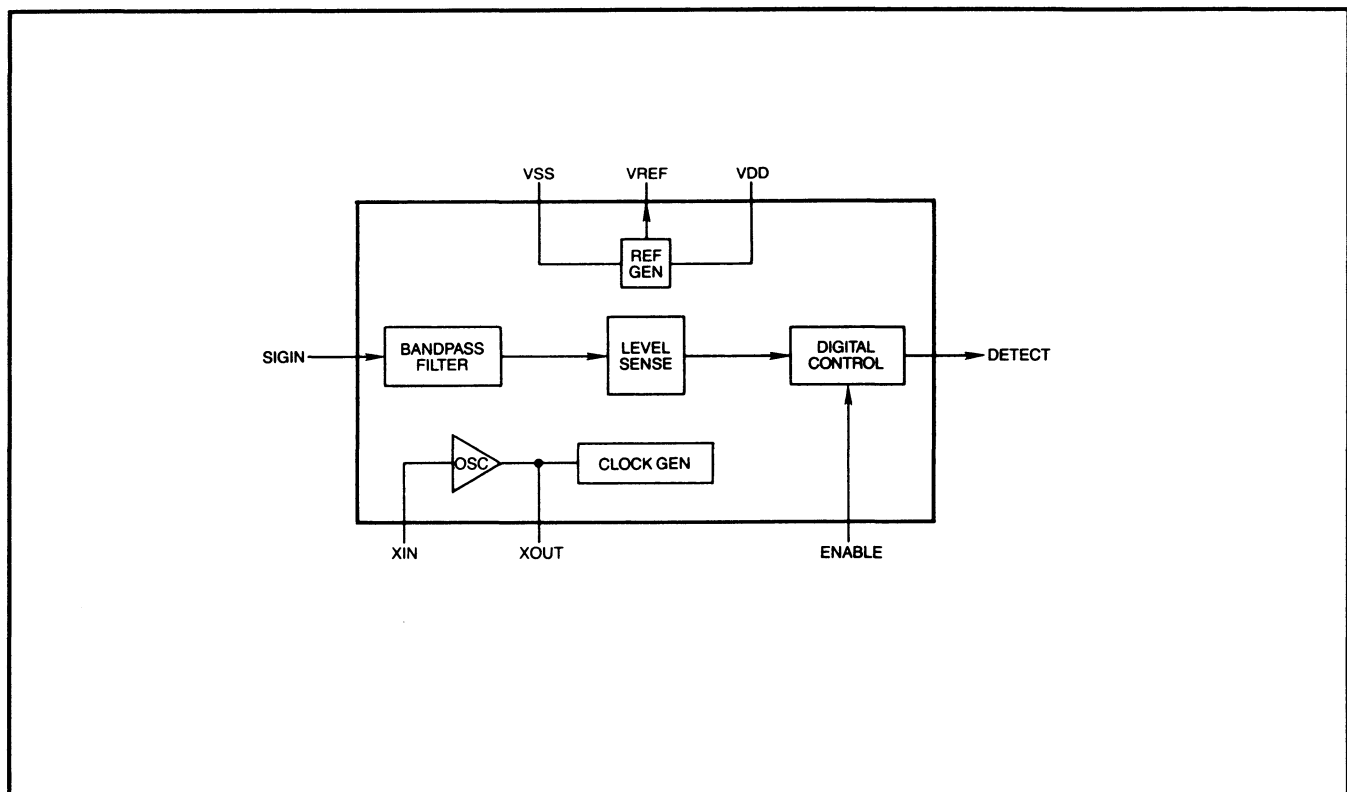- Billing systems

Figure 1 Pin Diagram

Figure 2 Typical Application: Dialed Digit Monitor

Table 1 Pin Descriptions

| Pin	Description
SIGIN	Signal input, AC or DC coupled (see level limitations elsewhere).
DETECT	Active output indicating signal detection. Activated by ENABLE.
ENABLE	Enables DETECT output. Used to mask signal activity.
VDD	Most positive power supply pin.
VREF	Internally generated reference voltage. (VSS + VDD) /2 volts.
VSS	Most negative power supply pin.
XIN, XOUT	Crystal attachment pins. XIN may be used as the input for an external 3.58 MHz clock.
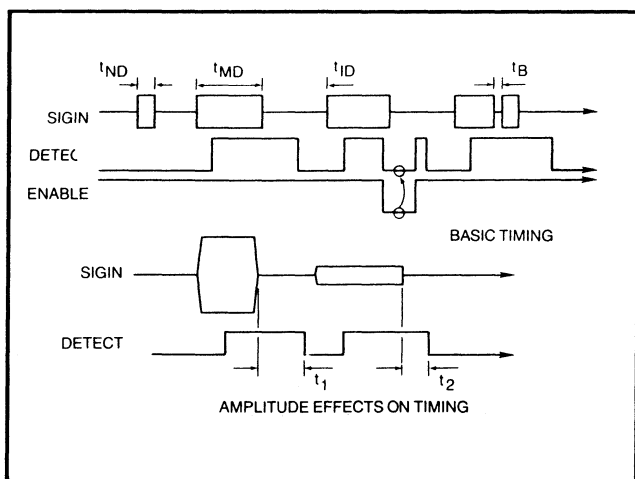
Figure 3 Signal Timing (See Table 2)
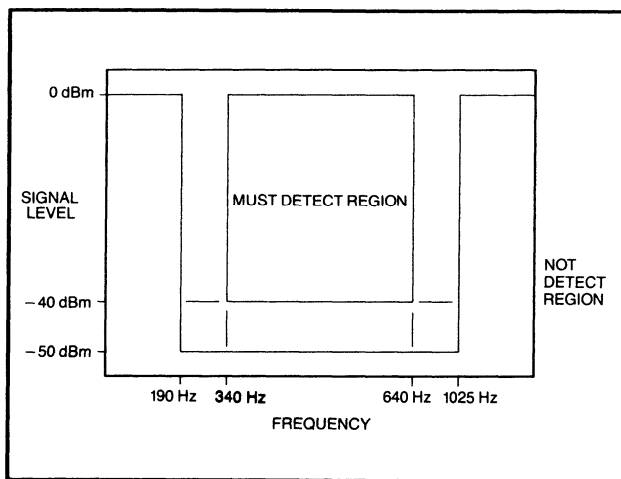
Figure 4 Detect Range

Table 2 Device Timing

Time	Value	Significance
tND	not specified	Length of an otherwise valid tone which will be ignored.
tMD	40 ms minimum	A valid tone will always be detected if it is at least 40 ms long.
tID	40 ms minimum	Inter-tone gaps must be at least 40 ms to be detected. See t1 and t2 below.
tB	20 ms maximum	Drop-outs of valid tone of up to 20 ms will be ignored.
t1	90 ms maximum	Detection of gaps may require as long as 90 ms following a large tone burst (0 dBm).
t2	40 ms maximum	Valid low level tones (< -10 dBm) will require only 40 ms for detection.

Table 3 Absolute Maximum Ratings*

DC Supply Voltage (VDD − VSS). . . . . 16.0 V
Voltage on SIGNAL IN. . . . . (VDD + 0.5 V) to (VSS − 22 V)
Voltage on Any Pin Except SIGNAL IN. . . . . (VDD + 0.5 V) to (VSS − 0.5 V)
Storage Temperature Range. . . . . −40° to 85° C
Operating Temperature Range. . . . . 0° to 70° C
Lead Soldering Temperature. . . . . 260° C for 5 seconds

* Note: Exceeding these ratings may permanently damage the M-980.

Table 4 Specifications

Unless otherwise noted, VDD − VSS = 4.5 to 5.5 V and Ta = 25°C.

Parameter		Min	Typ	Max	Units	Notes
Signal Detection	Level	−38		0	dBm	1, 2, 9
	Duration	40			ms	
Signal Rejection	Level			−50	dBm	1,2
				0	dBm	1, 3
	Duration			20	ms	2
Quiet Interval Detect ´	Duration	40			ms	4
		90			ms	5
"Detect" Output Pin	Logic 0			0.5	V	6
	Logic 1	4.5			V	6
"Enable", "XIN" Input Pin	Logic 0	VSS		VSS +0.2	V	7
	Logic 1	VDD-0.2		VDD	V	7
"XIN" Duty Cycle		40		60	%	
"XIN", "XOUT" Loading				10	pF	
"VREF" Output Pin	Deviation	−2		+2	%	8
	Resistance	3.25		6.75	Kohms	
"SIGIN" Input Pin	Max Voltage	VDD-18		VDD	V	
	Impedance (500 Hz)	80			Kohms	

Notes:

1. 0 dBm = 0.775 Vrms.
2. f = 340 to 640 Hz.
3. f > 1025 Hz, <190 Hz.
4. Signal dropping from −40 to −50 dBm.
5. Signal dropping from 0 to −50 dBm.

6. Output current = 1 mA, VSS − VDD = 5.0V.
7. Input current = 10 uA max.
8. Nominal = (VDD + VSS)/2.
9. −37 (Ta = 50°C), −36 (Ta = 60°C) −35 (Ta = 70°C).

Call Progress Tone Detection

Call progress tones are audible tones sent from switching systems to calling parties to show the status of calls. Calling parties can identify the success of a call placed by what is heard after dialing. The type of tone used and its timing vary from system to system, and though intended for human ears these signals can provide valuable information for automated calling systems.

The Teltone M-980 is a signal detector sensitive to the frequencies most often used for these progress tones. Electronic equipment monitoring the DETECT output of the M-980 can determine the nature of signals present by measuring their duty cycle. See Figure 5 for a diagram of a circuit that could be used to permit a microcomputer to directly monitor tones on the telephone line. Much of the character of the progress tones is in their duty cycle or cadence (sometimes referred to as interruption rate). This information, coupled with level and frequency indication from the M-980, can be used to decide what progress tones have been encountered.

For example, dial tones as shown in the table are usually "on" continuously and last until the first dial digit is received by the switching system. Line Busy, on the other hand, is turned off and on at a rate of 1 Hz with a a 50% duty cycle, or an interruption rate of 60 times per minute (60 IPM). The tones can be distinguished in this way. Table 5 shows some call progress tones with on/off times—0.25/0.25 being 250 ms on, 250 ms off on a repeating basis. It should be noted that while such techniques will usually be effective, there are some circumstances in which the M-980 cannot be accurately used. Examples include situations where ringback tone may be short or not even encountered. Ringback may be provided at ringing voltage frequency (20 or 30 Hz) with some harmonics and may not fall in the detect range, and speech or other strong noise may obscure tones making cadence measurement difficult. Detection of "answer" is most difficult for many reasons. One way to determine if a called party has answered is by looking for a short burst of DETECT indications without a cadence match (produced by a click and "hello" at the far

end). Some applications will require special methods like speech detection, but most can be reliably handled with the M-980 and simple cadence measurement.

As can be seen, the tones used for the same purposes in different systems may not be the same. Standards do exist and should be consulted for your particular application. In North America AT&T's "Notes on the Network" or EIA's RS-464 PBX standard should be reviewed. In Europe tone plans may vary with locale, in which case the CEPT administration in each country must be consulted. Outside these areas, national PTT organizations can provide information on the systems within their borders.

Table 5 Call Progress Tones

Frequency 1	Frequency 2	On/Off	Use
350	+440	Continuous	Dial tones
425	—		
600	X 120		
400	—		
480	+620	0.5/0.5s	Line Busy Tones
600	X 120		
480	+ 620	0.25/0.25s	Reorder Tones
600	X 120		
440	+ 480	2.0/4.0s	Audible Ringing
500	X 40		
440		0.5s burst	Various
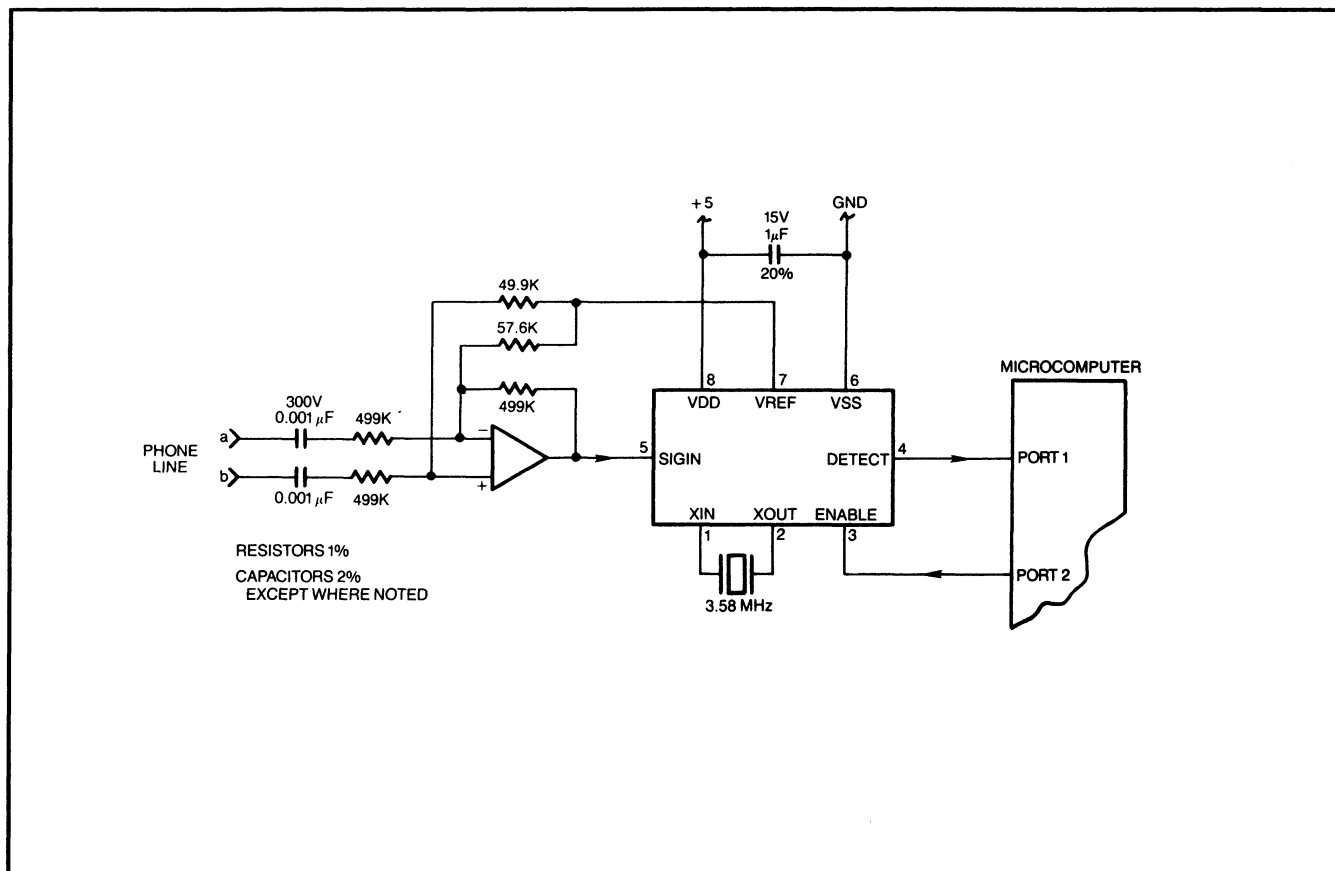
Figure 5 A Telephone Line Circuit Application

8-Lead Plastic DIP
617-00015-01

8-Lead CerDIP
617-00015-02

$\dfrac{0.400}{(10.160)}$ MAX

$\dfrac{0.250 \pm 0.005}{(6.350 - 0.127)}$

$\dfrac{0.300 - 0.320}{(7.620 - 8.128)}$

$\dfrac{0.125}{(3.175)}$ MIN

$\dfrac{0.018 \pm 0.003}{(0.457 \pm 0.076)}$

$\dfrac{0.100}{(2.540)}$ TYP

$\dfrac{0.400}{(10.160)}$ MAX

$\dfrac{0.291}{(7.391)}$ MAX

$\dfrac{0.290 - 0.320}{(7.366 - 8.128)}$

$\dfrac{0.125}{(3.175)}$ MIN

$\dfrac{0.018 \pm 0.002}{(0.457 \pm 0.051)}$

$\dfrac{0.100 \pm 0.010}{(2.540 \pm 0.254)}$

$\dfrac{\text{INCHES}}{\text{MILLIMETERS}}$

Figure 6 Package Dimensions

Teltone Corporation / 10801-120th Avenue NE, Kirkland, WA 98033   Phone: 1-800-426-3926 or 206-827-9626   Fax: 206-827-6050   TWX: 910-449-2862
Teltone Limited / 3375-14th Avenue, Markham, Ontario, Canada L3R 2L6   Phone: 416-475-0837   Fax: 416-474-9151   Envoy User Name: TTL.HQ

4-6
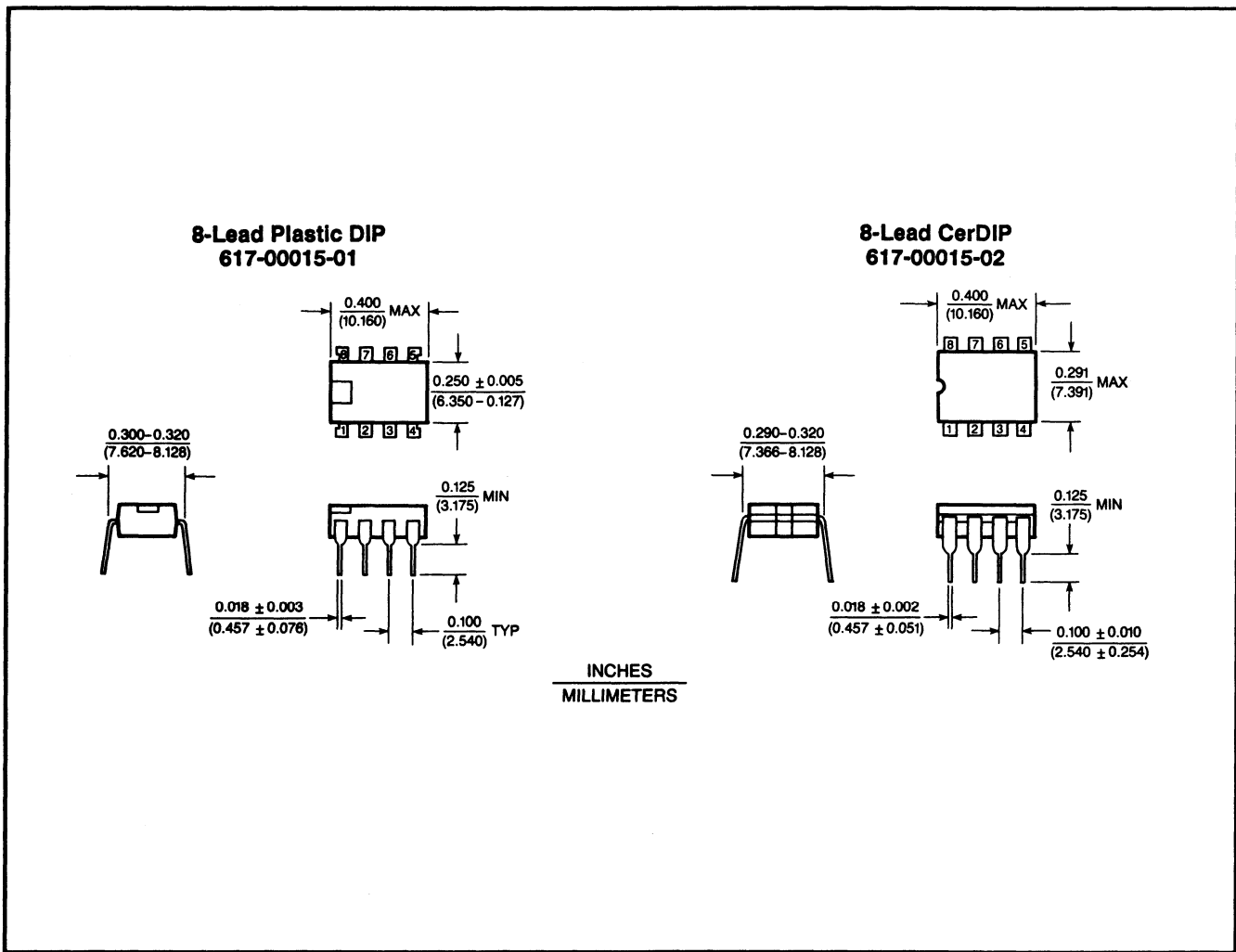
M-981 PRECISE CALL PROGRESS TONE DETECTOR

The Teltone® M-981 is an integrated circuit precise tone detector for special purpose use in automatic following of switched telephone calls. The circuit uses low-power CMOS techniques to provide the complete filtering and control required for this function. The basic timing of the M-981 is designed to permit operation with almost any progress tone system.

The use of integrated circuit techniques allows the M-981 to pack the four filters and amplitude detectors for call progress following into a single 22-pin DIP. A 3.58 MHz crystal-controlled time base guarantees accuracy and repeatability.

Features

- Precise detection of call progress tones
- Linear (analog) input
- Digital (CMOS compatible), tri-statable outputs
- 22-pin DIP
- Single supply 5 V CMOS (low power)
- Inexpensive 3.58-MHz time base
- Wide dynamic range (30 dB)

Applications

- Automatic dialers
- Dialing modems
- Traffic measurement systems
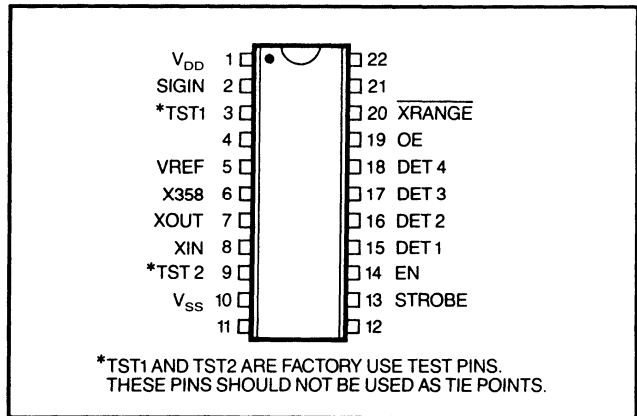- Test equipment
- Service evaluation
- Billing systems


```
            V_DD  1 □•        □ 22
           SIGIN  2 □         □ 21
           *TST1  3 □         □ 20  XRANGE
                  4 □         □ 19  OE
            VREF  5 □         □ 18  DET 4
            X358  6 □         □ 17  DET 3
            XOUT  7 □         □ 16  DET 2
             XIN  8 □         □ 15  DET 1
           *TST2  9 □         □ 14  EN
            V_SS 10 □         □ 13  STROBE
                 11 □         □ 12
```

*TST1 AND TST2 ARE FACTORY USE TEST PINS.
THESE PINS SHOULD NOT BE USED AS TIE POINTS.
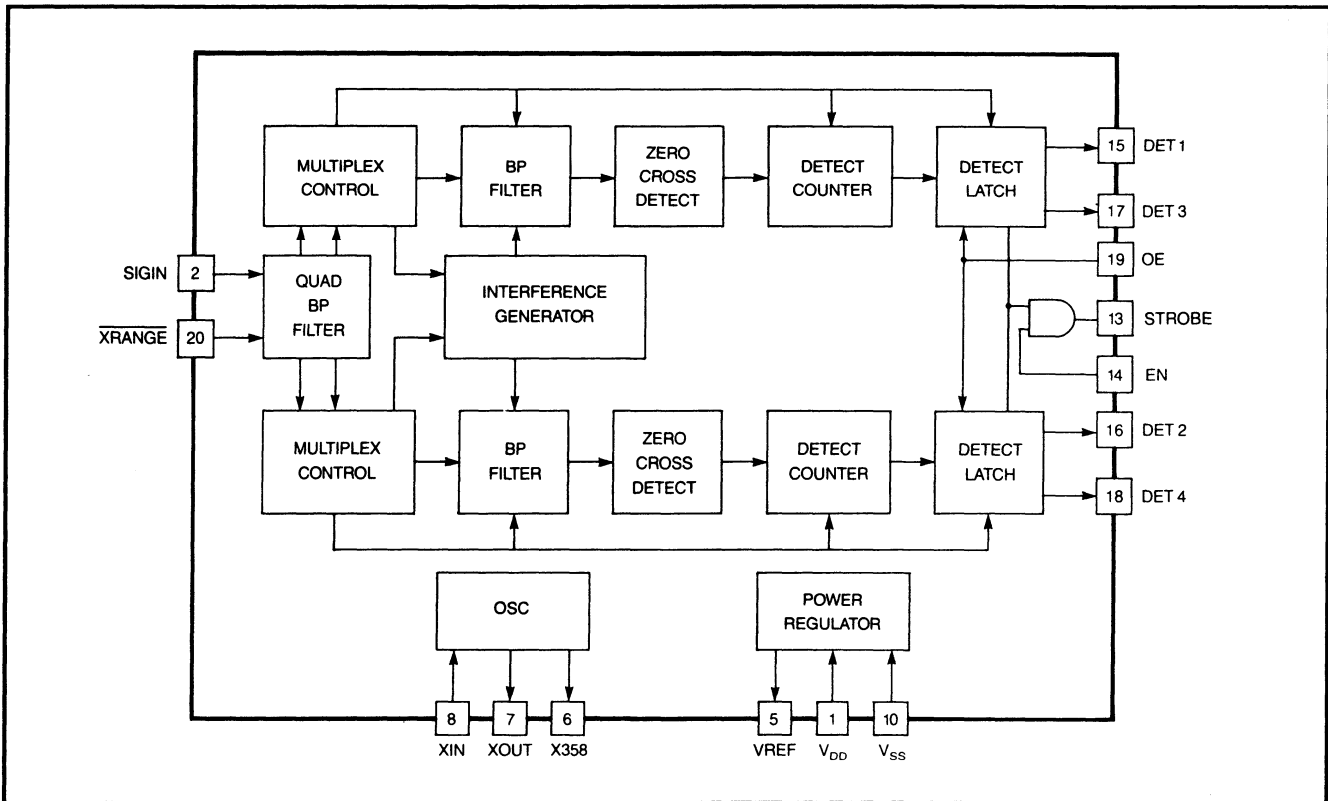
Figure 1 Pin Diagram

Figure 2 Block Diagram

Call Progress Tone Detection

Call progress tones are audible tones sent from switching systems to calling parties to show the status of calls. Calling parties can identify the success of a call placed by what is heard after dialing. The type of tone used and its timing vary from system to system, and though intended for human ears these signals can provide valuable information for automated calling systems.

The Teltone M-981 contains four signal detectors sensitive to the frequencies often used for these progress tones. Electronic equipment monitoring the DET n outputs of the M-981 can determine the nature of signals present by measuring their duty cycle. See Figure 4 for a diagram of a circuit that could be used to permit a microcomputer to directly monitor tones on the telephone line. Much of the character of the progress tones is in their duty cycle or cadence (sometimes referred to as interruption rate). This information, coupled with level and frequency indication from the M-981, can be used to decide what progress tones have been encountered.

For example, dial tones as shown in the table are usually "on" continuously and last until the first dial digit is received by the switching system. Line Busy, on the other hand, is turned off and on at a rate of 1 Hz with a a 50% duty cycle, or an interruption rate of 60 times per minute (60 IPM). The tones can be distinguished in this way. Table 4 shows some call progress tones with on/off times—0.25/0.25 being 250 ms on, 250 ms off on a repeating basis. It should be noted that while such techniques will usually be effective, there are some circumstances in which the M-981 cannot be accurately used. Examples include situations where ringback tone may be short or not even encountered. Ringback may be provided at ringing voltage frequency (20 or 30 Hz) with some harmonics and may not fall in the detect range, and speech or other strong noise may obscure tones making cadence measurement difficult.

As can be seen, the tones used for the same purposes in different systems may not be the same. Standards do exist and should be consulted for your particular application. In North America AT&T's "Notes on the Network" or EIA's RS-464 PBX standard should be reviewed. In Europe tone plans may vary with locale, in which case the CEPT administration in each country must be consulted. Outside these areas, national PTT organizations can provide information on the systems within their borders.

Table 1 Pin Functions

Pin	Function
DET1	Active high tri-statable output, detect for 350 Hz.
DET2	Active high tri-statable output, detect for 400 Hz.
DET3	Active high tri-statable output, detect for 440 Hz.
DET4	Active high tri-statable output, detect for 480 Hz.
EN	Active high enable, when low drives STROBE low.
OE	Active low input. When high tri-states DETn pins.
SIGIN	Analog signal input (internally capacitive coupled).
STROBE	Active high output, indicates valid DETn.
V_{DD}	Most positive power supply input pin.
VREF	Internally generated mid-power supply voltage (output).
V_{SS}	Most negative power supply input pin.
X358	Buffered oscillator output (3.58 MHz).
XIN	Crystal oscillator or digital clock input.
XOUT	Crystal oscillator output.
XRANGE	Active low input. Adds 10 dB of gain to input stage.

Table 2 Truth Table

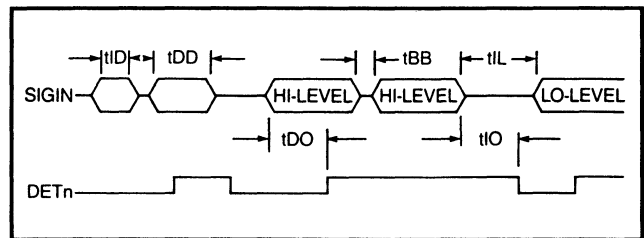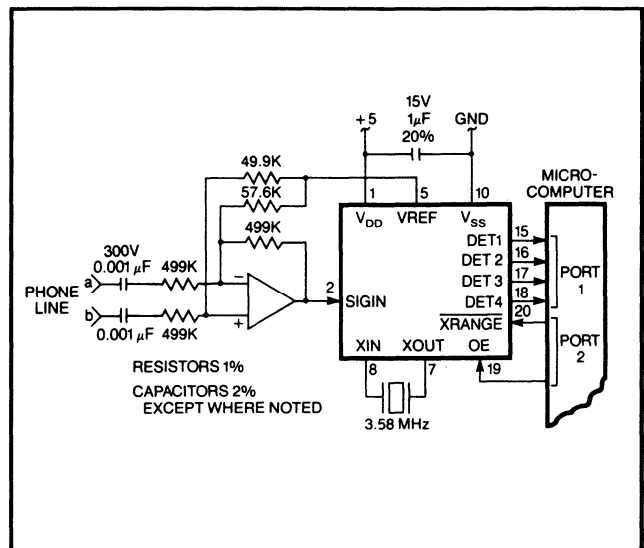| Signal present (fo)	DET1	DET2	DET3	DET4	STROBE	OE	EN
350 Hz	1	X	X	X	1	1	1
400 Hz	X	1	X	X	1	1	1
440 Hz	X	X	1	X	1	1	1
480 Hz	X	X	X	1	1	1	1
Other In-Band	0	0	0	0	0	1	1
Any	High Impedance				X	0	1
Any	High Impedance				0	0	0

Figure 3 Signal Timing (See Table 3)

Figure 4 A Telephone Line Circuit Application

Table 3 Specifications

Unless otherwise noted, $V_{DD} - V_{SS} = 5V$ and Ta = 25°C

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Conditions Power	V_{DD}	—	4.75	—	5.5	V	
	Power Supply Noise	0.1-5 kHz	—	—	20	mV p-p	
	Current Drain (IDD)	—	—	—	20	mA	
Signal Detection	Frequency Range	in-band signal	−2.2	—	+2.2	% of fo	
	Level	—	−26	—	0	dBm	2
	Duration (tDD)	—	160	—	—	ms	
	Bridge Time (tBB)	—	—	—	30	ms	
	Level Skew Between Adjacent In-Band Signals	for detection of both	—	—	6	dB	3
	High Level to Low Level Signal for Detection of Both (tIL)	high = 0 dBm low = − 30 dBm	1	—	—	s	
	Time to Output (tDO)	—	—	—	200	ms	
Signal Rejection	Level	noise at SIGIN 0.2-3.4 kHz	—	—	− 50	dBm	4, 5
	Interval Duration (tID)	—	115	—	—	ms	
	Time to Output (tIO)	—	—	—	200	ms	
Outputs	DETECT Pins (DETn):						
	VOL	ISINK = − 1 mA	—	—	0.5	V	
	VOH	ISOURCE = 1 mA	V_{DD}-0.5	—	—	V	
	IOZ	VO = V_{DD}, V_{SS}	—	—	1	µA	
	TEN, Z to Lo or Hi	CL = 50 pF	—	—	100	µs	
	TDE, Lo or Hi to Z	RL = 100 Kohms	—	—	100	µs	
	STROBE PIN:						
	VOL	ISINK = − 1 mA	—	—	0.5	V	
Inputs	EN, OE, $\overline{XRANGE}$ Pins:						
	VIL	—	—	—	0.5	V	
	VIH	—	V_{DD}-2.0	—	—	V	
	Pullup Current	EN, OE, $\overline{XRANGE}$ = V_{SS}	—	—	10	µA	
	SIGIN Pin:						
	Voltage Range	—	V_{DD}-18	—	V_{DD}	V	
	Input Impedance	f = 500 Hz	80K	—	—	ohms	
Gain		$\overline{XRANGE}$ = 0	9.9	—	10.1	dB	
Clock	External Clock:	XOUT open					
	VIL	—	—	—	0.2	V	
	VIH	—	V_{DD}-0.2	—	—	V	
	Duty Cycle	—	40	—	60	%	
	XIN, XOUT Loading	Crystal Osc. Active					
	Capacitance	—	—	—	10	pF	
	Resistance	—	20M	—	—	ohms	
	X358 Pin:	CL = 20 pF					
	VOL	ISINK = − 10µA	—	—	0.2	V	
	VOH	ISOURCE = 10 µA	V_{DD}-0.2	—	—	V	
	Duty Cycle	—	40	—	60	%	

Notes

1. All parameters are specified at V_{DD} = 5 volts and $\overline{XRANGE}$ at a logical "hi" state (i.e. unity front-end gain). Power levels are in dBm referenced to 600 ohms. All DC voltages are referenced to V_{SS}.

2. A post-filter AGC is employed to enhance end-of-tone detection for high-level signals. A drop in amplitude of the input tone may cause an end-of-tone (interval) indication.

3. Any tone 40 Hz from center frequency must adhere to this specification.

4. Large input voltage transients may cause excessive ringing in the highly selective filter, causing spurious detection. The detects are not considered as incorrect circuit operation.

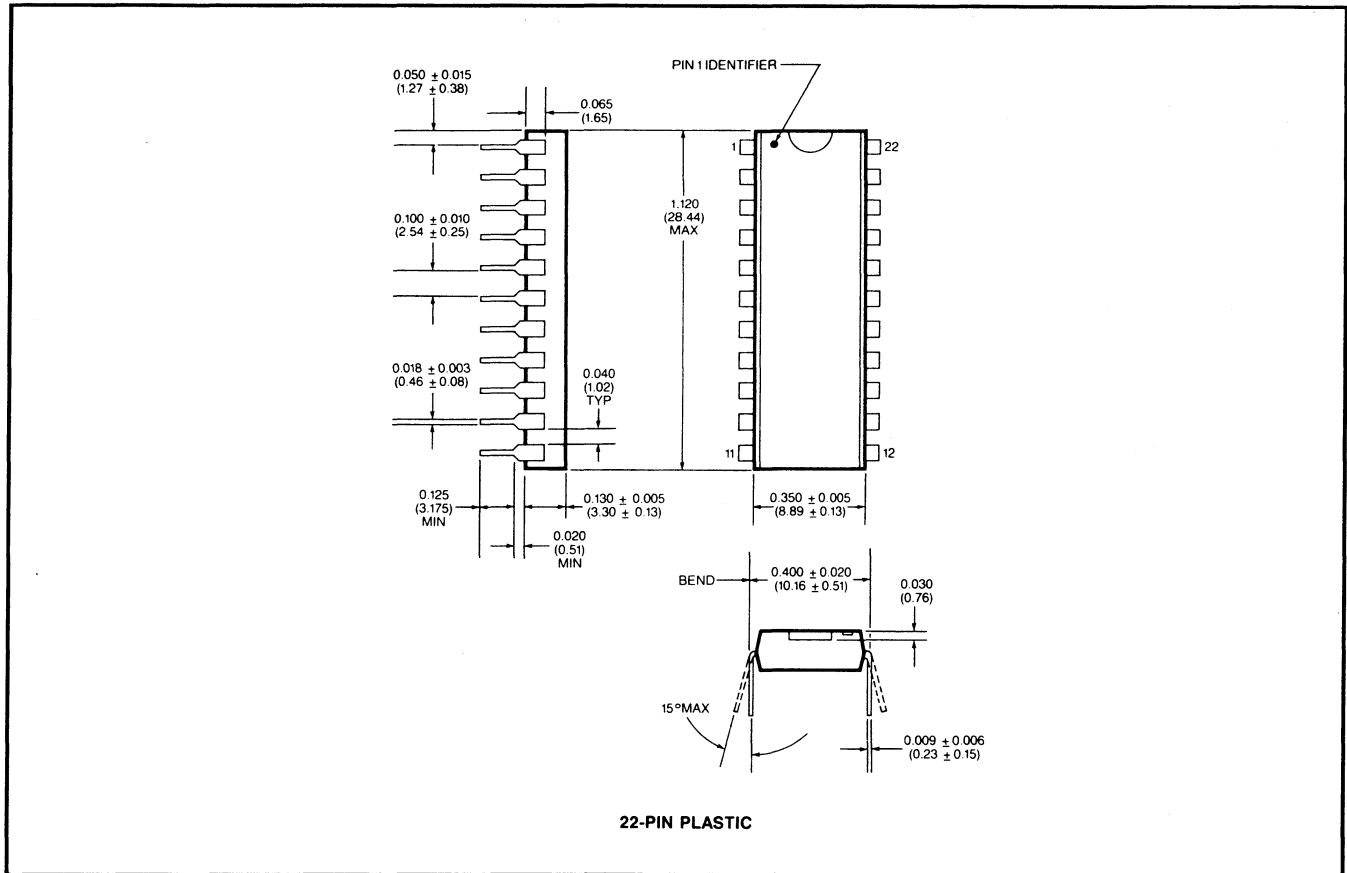5. Frequency 5% away from center frequency.

Figure 5 Package Dimensions

Table 4 Call Progress Tones

Frequency 1	Frequency 2	On/Off	Use
350	+440	Continuous	Dial tones
400	—		
440	+480	2.0/4.0s	Audible Ringing
440		0.5s burst	Various

Table 5 Absolute Maximum Ratings (Note 1)

Storage Temperature . . . . -40 to $125\,°C$
Operating Ambient Temperature . . . . -0 to $70\,°C$
V_{DD} 15V
Input Voltage on SIGIN . . . . . . $V_{SS} -22$ to $V_{DD} +0.5V$
Input Voltages (except SIGIN) . . . . $V_{SS} -0.3$ to $V_{DD} +0.3V$
Lead Soldering Temperature . . . . . $260\,°C$ for 5 seconds

Note:

1. Exceeding these ratings may permanently damage the M-981.

M-982 PRECISE CALL PROGRESS TONE DETECTOR

The Teltone® M-982 is an integrated circuit precise tone detector for special purpose use in automatic following of switched telephone calls. The circuit uses low-power CMOS techniques to provide the complete filtering and control required for this function. The basic timing of the M-982 is designed to permit operation with almost any progress tone system.

The use of integrated circuit techniques allows the M-982 to pack the four filters and amplitude detectors for call progress following into a single 22-pin DIP. A 3.58 MHz crystal-controlled time base guarantees accuracy and repeatability.

Features

- Precise detection of call progress tones
- Linear (analog) input
- Digital (CMOS compatible), tri-statable outputs
- 22-pin DIP
- Single supply 5 volt CMOS (low power)
- Inexpensive 3.58-MHz time base
- Wide dynamic range (30 dB)

Applications

- Automatic dialers
- Dialing modems
- Traffic measurement equipment
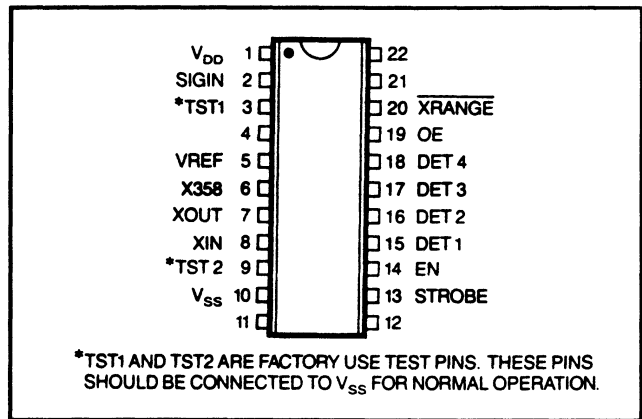- Test equipment
- Service evaluation
- Billing systems

*TST1 AND TST2 ARE FACTORY USE TEST PINS. THESE PINS SHOULD BE CONNECTED TO V_{SS} FOR NORMAL OPERATION.
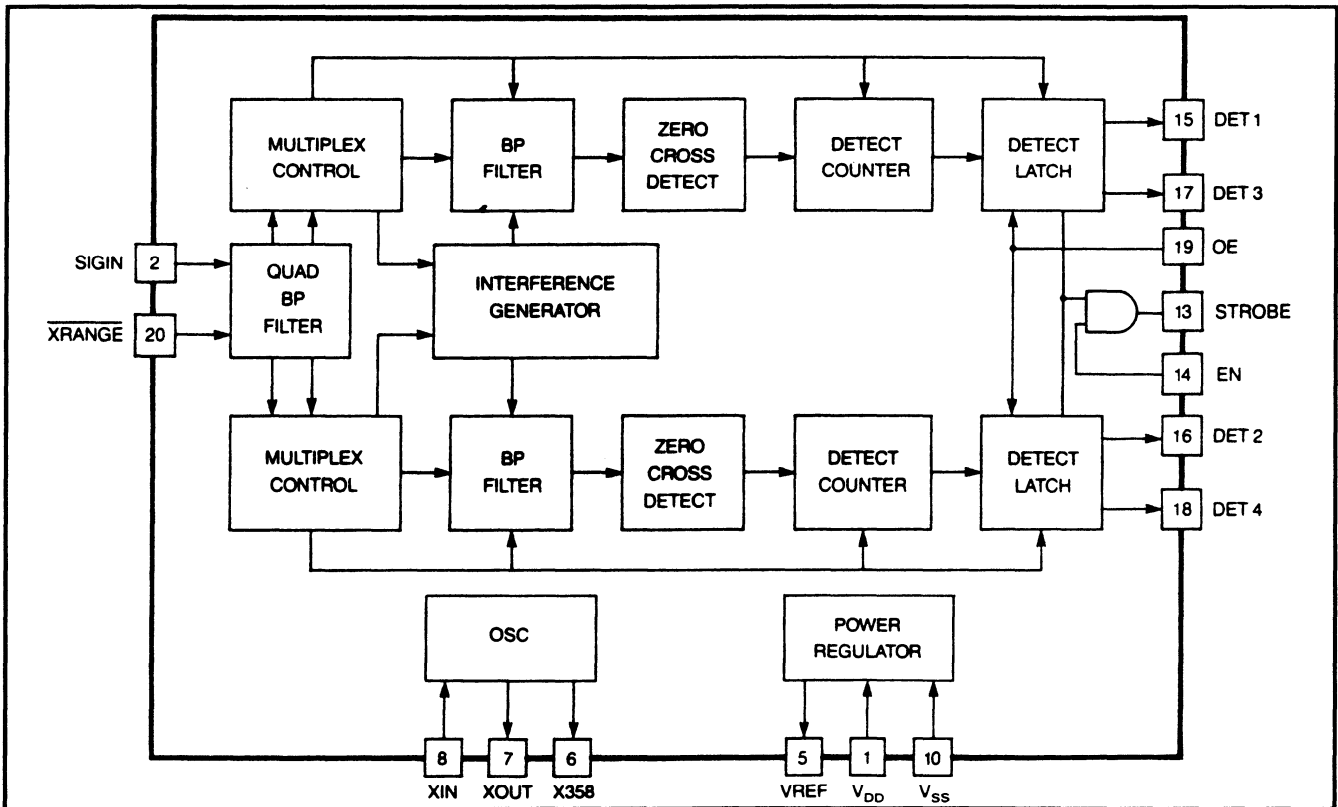
Figure 1 Pin Diagram

Figure 2 Block Diagram

4-11

Call Progress Tone Detection

Call progress tones are audible tones sent from switching systems to calling parties to show the status of calls. Calling parties can identify the success of a call placed by what is heard after dialing. The type of tone used and its timing vary from system to system, and though intended for human ears these signals can provide valuable information for automated calling systems.

The Teltone M-982 contains four signal detectors sensitive to the frequencies often used for these progress tones. Electronic equipment monitoring the DET n outputs of the M-982 can determine the nature of signals present by measuring their duty cycle. See Figure 4 for a diagram of a circuit that could be used to permit a microcomputer to directly monitor tones on the telephone line. Much of the character of the progress tones is in their duty cycle or cadence (sometimes referred to as interruption rate). This information, coupled with level and frequency indication from the M-982, can be used to decide what progress tones have been encountered.

For example, dial tones as shown in the table are usually "on" continuously and last until the first dial digit is received by the switching system. Line Busy, on the other hand, is turned off and on at a rate of 1 Hz with a a 50% duty cycle, or an interruption rate of 60 times per minute (60 IPM). The tones can be distinguished in this way. Table 4 shows some call progress tones with on/off times—0.25/0.25 being 250 ms on, 250 ms off on a repeating basis. It should be noted that while such techniques will usually be effective, there are some circumstances in which the M-982 cannot be accurately used. Examples include situations where ringback tone may be short or not even encountered. Ringback may be provided at ringing voltage frequency (20 or 30 Hz) with some harmonics and may not fall in the detect range, and speech or other strong noise may obscure tones making cadence measurement difficult.

As can be seen, the tones used for the same purposes in different systems may not be the same. Standards do exist and should be consulted for your particular application. In North America AT&T's "Notes on the Network" or EIA's RS-464 PBX standard should be reviewed. In Europe tone plans may vary with locale, in which case the CEPT administration in each country must be consulted. Outside these areas, national PTT organizations can provide information on the systems within their borders.

Table 1 Pin Functions

Pin	Function
DET1	Active high tri-stateable output, detect for 350 Hz.
DET2	Active high tri-stateable output, detect for 620 Hz.
DET3	Active high tri-stateable output, detect for 440 Hz.
DET4	Active high tri-stateable output, detect for 480 Hz.
EN	Active high enable, when low drives STROBE low.
OE	Active high input. When low tri-states DETn pins.
SIGIN	Analog signal input (internally capacitive coupled).
STROBE	Active high output, indicates valid DETn.
V_{DD}	Most positive power supply input pin.
VREF	Internally generated mid-power supply voltage (output).
V_{SS}	Most negative power supply input pin.
X358	Buffered oscillator output (3.58 MHz).
XIN	Crystal oscillator or digital clock input.
XOUT	Crystal oscillator output.
$\overline{XRANGE}$	Active low input. Adds 10 dB of gain to input stage.

Table 2 Truth Table

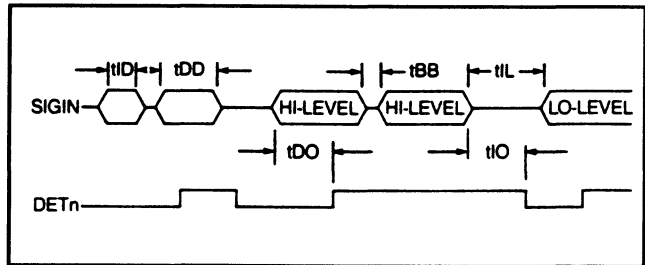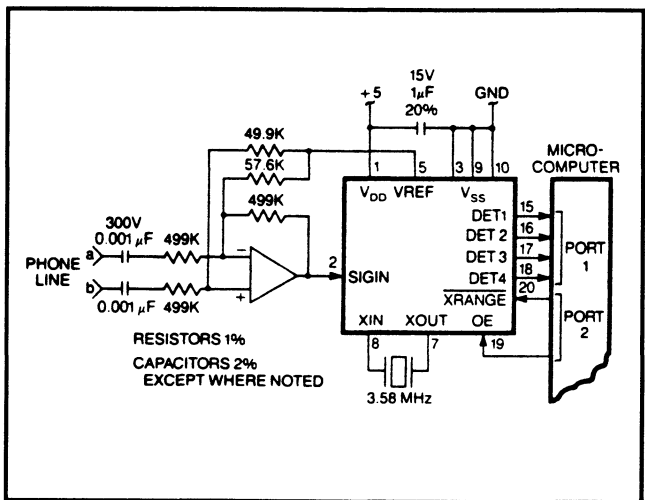| Signal present (fo)	DET1	DET2	DET3	DET4	STROBE	OE	EN
350 Hz	1	X	X	X	1	1	1
620 Hz	X	1	X	X	1	1	1
440 Hz	X	X	1	X	1	1	1
480 Hz	X	X	X	1	1	1	1
Other In-Band	0	0	0	0	0	1	1
Any	High Impedance				X	0	1
Any	High Impedance				0	0	0

Figure 3 Signal Timing (See Table 3)

Figure 4 A Telephone Line Circuit Application

Table 3 Specifications

Unless otherwise noted, $V_{DD} - V_{SS} = 5V$ and Ta = 25°C

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Conditions Power	V_{DD}	—	4.75	—	5.5	V	1
	Power Supply Noise	0.1-5 kHz	—	—	20	mV p-p	
	Current Drain (IDD)	—	—	—	20	mA	
Signal Detection	Frequency Range	in-band signal	−1	—	+1	% of fo	
	Level	—	−25	—	0	dBm	2
	Duration (tDD)	—	200	—	—	ms	
	Bridge Time (tBB)	—	—	—	30	ms	
	Level Skew Between Adjacent In-Band Signals	for detection of both	—	—	6	dB	3
	High Level to Low Level Signal for Detection of Both (tIL)	high = 0 dBm low = −30 dBm	1	—	—	s	
	Time to Output (tDO)	—	—	—	200	ms	
Signal Rejection	Level	noise at SIGIN 0.2-3.4 kHz	—	—	−50	dBm	4, 5
	Interval Duration (tID)	—	115	—	—	ms	
	Time to Output (tIO)	—	—	—	200	ms	
Outputs	DETECT Pins (DETn):						
	VOL	ISINK = −1 mA	—	—	0.5	V	
	VOH	ISOURCE = 1 mA	V_{DD}-0.5	—	—	V	
	IOZ	VO = V_{DD}, V_{SS}	—	—	1	μA	
	TEN, Z to Lo or Hi	CL = 50 pF	—	—	100	μs	
	TDE, Lo or Hi to Z	RL = 100 Kohms	—	—	100	μs	
	STROBE PIN:						
	VOL	ISINK = −1 mA	—	—	0.5	V	
Inputs	EN, OE, $\overline{XRANGE}$ Pins:						
	VIL	—	—	—	0.5	V	
	VIH	—	V_{DD}-2.0	—	—	V	
	Pullup Current	EN, OE, $\overline{XRANGE}$ = V_{SS}	—	—	10	μA	
	SIGIN Pin:						
	Voltage Range	—	V_{DD}-18	—	V_{DD}	V	
	Input Impedance	f = 500 Hz	80K	—	—	ohms	
Gain		$\overline{XRANGE}$ = 0	9.9	—	10.1	dB	
Clock	External Clock:	XOUT open					
	VIL	—	—	—	0.2	V	
	VIH	—	V_{DD}-0.2	—	—	V	
	Duty Cycle	—	40	—	60	%	
	XIN, XOUT Loading	Crystal Osc. Active					
	Capacitance	—	—	—	10	pF	
	Resistance	—	20M	—	—	ohms	
	X358 Pin:	CL = 20 pF					
	VOL	ISINK = −10μA	—	—	0.2	V	
	VOH	ISOURCE = 10 μA	V_{DD}-0.2	—	—	V	
	Duty Cycle	—	40	—	60	%	

Notes

1. All parameters are specified at V_{DD} = 5 volts and $\overline{XRANGE}$ at a logical "hi" state (i.e. unity front-end gain). Power levels are in dBm referenced to 600 ohms. All DC voltages are referenced to V_{SS}.

2. A post-filter AGC is employed to enhance end-of-tone detection for high-level signals. A drop in amplitude of the input tone may cause an end-of-tone (interval) indication.

3. Any tone 40 Hz from center frequency must adhere to this specification.

4. Large input voltage transients may cause excessive ringing in the highly selective filter, causing spurious detection. The detects are not considered as incorrect circuit operation.
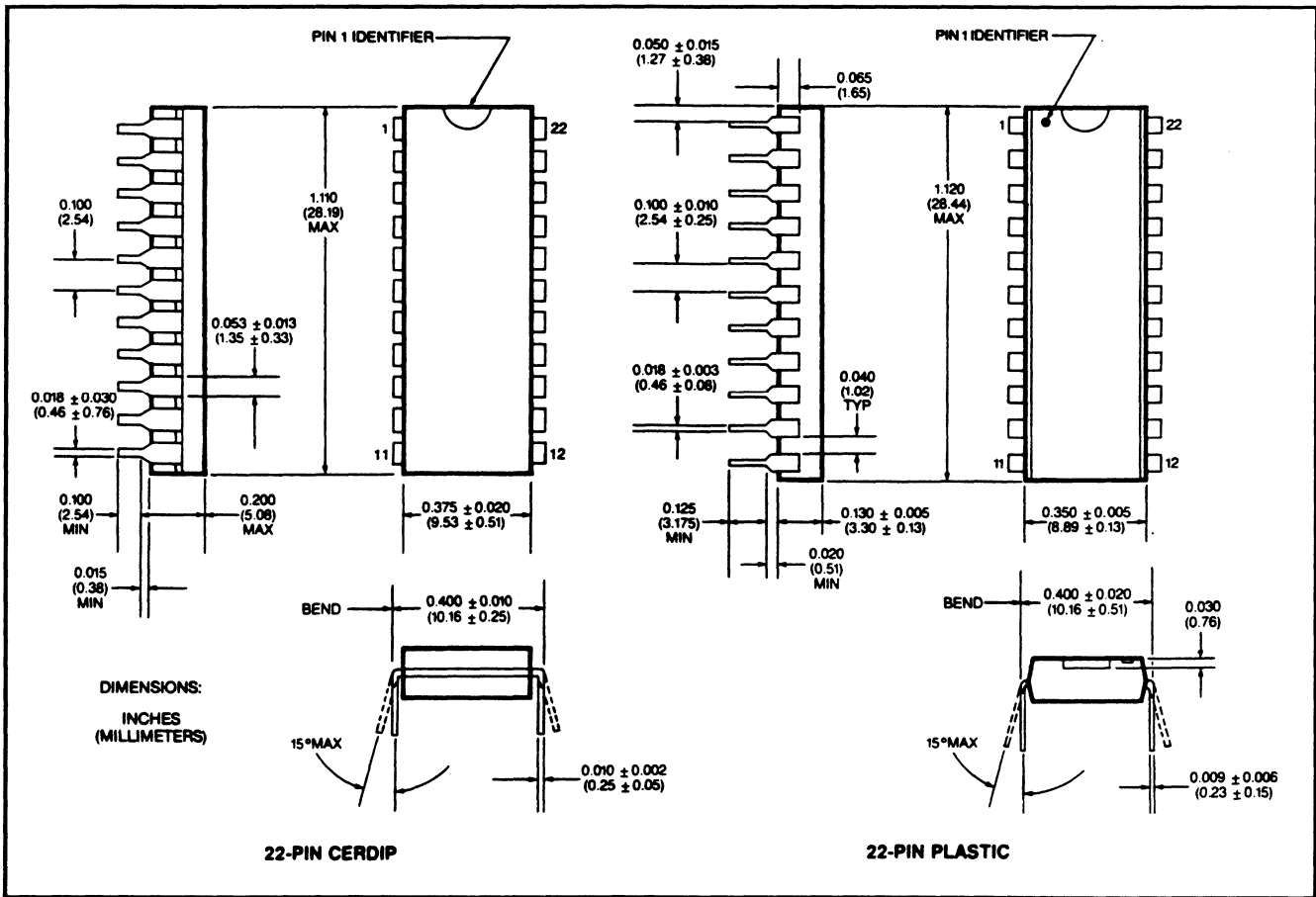
5. Frequency 5% away from center frequency.

Figure 5 Package Dimensions

Table 4 Call Progress Tones

Frequency 1	Frequency 2	On/Off	Use
350	+440	Continuous	Dial tones
480	+620	0.5/0.5s	Line Busy Tones
480	+620	0.25/0.25s	Reorder Tones
440	+480	2.0/4.0s	Audible Ringing
440		0.5s burst	Various

Table 5 Absolute Maximum Ratings (Note 1)

Storage Temperature . . . . -40 to $125\,°C$
Operating Ambient Temperature. . . . . . -0 to $70\,°C$
V_{DD} . . . . 15 V
Input Voltage on SIGIN . . . $V_{SS} -22$ to $V_{DD} +0.5$ V
Input Voltages (except SIGIN). $V_{SS} -0.3$ to $V_{DD} +0.3$ V
Lead Soldering Temperature. . . . $260\,°C$ for 5 seconds

Note:

1. Exceeding these ratings may permanently damage the M-982.

M-984 SPECIAL TONE AND CALL PROGRESS TONE DETECTOR

The Teltone® Special Tone and Call Progress Tone Detector is a monolithic integrated circuit designed to provide reliable detection of many common telephone network status signals. In particular, it detects the signals known as special information tones (SITs) or error tones as defined by the CCITT, and single tones often used as dial tone, audible ringing, and other general progress indications. The M-984 uses CMOS switched capacitor filters and a crystal time base to achieve the high stability and accuracy specified. Each tone detection window has an associated output pin, which can e placed in a high impedance state for use with time-share microcomputer bus applications.

Features

* Detects single-frequency tones used for error indication and call progress in telephone systems
* Provides detection windows for:
  400/425 Hz (Call Progress)
  950 Hz ⎫
  1400 Hz ⎬ (Special and error indication)
  1800 Hz ⎭
* Separate 3-state outputs for each tone window
* 3.58 MHz crystal time base
* Auxiliary 3.58 MHz clock output

* CMOS with switched capacitor technology
* Compact 14-pin DIP package
* Single 5 VDC supply
* 0 to -30 dBm detect range

Applications

* Automatic dialers
* Modems
* Telecom text equipment
* Telephone traffic measurement
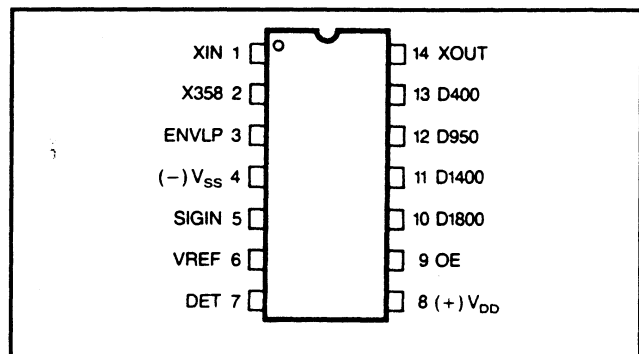* Service evaluation
* Billing equipment
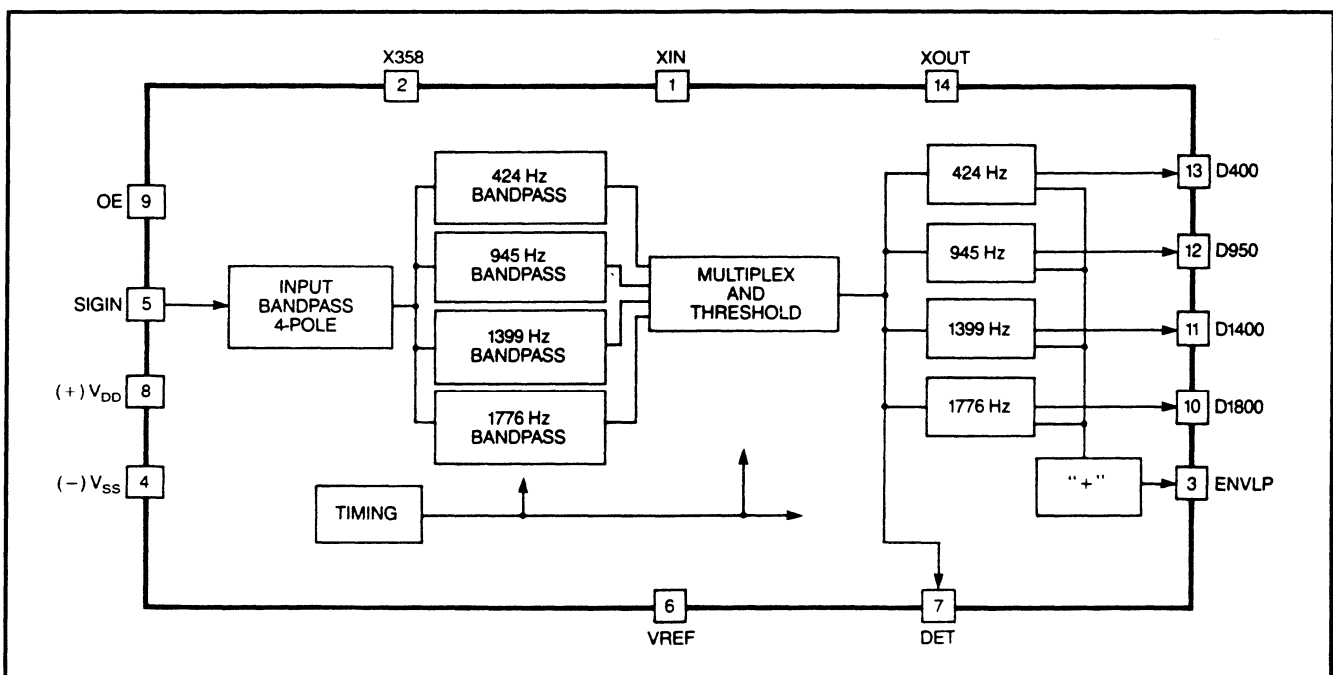

Figure 1 Pin Diagram

Figure 2 Block Diagram

Table 1 Pin Functions

Pin	Function
1, 14 XIN, XOUT	Crystal Connection — 3.58 MHz crystal across these pins will produce the timebase needed for proper operation of the M-984. An external clock signal may be fed to XIN providing the clock signal has a duty cycle of 50 ± 10% and comes within 0.2 volt of the supply rails. XOUT remains unconnected when an external clock is used. When used with a crystal, a 1 megohm resistor should be connected across XIN and XOUT.
2 X358	A buffered output pin. A 3.58 MHz clock signal is available for use in other circuits as a timebase. Leave open when unused.
3 ENVLP	The strobe pin is a common detection indicator for the four detect pins. Simply put, the strobe is a logical "OR" of the active detect circuits for each of the four windows, though there is a delay provided to permit strobe to latch the first active detect pin. Strobe is not 3-state controlled.
4, 8 VSS, VDD	The power supply pins, VDD being the most positive. Commonly, VDD is at 5 volts, while VSS is at ground.
5 SIGIN	The signal input pin, for analog signals referenced to VSS. The input voltage range is between VDD and VSS, and an input impedance of about 80 kohms is presented.
6 VREF	VREF is a bias voltage generated in the chip for use in external analog circuits, such as active filters and AC-coupled buffers. Leave open when unused.
7 DET	This is a general digital output pin not designated for use in application. The combined output of the four bandpass window filters after the signal has been converted to square wave and before the digital timing circuits appears on the pin. Leave open.
9 OE	The 3-state control pin. OE places the DET pins in the active mode when at logic "1". When at logic "0", OE causes the DET outputs to appear as high impedance. Should be tied to logic "1" when the M-984 is not used in a time-shared bus application.
10, 11 12, 13 D1800 D1400 D950 D400	The detect outputs associated with each window. 3-state control is available through use of the OE pin (9). Timing is shown in the timing diagram.

Figure 3 Timing Diagram

Table 2 Specifications

	PARAMETER	MIN	TYPICAL	MAX	UNITS	NOTES
Basic Operation	Power Supply	4.5	-	5.5	volts	
		-	4	30	mA	5.0 VDC
		-	-	20	mV	Noise Limit
	Input Spectrum	-	-	28	kHz	
Signal Detection	Level	-30	-	0	dBm	
	Duration	50	-	-	ms	
	Bridge Time	15	35	-	ms	
	S/N Ratio	16	-	-	dB	
	Drop Out	-	-	50	ms	
Signal Rejection	Level (In-Band)	-	-35	-40	dBm	200-3400 Hz
	(Other)	-	-	0	dBm	1% outside limit
Logic Conventions (except X358)	V (Out Low)	-	-	0.5	volts	1.0 mA Sink
	V (Out High)	V_{DD} -0.5	-	-	volts	0.5 mA Source
	V (In Low)	-	-	0.5	volts	
	V (In High)	V_{DD} -2.0	-	-	volts	
Clock Buffer (X358)	V (Out Low)	-	-	0.5	volts	1.0 mA, 20 pF
	V (Out High)	V_{DD} -0.5	-	-	volts	1.0 mA, 20 pF
	Duty Cycle	40	-	60	percent	C = 20 pF
3-State Operation	Enable Time	-	200	250	ns	C = 50 pF
	Disable Time	-	200	250	ns	R = 100 kohm
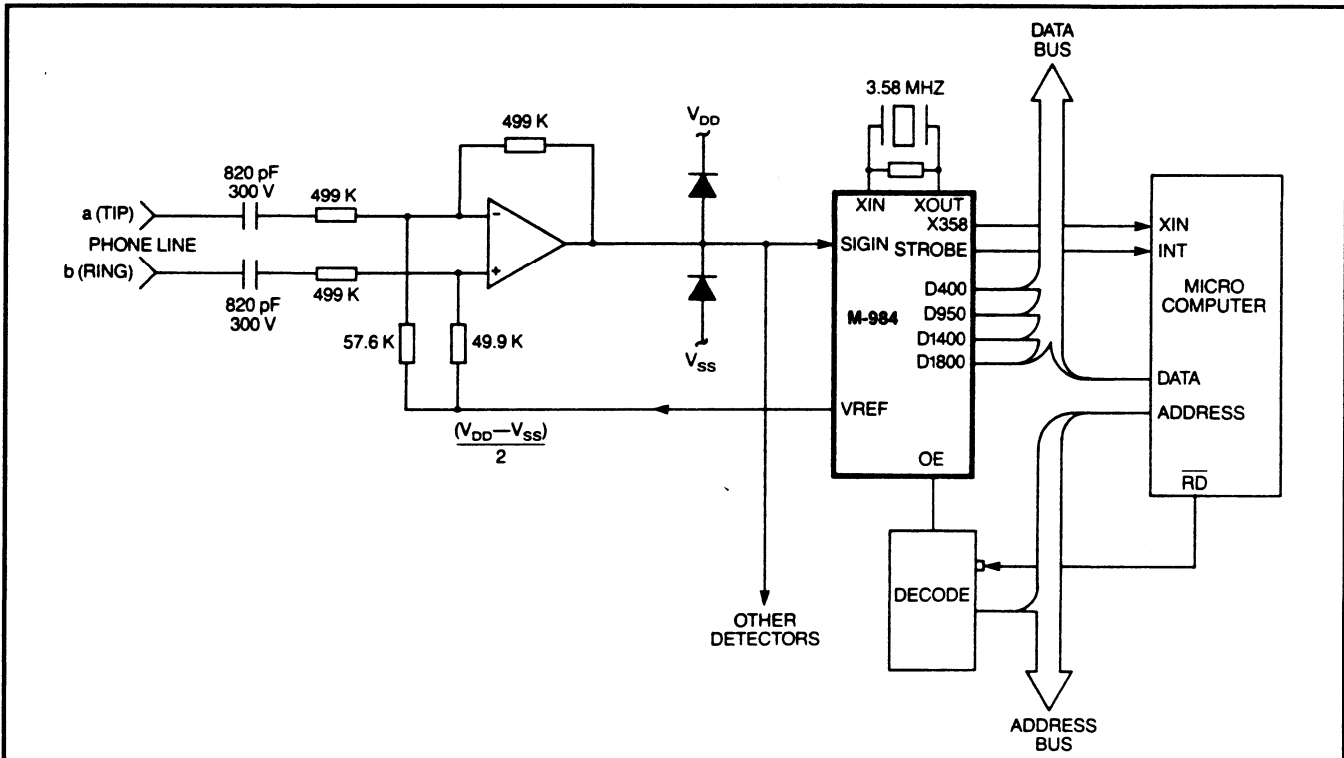
Figure 4 Typical Application

Teltone Corporation / 10801-120th Avenue NE, Kirkland, WA 98033   Phone: 1-800-426-3926 or 206-827-9626   Fax: 206-827-6050   TWX: 910-449-2862
Teltone Limited / 3375-14th Avenue, Markham, Ontario, Canada L3R 2L6   Phone: 416-475-0837   Fax: 416-474-9151   Envoy User Name: TTL.HQ

4-17
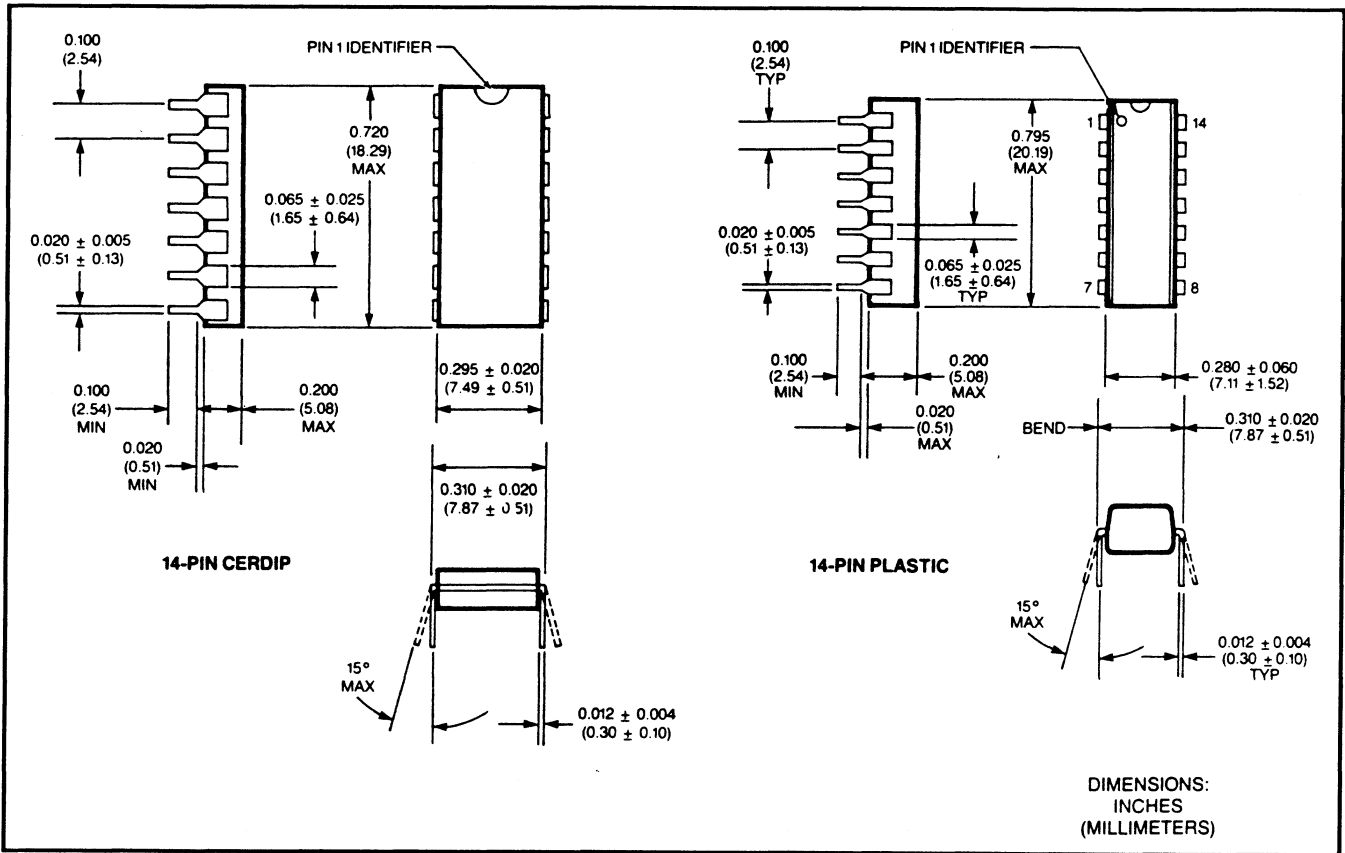
Figure 5 Package Dimensions

Table 3 Detector Frequency Windows

Window	Pin	Low Reject	Low Accept	High Accept	High Reject
1	D400	363	392	459	493
2	D950	845	895	1005	1060
3	D1400	1290	1343	1457	1512
4	D1800	1675	1741	1812	1882

Table 4 Absolute Maximum Ratings

DC Supply Voltage. . . . . 7.0 V
Voltage on Any Pin. . . . . $V_{DD} + 0.5$ to $V_{ss} - 0.5V$
Storage Temperature Range. . . . . 0° C to +70° C
Storage Temperature Range. . . . . −40° C to +85° C
Lead Soldering Temperature. . . . . 260° C for 5 seconds

M-991 CALL PROGRESS TONE GENERATOR

The Teltone® M-991 is an integrated circuit call progress tone generator for use in telephone systems. The circuit uses low-power CMOS techniques to generate tones which are digitally controlled and highly linear. The M-991 is designed to permit operation with almost any system.

The use of integrated circuit techniques allows the M-991 to incorporate the control, tone generating, and power output buffer into a single 14-pin DIP. A 3.58-MHz (color burst) crystal-controlled time base guarantees accuracy and repeatability.

Features
- Generates standard call progress tones
- Digital input control
- Linear (analog) output
- Power output capable of driving standard line
- 14-pin DIP
- Single supply 4B CMOS (low power)
- Inexpensive 3.58-MHz time base

Applications
- Telephone systems
- Test equipment
- Callback security systems
- Billing systems
- Audible alert systems
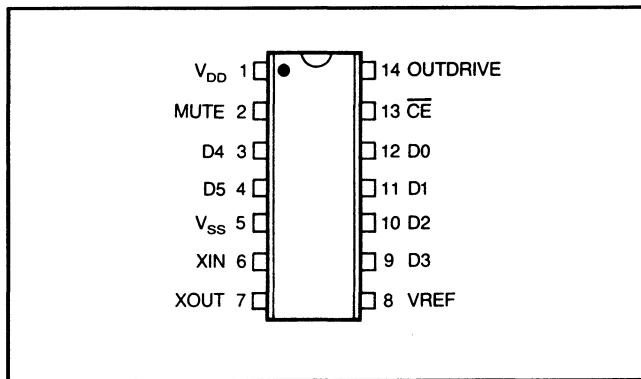
Figure 1 Pin Diagram
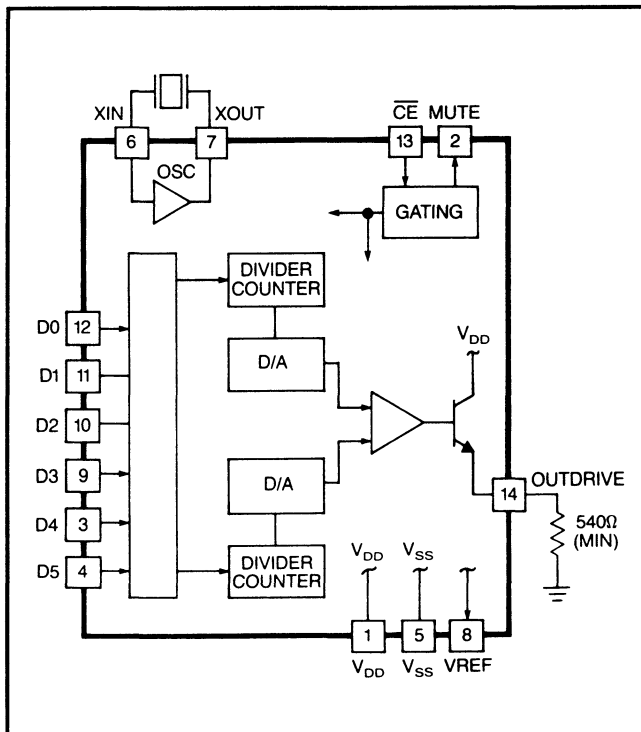
Figure 2 Block Diagram
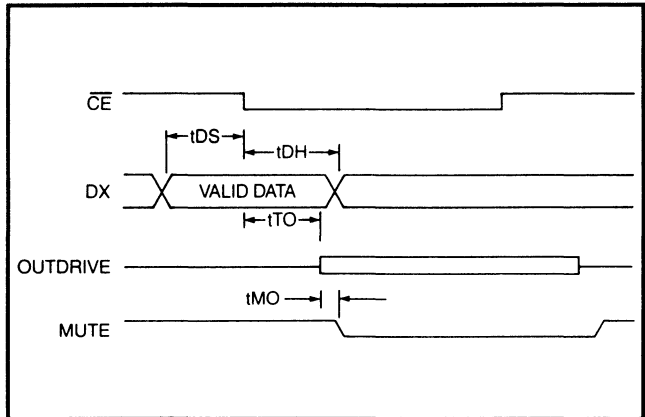
Figure 3 Timing Diagram
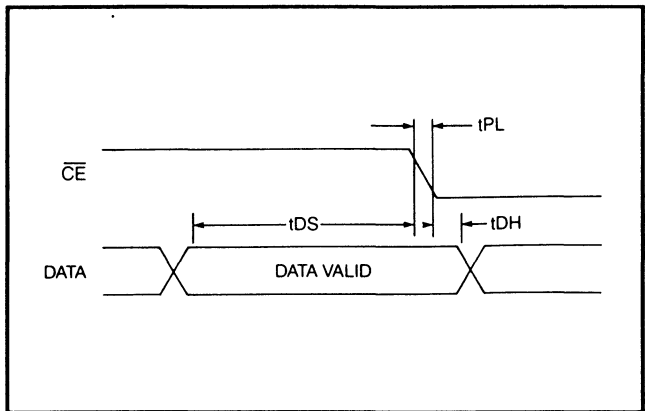
Figure 4 Expanded Wire Data Timing Diagram

Call Progress Tone Generation

Call progress tones are audible tones sent from switching systems to calling parties (or equipment) to show the status of calls. Calling parties can identify the success of a placed call by what is heard after dialing.

The M-991 is a highly linear tone generator that produces the unique frequencies (singly or in pairs) that are common to call progress signals. Duration and frequency selection are digitally controlled (see Table 2 for data settings for a particular tone output). A typical control sequence for the M-991 is: (1) set data lines to desired frequency selection, (2) wait for data lines to settle, (3) drive the chip enable ($\overline{CE}$) low, (4) maintain $\overline{CE}$ low for desired tone duration (Note: data lines may be changed after data hold time), and (4) return $\overline{CE}$ to a logic high.

The commonly used call progress tones are shown in Table 3.

Table 1 Pin Functions

PIN	FUNCTION
$\overline{CE}$	Latches data and enables output (active low input).
D0 - D5	Data input pins. (See Table 2).
MUTE	Output indicates that a signal is being generated at OUTDRIVE.
OUT-DRIVE	Linear buffered tone output.
V_{DD}	Most positive power supply input pin.
VREF	Internally generated mid-power supply voltage (output).
V_{SS}	Most negative power supply input pin.
XIN	Crystal oscillator or digital clock input.
XOUT	Crystal oscillator output.

Table 2 Data/Tone Selection

D3	D2	D1	D0	FREQUENCY (Hz) 1	FREQUENCY (Hz) 2	USE
0	0	0	0	350	440	Dial tone
0	0	0	1	400	Off	Special
0	0	1	0	440	Off	Alert Tone
0	0	1	1	440	480	Audible Ring
0	1	0	0	440	620	Pre-empt
0	1	0	1	480	Off	Bell high tone
0	1	1	0	480	620	Reorder (Bell low)
0	1	1	1	350	Off	Special
1	0	0	0	620	Off	Special
1	0	0	1	941	1209	DTMF "*"

Note: D4, D5 reserved for future use and default to inactive when left open.

Table 3 Standard Call Progress Tones

TONE NAME	FREQUENCY (Hz) 1	FREQUENCY (Hz) 2	INTERRUPTION RATE
Dial	350	440	Steady
Reorder	480	620	Repeat, tones on and off 250 ms ± 25 ms each
Busy	480	620	Repeat, tones on and off 500 ms ± 50 ms each
Audible Ring	440	480	Repeat, tones on 1 ± 0.2 s; tones off 3 ± 0.3 s
Recall Dial	350	440	Three bursts tones on and off 100 ms ± 20 ms each followed by dial tone
Special AR	440	480	Tones on 1 ± 0.2 s, followed by single 440 Hz on for 0.2 s on, and silence for 3 ± 0.3 s, repeat
Intercept	440	620	Repeat alternating tones, each on for 230 ms ± 70 ms with total cycle of 500 ± 50 ms
Call Waiting	440	Off	One burst 200 ± 100 ms
Busy Verification	440	Off	One burst of tone on 1.75 ± 0.25 s before attendant intrudes, followed by burst of tone 0.65 ± 0.15 s on, 8 to 20 s apart for as long as the call lasts
Executive Override	440	Off	One burst of tone for 3 ± 1 s before overriding station intrudes
Confirmation	350	440	Three bursts on and off 100 ± 20 ms each

Abbreviations: Hz = hertz, ms = milliseconds, s = seconds

Table 4 Specifications

Unless otherwise noted, $V_{DD} - V_{SS} = 5VDC$, Ta = 25°C

PARAMETER		MIN	TYP	MAX	UNITS	NOTES
Power Supply and Reference	V_{DD}	4.75	—	5.25	V	1
	Current Drain, IDD	—	—	30	mA	8
	VREF Pin: Deviation from $(V_{DD} + V_{SS})/2$	−2	—	+2	%	
	Internal Resistance from VREF to V_{DD}, V_{SS}	3.25	—	6.75	Kohms	
Oscillator	Frequency Deviation	−0.01	—	+0.01	%	7
	External Clock: (XOUT open) VIL	0	—	0.2	V	
	VIH	$V_{DD} - 0.2$	—	V_{DD}	V	
	Duty Cycle	40	—	60	%	
	XIN, XOUT Loading: Capacitance	—	—	10	pF	10
	Resistance	20	—	—	Mohms	
Tone Output	Frequency Deviation	−0.5	—	+0.5	%	
	Level	110	—	180	mV	2
	Distorting Components	−35	—	—	dB	3
	Idle	—	—	−60	dBm	4
	OUTDRIVE Envelope Rise Time	—	—	4	ms	5
Control	DX, $\overline{CE}$ Pins: VIL	—	—	0.5	V	6
	VIH	2.5	—	—	V	
	Mute Pins: VOL (ISINK = −100 µA)	—	—	1.5	V	
	VOH (ISOURCE = 100 µA)	$V_{DD} - 1.5$	—	—	V	
Timing	Data Setup (tDS)	200	—	—	ns	
	Data Hold (tDH)	10	—	—	ns	
	Chip Enable Fall (tPL)	—	—	90	ns	11
	Tone On Delay (tTO)	—	—	5	ms	
	Tone Off Delay (tTD)	—	—	5	ms	
	Mute Delay from Outdrive (tMO)	—	—	200	ns	

Notes: (unless otherwise specified)

1. All DC voltages are referenced to V_{SS}.
2. Vrms per tone, 540 ohm load.
3. Any one frequency relative to the lowest level output tone (f < 4000 Hz).
4. 0 dBm = 0.775 Vrms.
5. To 90% maximum amplitude.
6. For all supply voltages in the operating range.
7. At XOUT pin as compared to 3.579545 MHz.
8. OUTDRIVE inactive.
9. Resistance at VREF to V_{DD} or V_{SS} >1 Mohm.
10. Crystal oscillator active.
11. Measured 90% to 10%.

Figure 5 Package Dimensions

Table 5 Absolute Maximum Ratings (Note 1)

Storage Temperature . . . . -55 to $125\,°C$
Operating Ambient Temperature. . . . . -25 to $70\,°C$
V_{DD} . . . . $7.0V$
Any Input Voltage . . . . $V_{SS} -0.6$ to $V_{DD} +0.6V$

Note:

1. Exceeding these ratings may permanently damage the M-991.

MF Trunk Receivers and Transmitters

M-986-1R1 AND -2R1 MFC TRANSCEIVERS

M-986-1R1 and -1R2 are now available.

Call Teltone for complete data sheet.

Teltone M-986-1R1 and -2R1 MF Transceivers contain all the logic necessary to transmit and receive R1 multifrequency signals on one 40-pin integrated circuit (IC). M-986-1R1 is a single-channel version; M-986-2R1 provides two channels. CCITT R2 single and dual multifrequency transceivers are also available as M-986-1R2 and -2R2.

With the addition of only a 20.48 MHz crystal, the M-986 is capable of providing a direct digital interface to an audio source. With a 20.48 MHz crystal as well as a coder-decoder (codec) connected to each channel as shown in Figure 1, the M-986 provides an analog interface.

μ-law is used for coding/decoding. The M-986 is configured and controlled through an integral coprocessor port.

Features

- Direct μ-Law PCM digital input
- 2.048 Mb/s clocking
- Operates with standard codecs for analog interfacing
- Microprocessor read/write interface
- Binary or 2-of-6 data formats
- Single- or dual-channel versions
- 5 volt power

Applications

- Test equipment
- Trunk adapters
- Paging terminals
- Traffic recorders
- PBXs
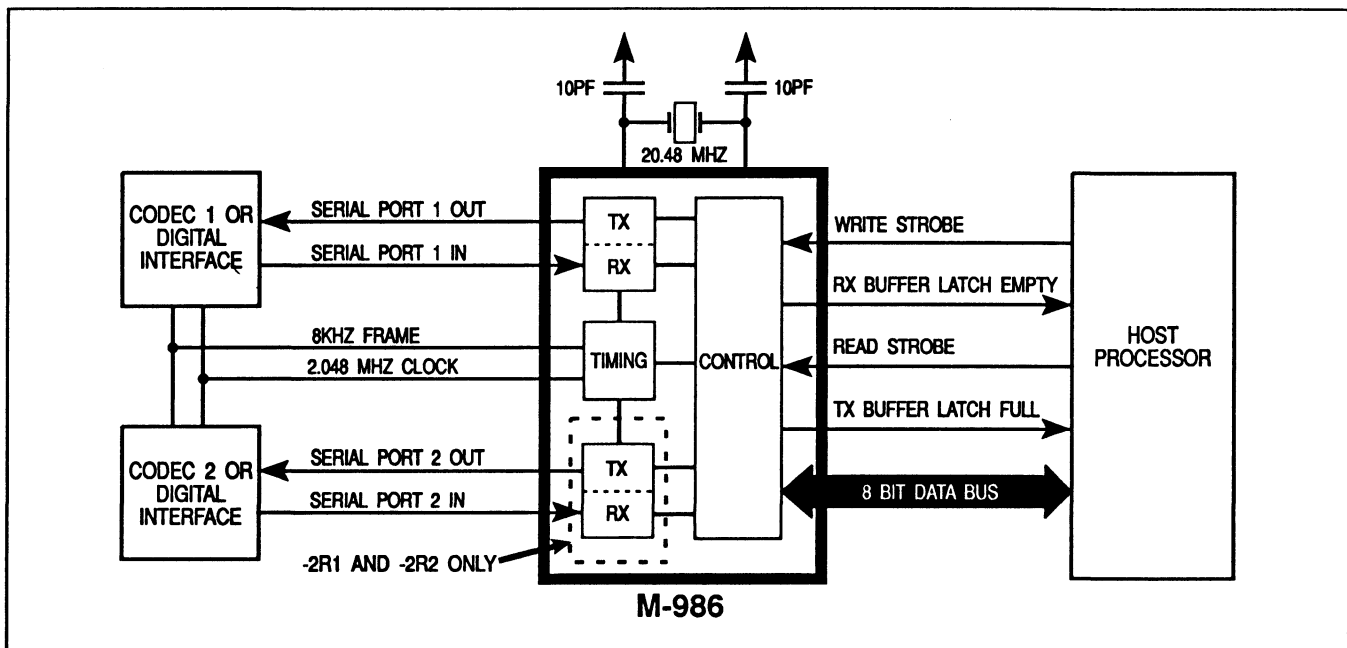
Figure 1 Block Diagram

M-986-1R2 AND -2R2 MFC TRANSCEIVERS

Teltone M-986-1R2 and -2R2 MFC Transceivers contain all the logic necessary to transmit and receive CCITT R2F (forward) and R2B (backward) multifrequency signals on one 40-pin integrated circuit (IC). M-986-1R2 is a single-channel version; M-986-2R2 provides two channels. R1 single and dual multifrequency transceivers are also available as M-986-1R1 and -2R1.*

With the addition of only a 20.48 MHz crystal, the M-986 is capable of providing a direct digital interface to an audio source. With a 20.48 MHz crystal as well as a coder-decoder (codec) connected to each channel as shown in Figure 1, the M-986 provides an analog interface.

The M-986 can be configured by the customer to operate with the transmitter and receiver either coupled together or independent, allowing it to handle a compelled cycle automatically or via command from the host processor. A-law is used for coding/decoding. The M-986 is configured and controlled through an integral coprocessor port.

*as of November 1990.

Features

- Direct A-Law PCM digital input
- 2.048 Mb/s clocking
- Programmable forward/backward mode
- Programmable compelled/direct control
- Operates with standard codecs for analog interfacing
- Microprocessor read/write interface
- Binary or 2-of-6 data formats
- Single- or dual-channel versions
- 5 volt power

Applications

- Test equipment
- Trunk adapters
- Paging terminals
- Traffic recorders
- PBXs
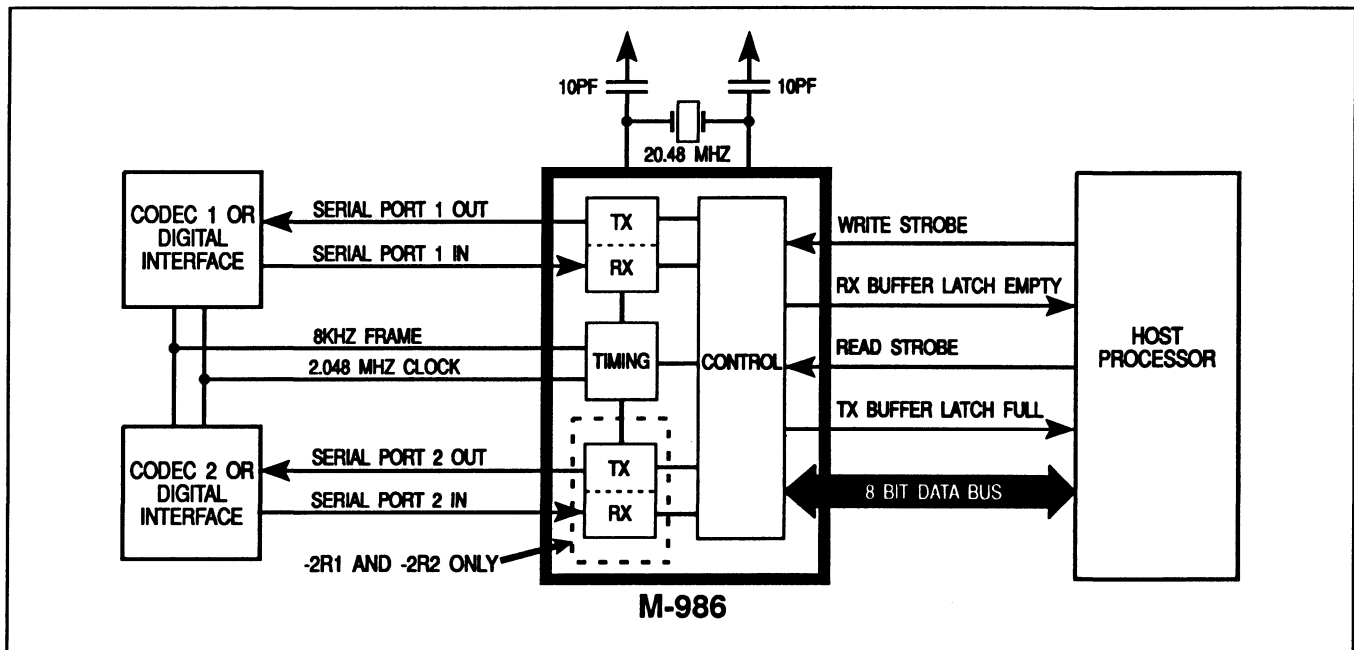
Figure 1   Block Diagram

Functional Description

The M-986 can be configured for various operational characteristics by writing two configuration bytes to the coprocessor port. The format of the two configuration bytes is shown in Table 1 and the configuration options are described in the following paragraphs.

Configuration Options

External/Internal Codec Clock (ECLK): If external codec clocking is selected, an external clocking source provides an 8kHz transmit framing clock, an 8kHz receive framing clock, and a serial bit clock that is a multiple of 8 kHz between 2.496 MHz and 216 kHz for exchange of data via the serial ports. When internal codec clocking is selected, the M-986 provides an 8kHz framing clock and a 2.048 MHz serial bit clock.

Binary/2 of 6 Input/Output (IOM): When 2-of-6 input/output is selected, the M-986 outputs data to the coprocessor port in a 6-bit format, where each bit represents one of the six possible frequencies. A logic high level indicates the presence of a frequency. Input to the M-986 for selecting the transmitted R2 MF tone must also be coded in the 2-of-6 format. See Table 2.

When binary input/output is selected, the M-986 outputs data to the coprocessor port that codes the received R2 MF tone into a 4 bit binary format. Input to the M-986 for selecting the transmitted R2 MF tone must also be coded in a 4 bit binary format. See Table 3.

Enable/Disable Channel (ENC): When a channel is disabled, the receiver does not process its codec input for R2 MF tones, and the transmitter transmits its "tone off" pattern. The serial port clock and the frame clock continue to function. When a channel is enabled, the receiver and transmitter for that channel function normally.

End-of-Digit Indication (EOD): The end-of-digit indication option configures the M-986 to inform the host processor when the far end terminates transmission of the R2 MF tone it is sending. If this option is disabled, the host processor will not be notified when tone transmission terminates.

Automatic Compelled/Manual Sequence Signaling (CMP): When manual mode is selected, R2 MF tone transmission is turned on and off only via command from the host processor.

If the automatic mode is selected, the transmitter and receiver perform the compelled signaling handshake automatically. The specifics of operation are different for the forward and backward configurations.

Table 1 Configuration Bytes

CONFIGURATION BYTE 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	ECLK	IOM	ENC1	EOD1	CMP1	FB1

ECLK	Channels 1 & 2	1 = External codec clock; 0 = Internal codec clock
IOM	Channels 1 & 2	1 = Binary input/output; 0 = 2-of-6 input/output
ENC1	Channel 1	1 = Enable channel; 0 = Disable channel
EOD1	Channel 1	1 = Indicate end of digit; 0 = No end of digit indication
CMP1	Channel 1	1 = Automatic compelled mode; 0 = Manual mode
FB1	Channel 1	1 = Forward mode (Tx forward frequencies and Rx backward frequencies) 0 = Backward mode (Tx backward frequencies and Rx forward frequencies)

CONFIGURATION BYTE 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	ENC2	EOD2	CMP2	FB2

ENC2	Channel 2	1 = Enable channel; 0 = Disable channel
EOD2	Channel 2	1 = Indicate end of digit; 0 = No end of digit indication
CMP2	Channel 2	1 = Automatic compelled mode; 0 = Manual mode
FB2	Channel 2	1 = Forward mode (Tx forward frequencies and Rx backward frequencies) 0 = Backward mode (Tx backward frequencies and Rx forward frequencies)
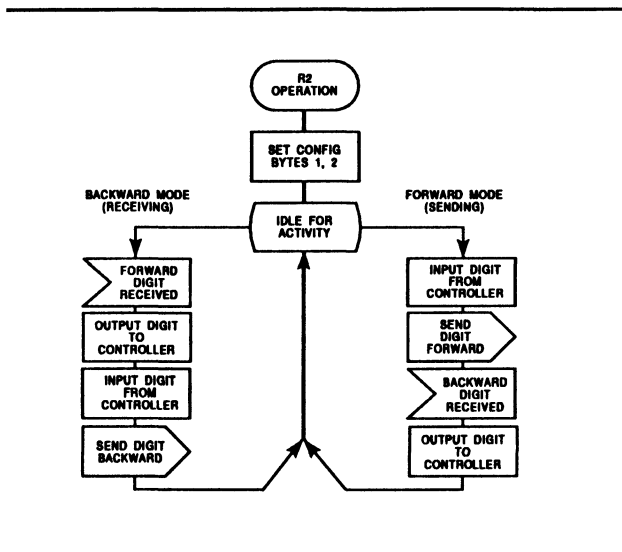
In forward mode, the transceiver can exist in two states, STATE 1 and STATE 2:

. STATE 1: No backward signal detected.
Transmitter under control of the host.

. STATE 2: Backward signal detected.
Transmitter off unconditionally.

A Transmit Tone Command written while the transceiver is in STATE 1 will be acted upon immediately. The transmitter is unconditionally disabled upon entry into STATE 2. If a transmit command is written to the transceiver while in STATE 2, that command will become pending. Upon entry into STATE 1, a pending transmit command is acted upon.

In backward mode, the transceiver can exist in two states, STATE 1 and STATE 2:

. STATE 1: No forward signal detected.
Transmitter off unconditionally.
. STATE 2: Forward signal detected.
Transmitter transmits backward signal.

Table 2   2 of 6 Coding Format

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit tone command	1	CHN	F6	F5	F4	F3	F2	F1
Receive tone return	0	CHN	F6	F5	F4	F3	F2	F1

CHN: 1 = channel 2;   0 = channel 1
R2 MF Frequencies:

Bit name	Forward (Hz)	Backward (Hz)	Bit name	Forward (Hz)	Backward (Hz)
F6	1980	540	F3	1620	900
F5	1860	660	F2	1500	1020
F4	1740	780	F1	1380	1140

Table 3   Binary Coding Format

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit tone command	1	CHN	0	0	A	B	C	D
Receive tone return	0	CHN	0	0	A	B	C	D

CHN: 1 = channel 2;   0 = channel 1
R2 MF Frequencies:

ABCD	Forward (Hz)	Backward (Hz)	ABCD	Forward (Hz)	Backward (Hz)
0 0 0 0	Tone off	Tone off	1 0 0 0	1500 & 1860	1020 & 660
0 0 0 1	1380 & 1500	1140 & 1020	1 0 0 1	1620 & 1860	900 & 660
0 0 1 0	1380 & 1620	1140 & 900	1 0 1 0	1740 & 1860	780 & 660
0 0 1 1	1500 & 1620	1020 & 900	1 0 1 1	1380 & 1980	1140 & 540
0 1 0 0	1380 & 1740	1140 & 780	1 1 0 0	1500 & 1980	1020 & 540
0 1 0 1	1500 & 1740	1020 & 780	1 1 0 1	1620 & 1980	900 & 540
0 1 1 0	1620 & 1740	900 & 780	1 1 1 0	1740 & 1980	780 & 540
0 1 1 1	1380 & 1860	1140 & 660	1 1 1 1	1860 & 1980	660 & 540

A transmit tone command written while the transceiver is in STATE 2 will be acted upon immediately. The transmitter is unconditionally disabled upon entry into STATE 1. If a transmit command is written to the transceiver while in STATE 1, that command will become pending. Upon entry into STATE 2, a pending transmit command is acted upon.

EXAMPLE: Assume that the transceivers at both ends of a link are configured in automatic compelled mode. Both transceivers are in STATE 1. A compelled signaling sequence begins with the R2F host writing a transmit command byte to its transceiver via the coprocessor bus. The transceiver immediately begins transmitting the signal.

The R2B transceiver detects the signal, enters STATE 2, and outputs the received tone code to its host via the coprocessor port. If the R2B host had determined the next tone to transmit and written a transmit command to the transceiver prior to entry into STATE 2, the state transition will cause this tone to be transmitted. Otherwise, the R2B transmitter waits for a transmit tone command from the host, and starts transmitting a tone once the transmit tone command is received.

The R2F transceiver detects the backward signal, enters STATE 2, and outputs the received tone code to its host. Entry into STATE 2 unconditionally disables the transmitter.

The R2B transceiver detects the absence of signal, enters STATE 1, and informs the host with the end-of-tone code if configured to do so. Entry into STATE 1 unconditionally disables the transmitter.

The R2F transceiver detects the absence of signal, enters STATE 1, and informs the host with the end-of-tone code if configured to do so. If the R2F host had determined the next signal to transmit and written a transmit command to the transceiver prior to entry into STATE 1, the state transition will cause this signal to be transmitted. Otherwise, the transmitter remains silent until the next transmit command by its host.

Forward/Backward Frequencies (FB): When forward mode is selected, the R2F (forward) frequencies are transmitted and R2B (backward) frequencies are received. When backward mode is selected, R2B frequencies are transmitted and R2F frequencies are received. The R2F frequencies are 1380, 1500, 1620, 1740, 1860, and 1980 Hertz. The R2B frequencies are 540, 660, 780, 900, 1020, and 1140 Hz.

Initial Configuration: The configuration of the M-986 immediately after a reset will be as follows:
- End-of-digit indication ON
- Forward mode ON
- Channel disabled
- 2-of-6 input/output
- External serial and serial frame clocks.

Also, the M-986 will place 00 hex on the coprocessor port to indicate to the host processor that it is working.

Transmit Tone Command

The transmit tone command allows the host processor to transmit any two of the 6 possible frequencies in the transmission mode the channel has been configured for (forward or backward). The format of the command depends on whether the M-986 is configured for binary format or 2-of-6 format. See Tables 2 and 3.

Received Tone Detection

When a tone is detected by the M-986, the $\overline{TBLF}$ output goes low, indicating reception of the tone to the host processor. The host processor can determine which tone was detected and which channel the tone was detected on by reading data from the M-986 coprocessor port. The M-986 will return a single byte indicating the tone received and the channel that the tone was received on.The format of the returned byte depends on whether the M-986 is configured for binary or 2-of-6 coding. See Tables 2 and 3.

Coprocessor Port

Commands are written to the M-986 via the coprocessor port, and data indicating the received R2 MF tone is read from the coprocessor port.

Writing to the Coprocessor Port: The following sequence describes writing a command to the M-986.

(1) The $\overline{WR}$ signal is driven low by the host processor.

(2) The $\overline{RBLE}$ (receive buffer latch empty) signal transitions to a logic high level.

(3) Data is written from LD7-LD0 to the receive buffer latch (D7-D0) when the $\overline{WR}$ signal goes high.

(4) The $\overline{RBLE}$ signal transitions to a logic low level after the M-986 reads the data. This signals the host processor that the receive buffer is empty.

Note: The RBLE should be low before writing to the coprocessor.

*Reading the Coprocessor Port:*The following sequence describes reading received tone information from the coprocessor port.

(1) The $\overline{TBLF}$ (transmit buffer latch full) port pin on the M-986 goes low indicating the reception of a tone.

(2) The host processor detects the low logic level on the $\overline{TBLF}$ pin either by polling a connected port pin or by an interrupt.

(3) The host processor drives the $\overline{RD}$ signal low.

(4) The $\overline{TBLF}$ (transmit buffer latch full) signal transitions to a logic high level.

(5) Data is driven onto LD7-LD0 by the M-986 until the $\overline{RD}$ signal is driven high by the host processor.

Table 4 Signal Descriptions

SIGNAL	PIN	I/O/Z	DESCRIPTION
D15-D8	18-11	I/O/Z	Unused. Leave open.
D7-D0	19-26	I/O/Z	8-bit coprocessor latch.
$\overline{\text{TBLF}}$	40	O	Transmit buffer latch full flag.
$\overline{\text{RBLE}}$	1	O	Receive buffer latch empty flag
HI/$\overline{\text{LO}}$	2	I	Latch byte select pin. Tie low.
$\overline{\text{BIO}}$	9	I	Unused. Leave open.
$\overline{\text{RD}}$	32	I/O	Used by the external processor to read from the coprocessor latch by driving the $\overline{\text{RD}}$ line active (low), thus enabling the output latch to drive the latched data. When the data has been read, the external device must bring the $\overline{\text{RD}}$ line high.
$\overline{\text{EXINT}}$	5	I	Unused. Leave open.
MC	3	I	Microcomputer mode select pin. Tie low.
MC/$\overline{\text{PM}}$	27	I	Coprocessor mode select pin. Tie low.
$\overline{\text{RS}}$	4	I	Reset input for initializing the device. When an active low is placed on $\overline{\text{RS}}$ pin for a minimum of five clock cycles, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are forced high, and the data bus (LD7 through LD0) goes to a high impedance state. The serial port clock and transmit outputs also go to the high impedance state.
$\overline{\text{WR}}$	31	I/O	Used by the external processor to write data to the coprocessor port. To write data the external processor drives the $\overline{\text{WR}}$ line low, places data on the data bus, and then drives the $\overline{\text{WR}}$ line high to clock the data into the on-chip latch.
XF	28	O	Watchdog signal. Toggles at least once every 10 milliseconds when the processor is functioning properly.
CLKOUT	6	O	System clock output (one-fourth crystal/CLKIN frequency, nominally 5.12 MHz).
Vcc	30	I	5V supply pin.
Vss	10	I	Ground pin.
X1	7	O	Crystal output pin for internal oscillator. If an internal oscillator is not used, this pin should be left unconnected.
X2/CLKIN	8	I	Input pin to the internal oscillator (X2) from the crystal. Alternatively, an input pin for the external oscillator (CLKIN).
DR1 & DR0	33 & 29	I	Serial-port receive-channel inputs. 2.048 MHz serial data is received in the receive registers via these pins.
DX1 & DX0	36 & 35	O	Serial-port transmit-channel outputs. 2.048 MHz serial data is transmitted from the transmit registers on these pins. These outputs are in the high-impedance state when not transmitting.
FR	37	O	8 kHz internal serial-port framing output. If internal clocking is selected, serial-port transmit and receive operations occur simultaneously on an active (high) FR framing pulse.
/FSR	39	I	8 kHz external serial-port receive-framing input. If external clocking is selected, data is received via the receive pins (DR1 and DR0) on the active (low) FSR input. The falling edge of FSR initiates the receive process, and the rising edge causes an interrupt.
/FSX	38	I	8 kHz external serial-port transmit-framing input. If external clocking is enabled, data is transmitted on the transmit pins (DX1)
SCLK	34	I/O/Z	2.048 MHz serial-port clock. Master clock for transmitting and receiving serial-port data. Configured as an input in external clocking mode or output in internal clocking mode. Reset ($\overline{\text{RS}}$) forces SCLK to the high-impedance state.

Clock Characteristics and Timing

Internal Clock Option: The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN. The crystal must be 20.48 MHz, fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pf.

External Clock Option: An external frequency source can be used by injecting the frequency directly in X2/CLKIN, with X1 left unconnected. The external frequency injected must conform to the specifications listed in Table 8.

Flammability/Reliability Specifications

Reliability: 185 FITS failures/billion hours
Flammability: Passes UL 94 V-0 tests

Ordering Information

M-986-1 R 2 C

1 or 2 channels
CCITT SYSTEM R1 or R2
P = plastic; C = ceramic; F = flat pack
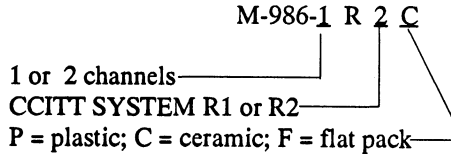
Table 5   Absolute Maximum Ratings Over Specified Temperature Range

Supply voltage range, V_{CC}	-0.3 V to 7 V
Input voltage range	-0.3 V to 15 V
Output voltage range	-0.3 V to 15 V
Ambient air temperature range	0 ° C to 70 ° C
Storage temperature range	-45 ° C to 150 ° C

Table 6   Recommended Operating Conditions

Parameter		Min	Nom	Max	Unit
V_{CC} Supply voltage	EPROM version	4.75	5	5.25	V
V_{CC} Supply voltage	All other versions	4.5	5	5.5	V
V_{SS} Supply voltage			0		V
V_{IH} High-level input voltage	All inputs except CLKIN	2			V
	CLKIN	3			V
V_{IL} Low-level input voltage	All inputs except MC/$\overline{MP}$			0.8	V
	MC/$\overline{MP}$			0.6	V
I_{OH} High-level output current (all outputs)				-300	μA
I_{OL} Low-level output current (all outputs)				2	mA


```
RBLE    [ 1   U  40 ]  TBLF
HI/LO   [ 2      39 ]  FSR
MC      [ 3      38 ]  FSX
RS      [ 4      37 ]  FR
EXINT   [ 5      36 ]  DX1
CLKOUT  [ 6      35 ]  DXO
X1      [ 7      34 ]  SCLK
X2/CLKIN[ 8      33 ]  DR1
BIO     [ 9      32 ]  RD
VSS     [ 10     31 ]  WR
D8      [ 11     30 ]  VCC
D9      [ 12     29 ]  DRO
D10     [ 13     28 ]  XF
D11     [ 14     27 ]  PM
D12     [ 15     26 ]  DO
D13     [ 16     25 ]  D1
D14     [ 17     24 ]  D2
D15     [ 18     23 ]  D3
D7      [ 19     22 ]  D4
D6      [ 20     21 ]  D5
```
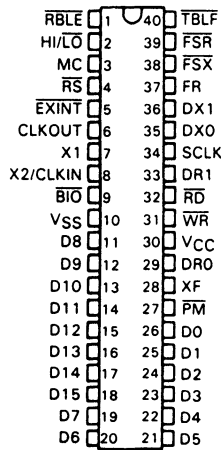
Figure 3   Pin Assignments
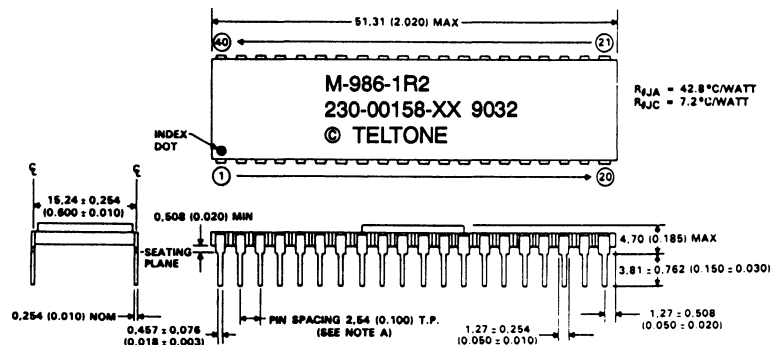
Figure 4   Package Dimensions

Table 7 Electrical Characteristics Over Specified Temperature Range

Parameter	Test Conditions		Min	Typ	Max	Unit
I_{CC} Supply current	f = 20.5 MHz, V_{CC} = 5.5V, T_A = 0 ° to 70 ° C			50	75	mA
V_{OH} High-level output voltage	I_{OH} = MAX		2.4	3		V
	I_{OH} = 20 μA		V_{CC} -0.4			V
V_{OL} Low-level output voltage	I_{OL} = MAX			0.3	0.5	V
I_{OZ} Off-state output current	V_{CC} = MAX	V_O = 2.4 V			20	μA
		V_O = 0.4 V			-20	μA
I_I Input current	V_I = V_{SS} to V_{CC}	Except CLKIN			±20	μA
					±20	μA

Table 8 External Frequency Specifications

Parameter	Min	Nom	Max	Unit
$t_{C(MC)}$ Master clock cycle time	48.818	48.828	48.838	ns
$t_{r(MC)}$ Rise time master clock input		5	10	ns

Table 9 Serial Port Timing

Parameter	Min	Nom	Max	Unit
t_d (CH-FR) Internal framing delay from SCLK rising edge			70	ns
t_d (DX1-CL) DX bit 1 valid before SCLK falling edge	20			ns
t_d (DX2-CL) DX bit 2 valid before SCLK falling edge	20			ns
t_h (DX) DX hold time after SCLK falling edge	244			ns
t_{su} (DR) DR setup time before SCLK falling edge	20			ns
t_h (DR) DR hold time after SCLK falling edge	20			ns
t_c (SCLK) Serial port clock cycle time	399	488.28	4770	ns
t_f (SCLK) Serial port clock fall time			30	ns
t_r (SCLK) Serial port clock rise time			30	ns
t_w (SCLKL) Serial port clock low-pulse duration	220	244.14	268	ns
t_w (SCLKH) Serial port clock high-pulse duration	220	244.14	268	ns

Table 10 Coprocessor Interface Timing

Parameter	Min	Nom	Max	Unit
$t_{d(R-A)}$ $\overline{RD}$ low to $\overline{TBLF}$ high			75	ns
$t_{d(W-A)}$ $\overline{WR}$ low to $\overline{RBLE}$ high			75	ns
$t_{a(RD)}$ $\overline{RD}$ low to data valid			80	ns
$t_{h(RD)}$ Data hold time after $\overline{RD}$ high	50			ns
$t_{su(WR)}$ Data setup time prior to $\overline{WR}$ high	30			ns
$t_{h(WR)}$ Data hold time after $\overline{WR}$ high	25			ns
$t_{w(RDL)}$ $\overline{RD}$ low-pulse duration	80			ns
$t_{w(WRL)}$ $\overline{WR}$ low-pulse duration	60			ns
$t_{wr(RBLE)}$ $\overline{RBLE}$↑ to $\overline{RBLE}$↓			1	ms

Table 11 Reset (RS) Timing

Parameter	Test Conditions	Min	Max	Unit
$t_{dis(R)}$ Data bus disable time after $\overline{RS}$	$R_L = 825\ \Omega$ $C_L = 100\ pF$		75	ns
t_{d12} Delay time from $\overline{RS}\downarrow$ to high-impedance SCLK			200	ns
t_{d13} Delay time from $\overline{RS}\downarrow$ to high-impedance DX1, DX0			200	ns
$t_{su(R)}$ Reset $(\overline{RS})$ setup time prior to CLKOUT		50		ns
$t_{w(R)}$ $\overline{RS}$ pulse duration		245		ns

Table 12 CLKOUT Timing Parameters

Parameter	Test Conditions	Min	Nom	Max	Unit
$t_{c(C)}$ CLKOUT cycle time	$R_L = 825\ \Omega$ $C_L = 100\ pF$	195.27	195.31	195.35	ns
$t_{r(C)}$ CLKOUT rise time			10		ns
$t_{f(C)}$ CLKOUT fall time			8		ns
$t_{d(MCC)}$ Delay time CLKIN↑ to CLKOUT↓		25		60	ns

Table 13 Transmitter Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
F_{OS} Frequency offset	From nominal			±1	Hz
TW Twist	High/low			±0.5	dB
A_S Signal amplitude	Per component	-9.26	-8.86	-8.46	dBm0
T_S Time skew	Between components			0	ms
P_{hi} Power due to harmonic distortion and intermodulation	300 to 3400 Hz			-46.5	dBm0

Table 14 Receiver Characteristics

Parameter	Test Conditions	Min	Max	Unit
A_d Detect amplitude	Per frequency	-35	-5	dBm0
A_{nd} No-detect amplitude	Per frequency	-42	-35	dBm0
F_d Detect with frequency offset	From nominal	±10		Hz
TW_d Detect with twist	Adjacent frequencies	±5		dB
	Nonadjacent frequencies	±7		dB
TW_{nd} No detect with twist		±20		dB
$T3_r$ Third R2F tone reject	Relative to highest level frequency	-20		dB
FF_d Detect R2B with R2F disturbing	Above lowest level R2B tone (-12.5 dBm0 max.)	13.5		dB
FT_{nd} No detect R2F with 2 out-of-band sine waves	Any frequencies from 330 - 1150 Hz and 2130 - 3400 Hz	-5		dBm0
RT_{nd} No detect R2B with 2 out-of-band sine waves	Any frequencies from 1300-3400 Hz	-5		dBm0
T_{on} Tone time	Reject	7		ms
T_{int} Interrupted tone time	Reject	7		ms
T_{or} Operate and release time			80	ms
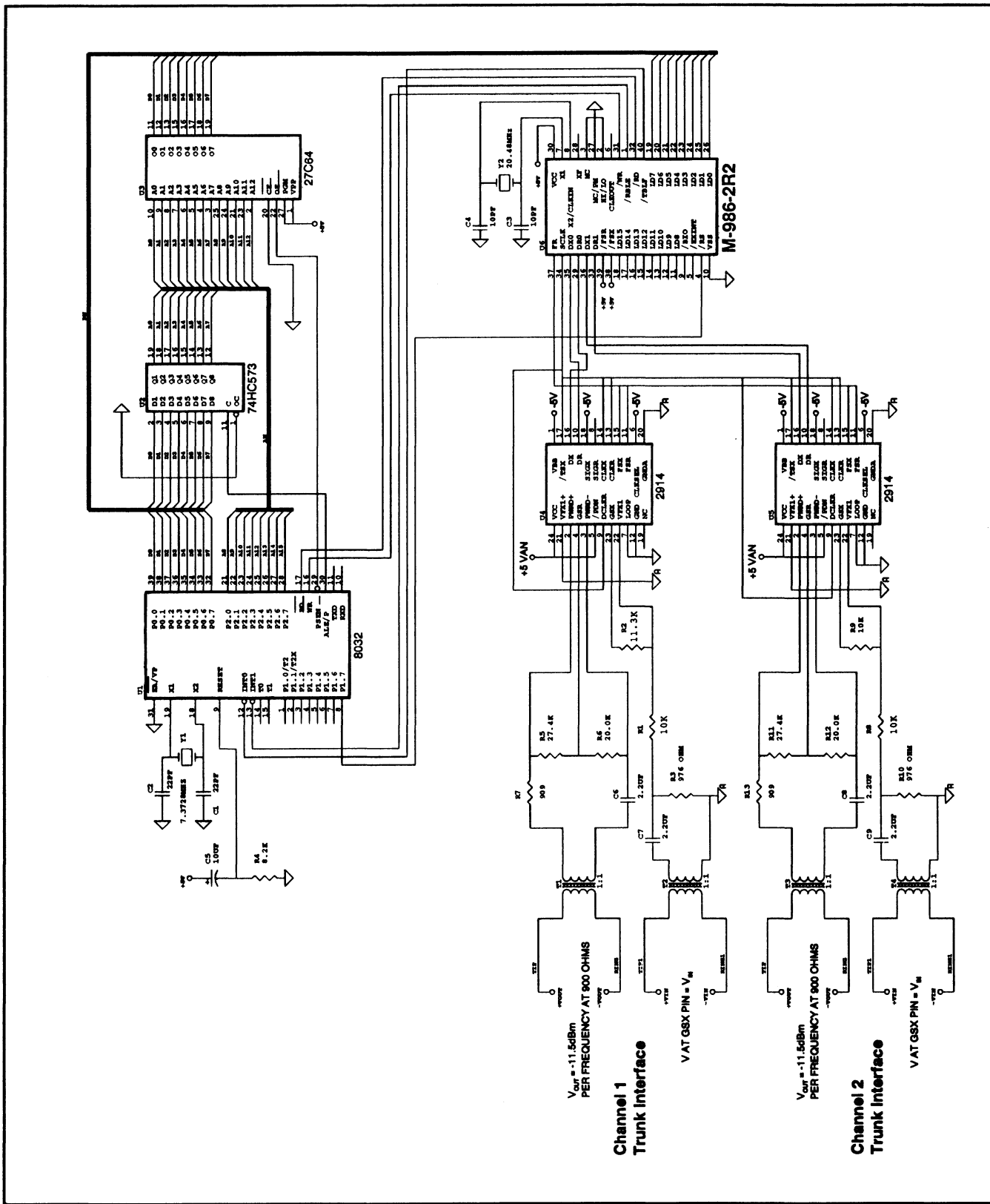
Figure 5   M-986 Dual Channel 4-wire Interface Application Circuit
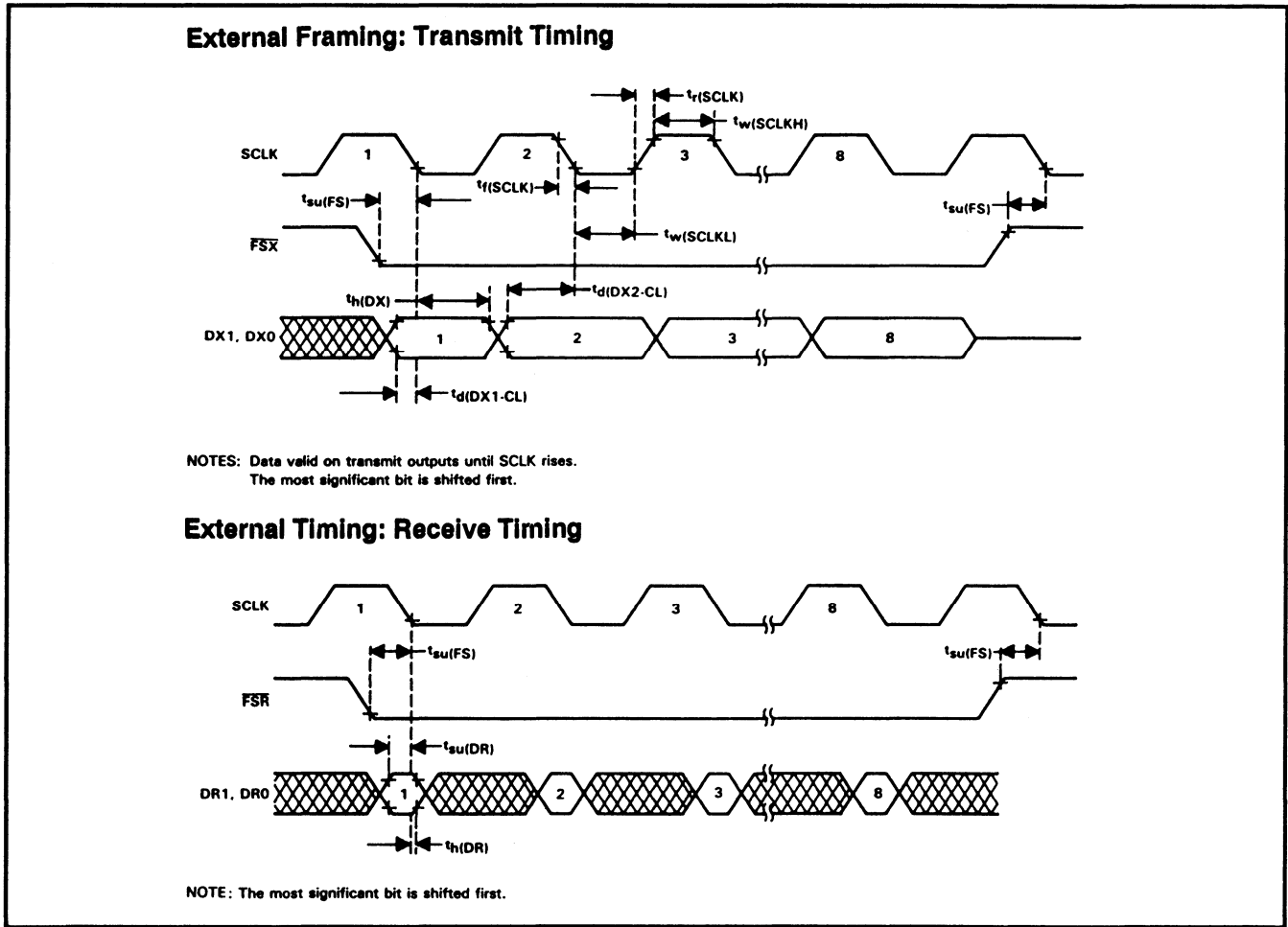
Figure 6 External Framing Timing Diagrams
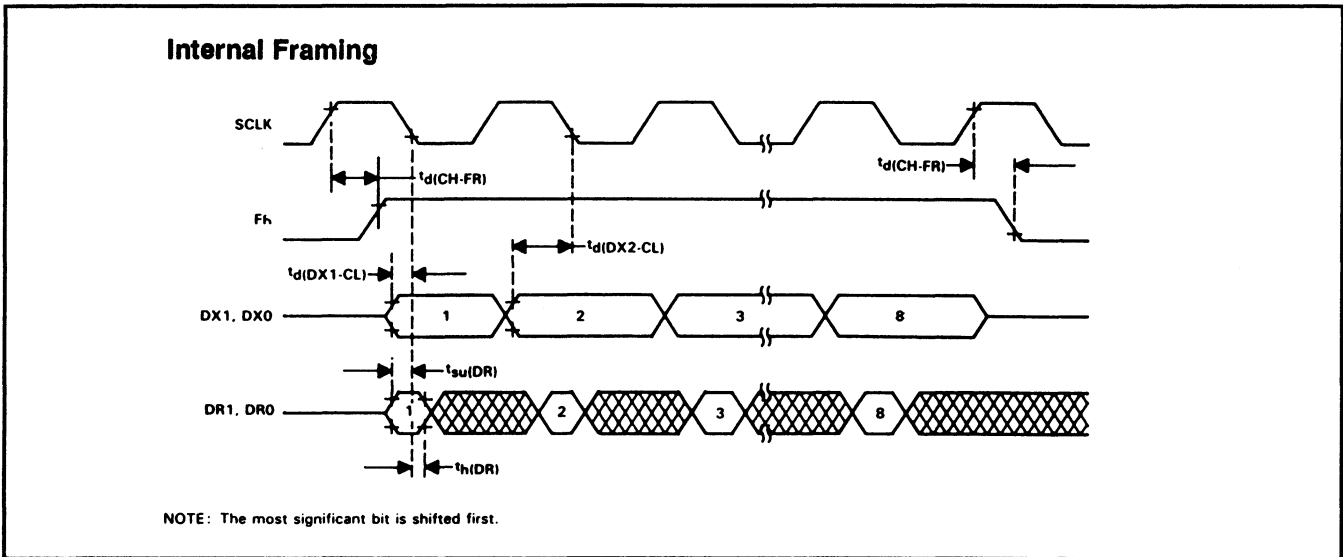
Figure 7 Internal Framing Timing

Reset Timing

Figure 8 Reset Timing

External Write to Coprocessor Port

External Read from Coprocessor Port
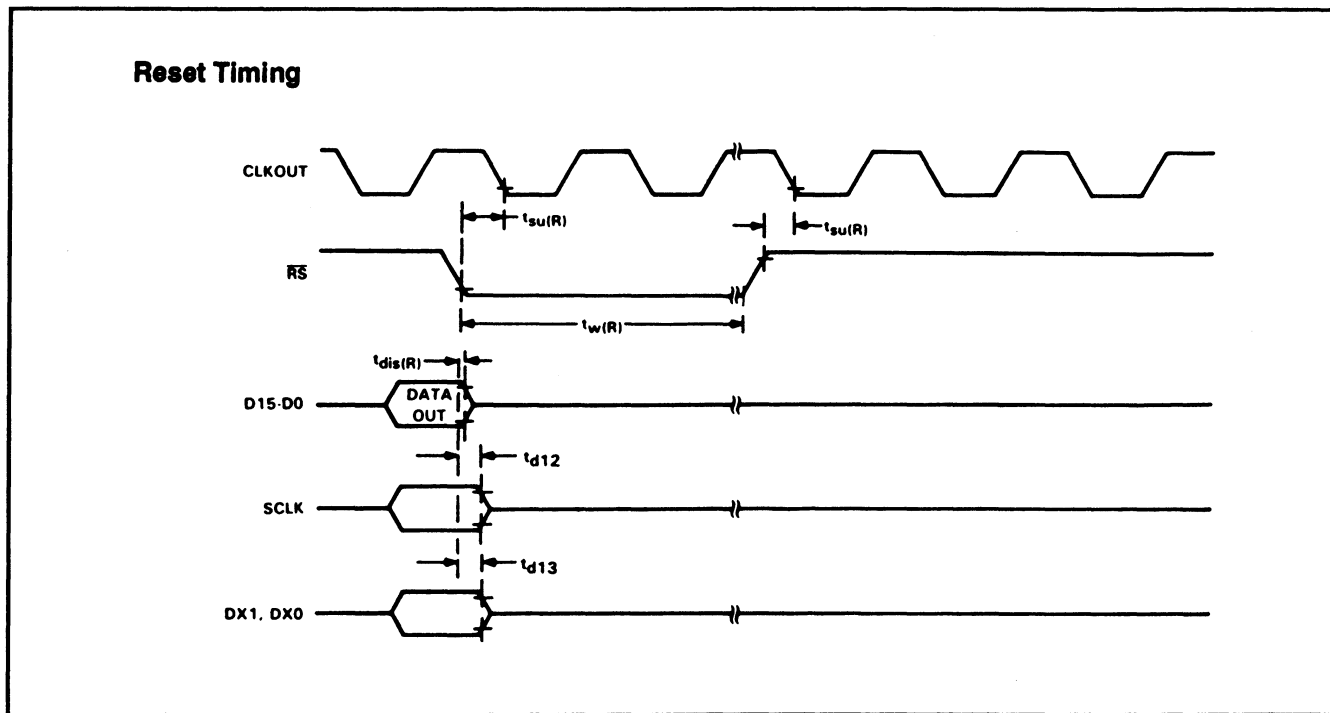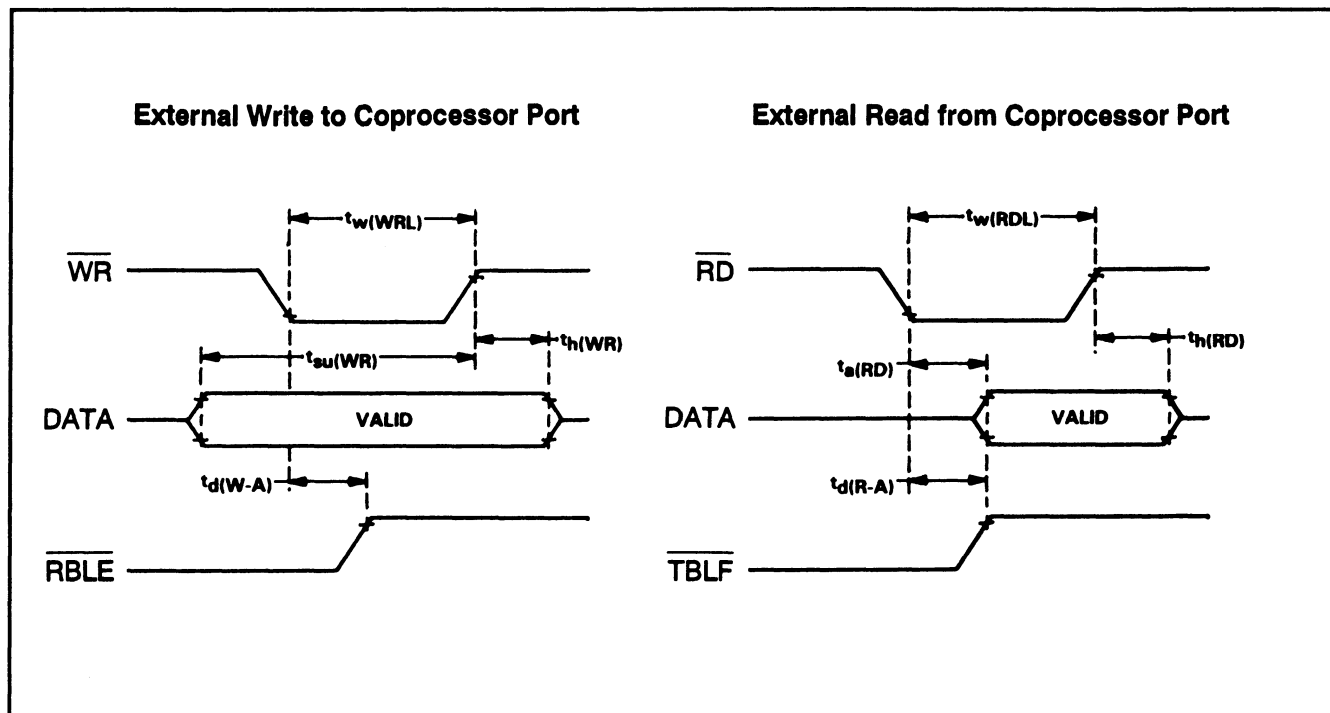
Figure 9 Coprocessor Timing

M-993 MULTIFREQUENCY TONE GENERATOR

The Teltone® M-993 is a monolithic CMOS integrated circuit designed to generate multifrequency (MF) tone pairs for use in trunk signaling. The tones generated conform to CCITT R1 signal recommendations and to AT&T MF standards. The M-993 permits design engineers to implement a highly accurate MF sender with a minimum of space, power, and added components. The accuracy of the tone frequencies is assured through use of an easily obtained 3.58-MHz color burst crystal or an external 3.58-MHz clock source.

Features
- Generates standard CCITT R1 MF tones
- Digital input control
- Linear (analog) output
- Power output capable of driving standard line
- 14-pin DIP
- Single 5-Volt supply
- Inexpensive 3.58-MHz time base

Applications
- Telephone systems
- Test equipment
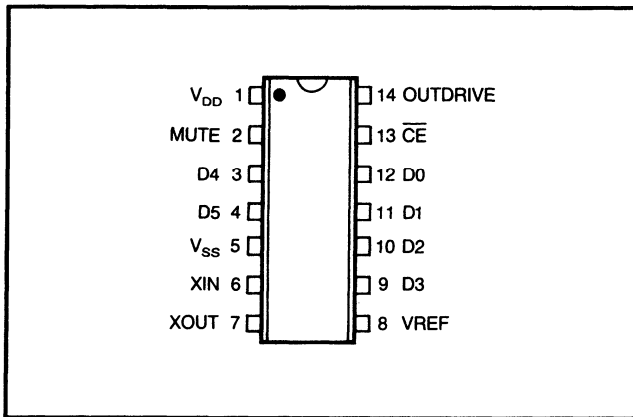
Figure 1 Pin Diagram
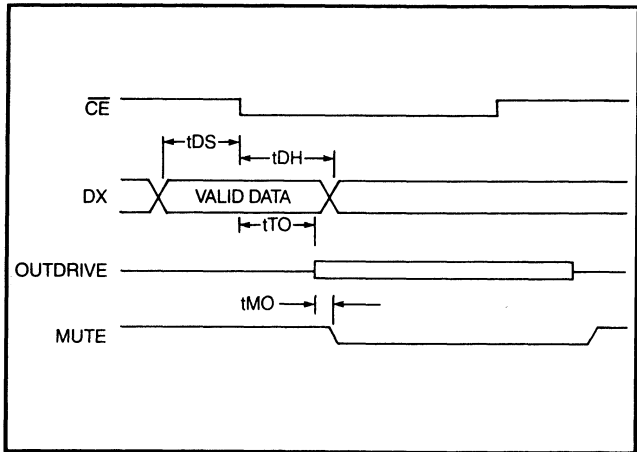
Figure 3 Timing Diagram
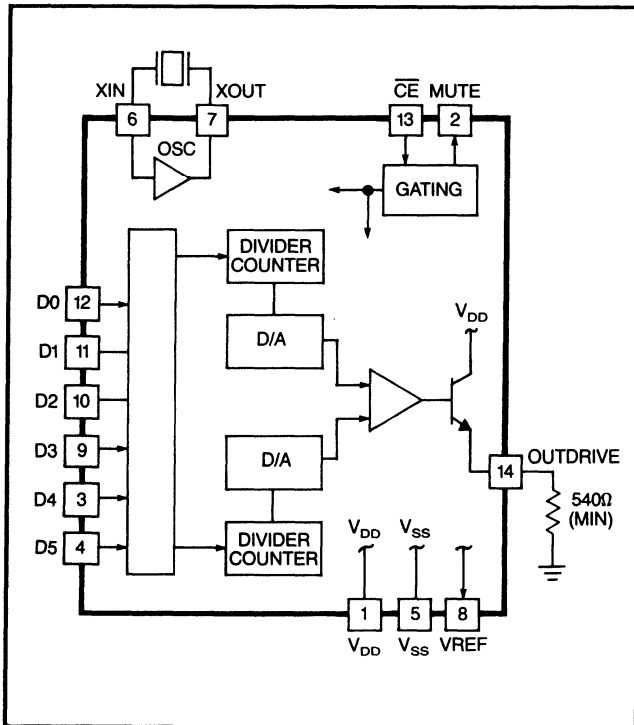
Figure 2 Block Diagram
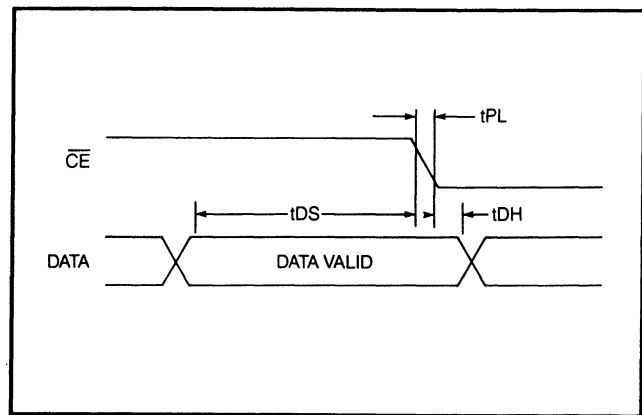
Figure 4 Expanded Wire Data Timing Diagram

R1 MF Tone Generation

MF tones are used to signal between telephone offices and between telephone company central switching equipment and customer equipment.

The M-993 is a highly linear tone generator that produces the tone pairs required for R1 MF signaling. Duration and frequency selection are digitally controlled (see Table 2 for data settings for a particular tone pair output).

A typical control sequence for the M-993 is: (1) set data lines to desired frequency selection, (2) wait for data lines to settle, (3) drive the chip enable ($\overline{CE}$) low, (4) maintain $\overline{CE}$ low for desired tone duration (Note: data lines may be changed after data hold time), and (5) return $\overline{CE}$ to a logic high.

Table 1 Pin Functions

PIN	FUNCTION
$\overline{CE}$	Latches data and enables output (active low input).
D0 - D5	Data input pins. (See Table 2).
MUTE	Output indicates that a signal is being generated at OUTDRIVE.
OUT-DRIVE	Linear buffered tone output.
V_{DD}	Most positive power supply input pin.
VREF	Internally generated mid-power supply voltage (output).
V_{SS}	Most negative power supply input pin.
XIN	Crystal oscillator or digital clock input.
XOUT	Crystal oscillator output.

Table 2 Data/Tone Selection

D3	D2	D1	D0	FREQUENCY (Hz) 1	FREQUENCY (Hz) 2	USE
0	0	0	0	1100	1700	Key Pulse (KP)
0	0	0	1	700	900	Digit 1
0	0	1	0	700	1100	Digit 2
0	0	1	1	900	1100	Digit 3
0	1	0	0	700	1300	Digit 4
0	1	0	1	900	1300	Digit 5
0	1	1	0	1100	1300	Digit 6
0	1	1	1	700	1500	Digit 7
1	0	0	0	900	1500	Digit 8
1	0	0	1	1100	1500	Digit 9
1	0	1	0	1300	1500	Digit 0
1	0	1	1	1500	1700	ST
1	1	0	0	900	1700	ST1
1	1	0	1	1300	1700	ST2
1	1	1	0	700	1700	ST3

Note: D4, D5 reserved for future use and default to inactive when left open.

Table 3 Absolute Maximum Ratings (Note 1)

Storage Temperature	-55 to $125\,°C$
Operating Ambient Temperature	-25 to $70\,°C$
V_{DD}	$7.0V$
Any Input Voltage	$V_{SS} -0.6$ to $V_{DD} +0.6V$

Note:

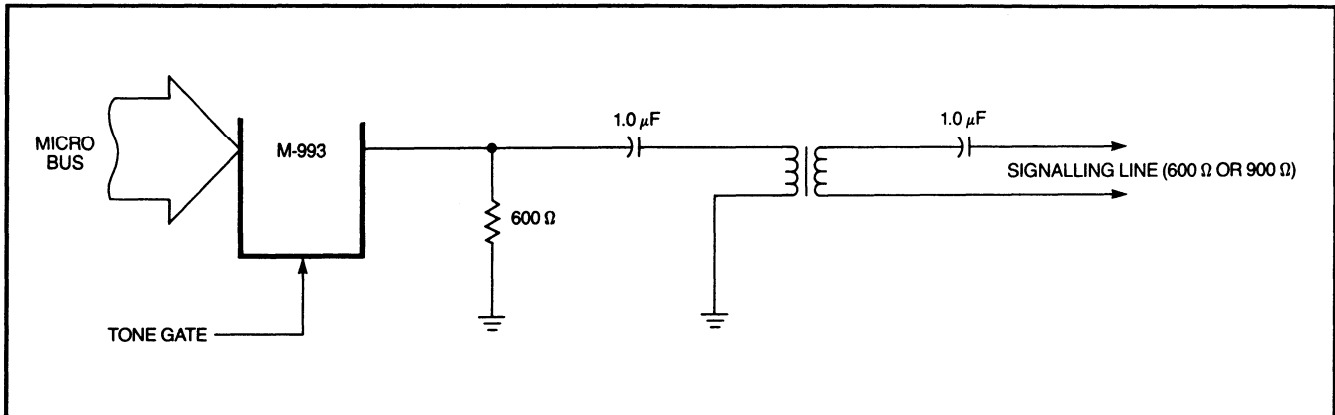1. Exceeding these ratings may permanently damage the M-993.

Figure 5 Typical Application

Table 4 Specifications

Unless otherwise noted, $V_{DD} - V_{SS} = 5VDC$, Ta $= 25°C$

PARAMETER		MIN	TYP	MAX	UNITS	NOTES
Power Supply and Reference	V_{DD}	4.75	—	5.25	V	1
	Current Drain, IDD	—	—	30	mA	8
	VREF Pin: Deviation from $(V_{DD} + V_{SS})/2$	−2	—	+2	%	
	Internal Resistance from VREF to V_{DD}, V_{SS}	3.25	—	6.75	Kohms	
Oscillator	Frequency Deviation	−0.01	—	+0.01	%	7
	External Clock: (XOUT open) VIL	0	—	0.2	V	
	VIH	V_{DD} −0.2	—	V_{DD}	V	
	Duty Cycle	40	—	60	%	
	XIN, XOUT Loading: Capacitance	—	—	10	pF	10
	Resitance	20	—	—	Mohms	
Tone Output	Frequency Deviation	−1.5	—	+1.5	%	
	Level	110	—	180	mV	2
	Distorting Components	−35	—	—	dB	3
	Idle	—	—	−60	dBm	4
	OUTDRIVE Envelope Rise Time	—	—	4	ms	5
Control	DX, $\overline{CE}$ Pins: VIL	—	—	0.5	V	6
	VIH	2.5	—	—	V	
	Mute Pins: VOL (ISINK = −100 μA)	—	—	1.5	V	
	VOH (ISOURCE = 100 μA)	V_{DD} −1.5	—	—	V	
Timing	Data Setup (tDS)	200	—	—	ns	
	Data Hold (tDH)	10	—	—	ns	
	Chip Enable Fall (tPL)	—	—	90	ns	11
	Tone On Delay (tTO)	—	—	5	ms	
	Tone Off Delay (tTD)	—	—	5	ms	
	Mute Delay from Outdrive (tMO)	—	—	200	ns	

Notes: (unless otherwise specified)

1. All DC voltages are referenced to V_{SS}.
2. Vrms per tone, 540 ohm load.
3. Any one frequency relative to the lowest level output tone (f < 4000 Hz).
4. 0 dBm = 0.775 Vrms.
5. To 90% maximum amplitude.
6. For all supply voltages in the operating range.
7. At XOUT pin as compared to 3.579545 MHz.
8. OUTDRIVE inactive.
9. Resistance at VREF to V_{DD} or V_{SS} >1 Mohm.
10. Crystal oscillator active.
11. Measured 90% to 10%.

Figure 6 Package Dimensions

14-PIN CERDIP

14-PIN PLASTIC

DIMENSIONS:
INCHES
(MILLIMETERS)

DC Signaling Devices

M-949-01 LINE SENSE RELAY   6-1

The Teltone® M-949-01 Line Sense Relay is a small PWB-mount loop current detector with the safety and reliability features required for FCC Part 68 regulated telephone applications. When connected to the voice pair (Tip and Ring) of an ordinary telephone line, the M-949-01 provides a 1 Form A relay closure in response to current above 20 mA flowing through the wires. This closure can be used by control circuitry for on-hook/off-hook monitoring, switchhook flash detection, and rotary dial pulse counting. Simple in design and rugged in construction, the M-949-01 is ideally suited for use with the Teltone M-927, M-948, M-967, and other loop current controlled telephone dialing receivers.

Features

- Senses telephone line current from 20 to 125 mA
- Includes 1 Form A relay contact
- Maximum closure time 1 ms including bounce
- Achieves 63 dB minimum longitudinal balance
- Provides 1500 VDC coil-to-contact isolation

Applications

- Central office products
- PBX and key systems
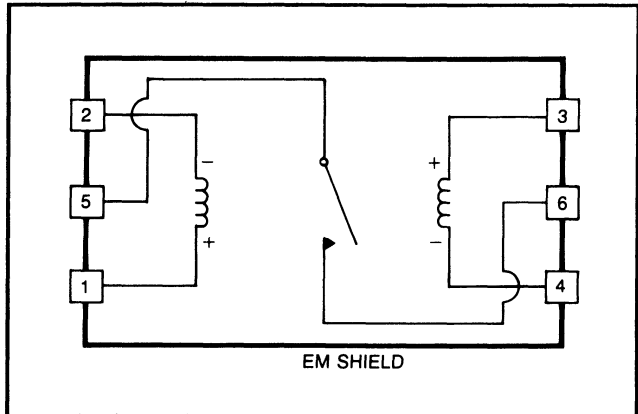- Rotary dial monitoring devices

Figure 1 Electrical Configuration

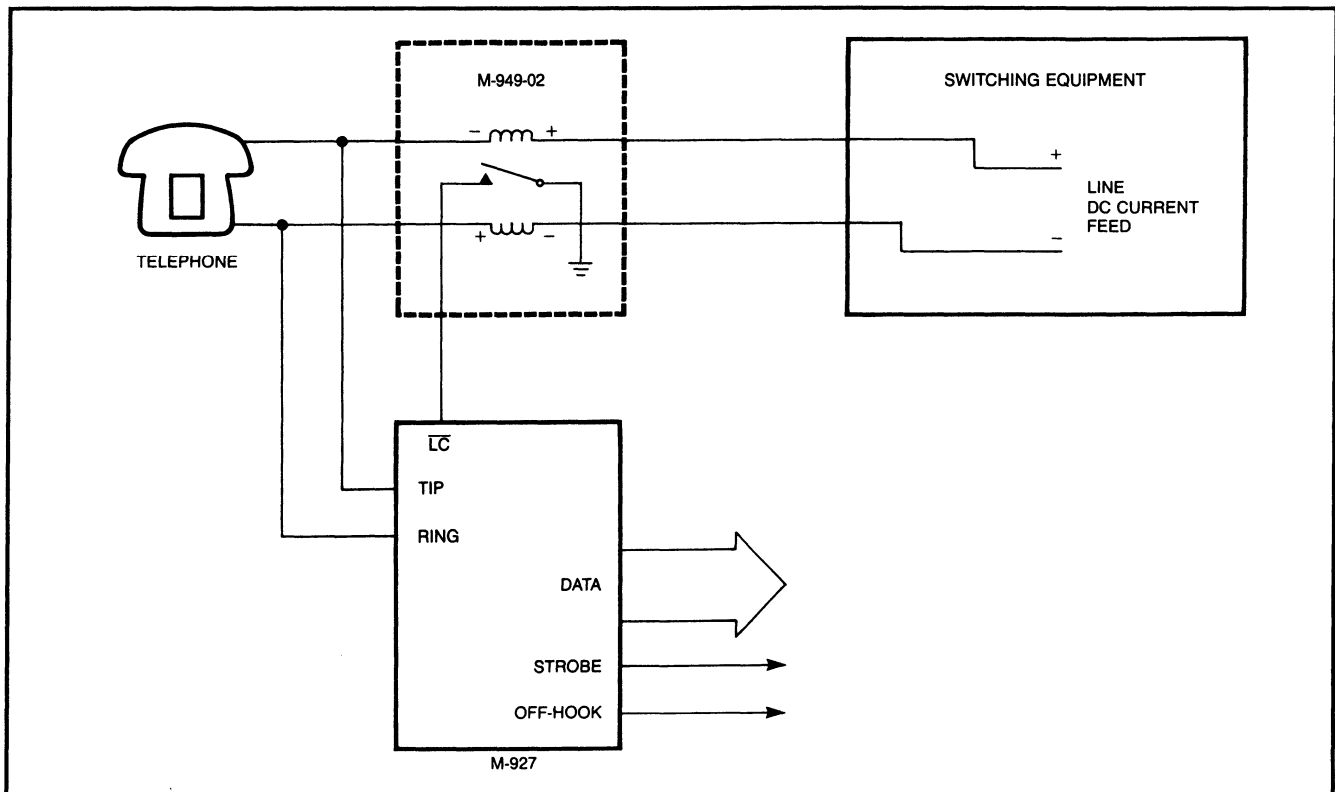**Figure 2 Typical Application: Dialed Digit Monitor**

Table 1 Specifications

	Parameter	Conditions	Min	Max	Units	Notes
Dual Coils	Pick Up Current	0° to 70°C ambient	20	—	mA	1
	Drop Out Current	0° to 70°C ambient	—	6	mA	1
	Coil Current	20°C ambient	—	125	mA	2
	Coil Resistance		—	20	ohms	
	Coil Inductance		—	4	mH	3
	Longitudinal Balance		63	—	dB	4
	Excitation to Closure Time (Including Bounce)		—	1	ms	5
	Excitation Removal to Open Time		—	0.5	ms	
Relay Contact	Voltage Rating		200	—	VDC	
	Current Rating		500	—	mA	
	Power (Resistive) Rating		10	—	W	
	Rated Life		10^7	—	operations	6
Dielectric Strength	Open Contacts		300	—	VDC	
	Coil to Coil		1000	—	VDC	
	Coil to Contact		1500	—	VDC	
Ambient Temperature	Operating	85% RH	0	70	°C	
	Non-operating	95% RH	−20	70	°C	

Notes:
1. With coils in series-aiding configuration.
2. With the current continuously applied.
3. At 1 kHz.
4. With current of 20—100 mA at 200—3000 Hz.
5. With current of 20 mA and coils in series-aiding configuration.
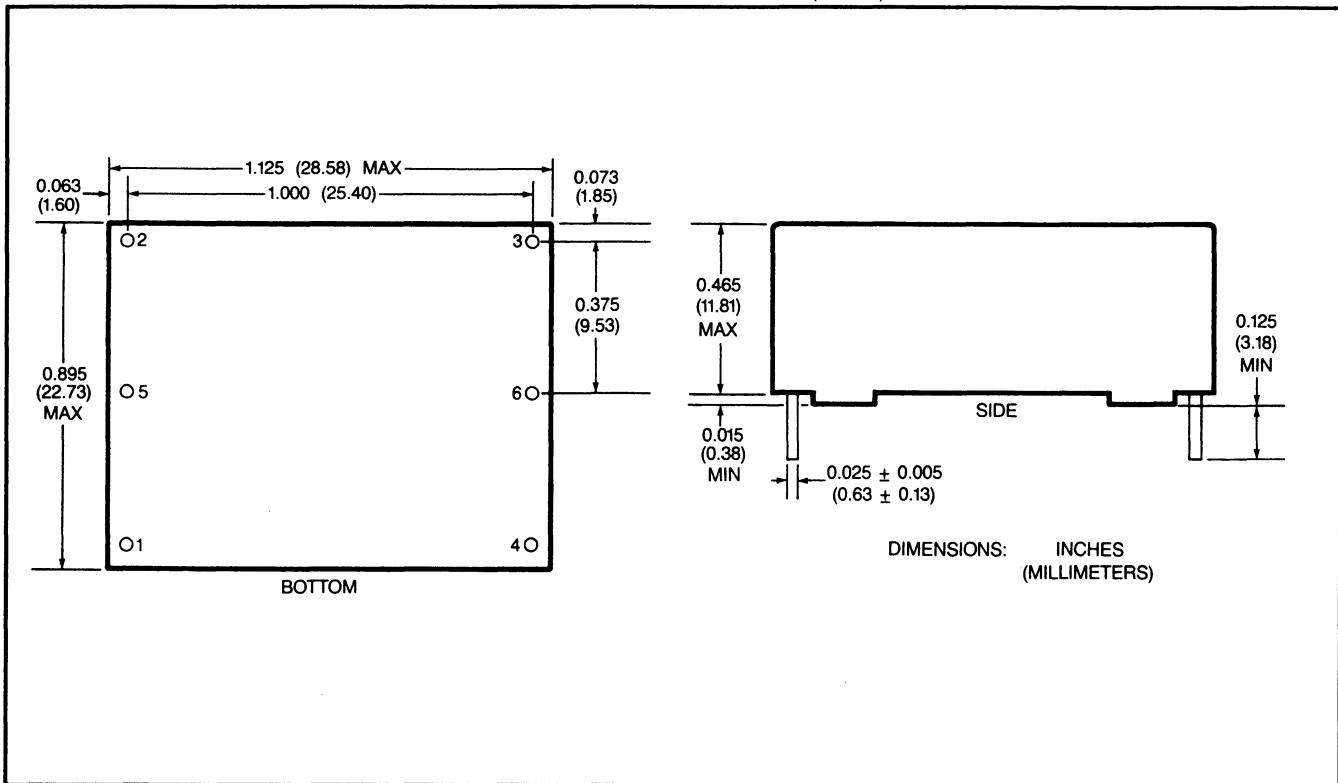6. At 10 W (resistive).

Figure 3 Package Dimensions

M-949-02 HIGH-BREAKDOWN LINE SENSE RELAY

The Teltone® M-949-02 High-Breakdown Line Sense Relay is a small PWB-mount loop current detector with the safety and reliability features required for International regulated telephone applications. When connected to the voice pair (Tip and Ring) of an ordinary telephone line, the M-949-02 provides a 1 Form A relay closure in response to current above 15 mA flowing through the wires. This closure can be used by control circuitry for on-hook/off-hook monitoring, switchhook flash detection, and rotary dial pulse counting. The Teltone M-949-02 is mechanically and electrically designed to meet or exceed coil-to-contact spacing and breakdown requirements common to International applications.

Features

- Senses telephone line current from 15 to 170 mA
- Includes 1 Form A relay contact
- Maximum closure time 1 ms including bounce
- Achieves 70 dB typical longitudinal balance
- Provides 9.5 mm coil-to-contact lead spacing
- Provides 3750 Vrms coil-to-contact isolation
- Relay is magnetically shielded

Applications

- Central office products
- PBX and key systems
- Rotary dial monitoring devices
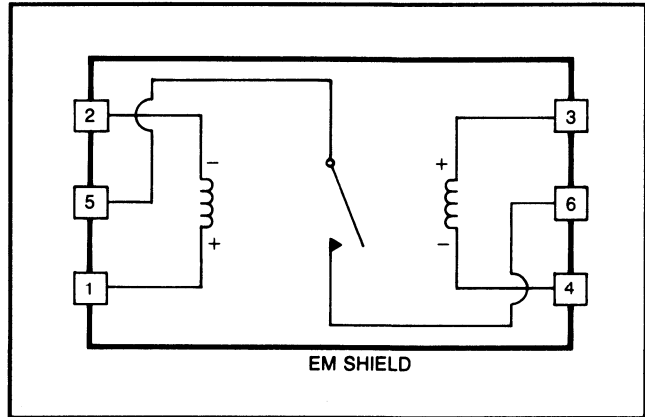- Subscriber loop applications

EM SHIELD

Figure 1 Electrical Configuration

Figure 2 Typical Application: Dialed Digit Monitor

Table 1 Specifications

	Parameter	Conditions	Min	Max	Units	Notes
Dual Coils	Pick Up Current	0° to 70°C ambient	15	—	mA	1
	Drop Out Current	0° to 70°C ambient	—	6	mA	1
	Coil Current	20°C ambient	—	170	mA	2
	Coil Resistance		—	20	ohms	
	Coil Inductance		—	4	mH	3
	,Longitudinal Balance		63	—	dB	4
	Excitation to Closure Time (Including Bounce)		—	1	ms	5
	Excitation Removal to Open Time		—	0.5	ms	
Relay Contact	Voltage Rating		200	—	V	
	Current Rating		500	—	mA	
	Power (Resistive) Rating		10	—	W	
	Rated Life		10^7	—	operations	6
Dielectric Strength	Open Contacts		250	—	VDC	
	Coil to Coil		1000	—	VDC	
	Coil to Contact		3750	—	Vrms	
Ambient Temperature	Operating	85% RH	0	70	°C	
	Non-operating	95% RH	−20	70	°C	

Notes:
1. With coils in series-aiding configuration.
2. With the current continuously applied.
3. At 1 kHz.
4. With current of 20—100 mA at 200—3000 Hz.
5. With current of 20 mA and coils in series-aiding configuration.
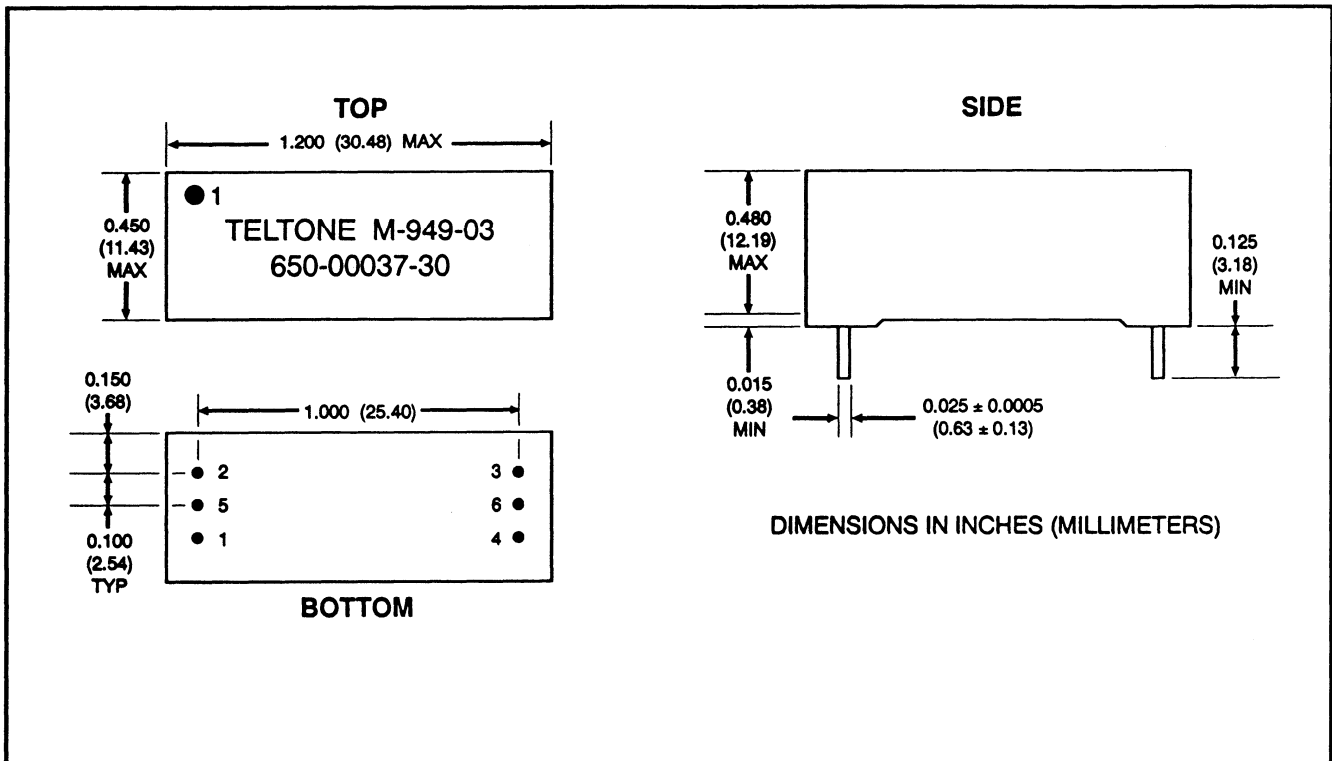6. At 10 W (resistive).

Figure 3 Package Dimensions

M-949-03 LINE SENSE RELAY

The Teltone® M-949-03 Line Sense Relay is a small PWB-mount loop current detector with the safety and reliability features required for FCC Part 68 as well as for Canadian and other international regulated telephone applications. When connected to the voice pair (Tip and Ring) of an ordinary telephone line, the M-949-03 provides a 1 Form A relay closure in response to current above 20 mA flowing through the wires. This closure can be used by control circuitry for on-hook/off-hook monitoring, switchhook flash detection, and rotary dial pulse counting. Simple in design and rugged in construction, the M-949-03 is ideally suited for use with the Teltone M-927, M-948, M-967, and other loop current controlled telephone dialing receivers.

Features

- Senses telephone line current from 20 to 125 mA
- Low coil resistance (9 ohms)
- Includes 1 Form A relay contact
- Maximum closure time 1 ms including bounce
- Achieves 63 dB minimum longitudinal balance
- Provides 1500 VDC coil-to-contact isolation

Applications

- Central office products
- PBX and key systems
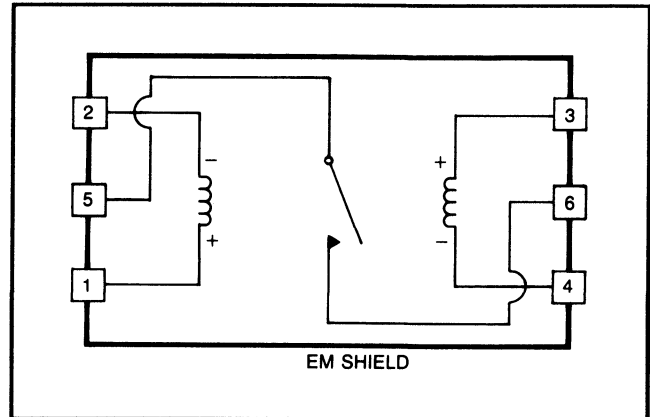- Rotary dial monitoring devices

Figure 1 Electrical Configuration

Figure 2 Typical Application: Dialed Digit Monitor

Table 1 Specifications

	Parameter	Conditions	Min	Max	Units	Notes
Dual Coils	Pick Up Current	0° to 70° C ambient	20	—	mA	1
	Drop Out Current	0° to 70° C ambient	—	6	mA	1
	Coil Current	20° C ambient	—	125	mA	2
	Coil Resistance		—	9	ohms	
	Coil Inductance		—	4	mH	3
	Longitudinal Balance		63	—	dB	4
	Excitation to Closure Time (Including Bounce)		—	1	ms	5
	Excitation Removal to Open Time		—	0.5	ms	
Relay Contact	Voltage Rating		200	—	VDC	
	Current Rating		500	—	mA	
	Power (Resistive) Rating		10	—	W	
	Rated Life		10^7	—	operations	6
Dielectric Strength	Open Contacts		300	—	VDC	
	Coil to Coil		1000	—	VDC	
	Coil to Contact		1500	—	VDC	
Ambient Temperature	Operating	85% RH	0	70	°C	
	Non-operating	95% RH	−20	70	°C	

Notes:

1. With coils in series-aiding configuration.
2. With the current continuously applied.
3. At 1 kHz.
4. With current of 20—100 mA at 200—3000 Hz.
5. With current of 20 mA and coils in series-aiding configuration.
6. At 10 W (resistive).

Figure 3 Package Dimensions

M-949-06 HIGH-BREAKDOWN LINE SENSE RELAY

The Teltone® M-949-06 High-Breakdown Line Sense Relay is a small PWB-mount loop current detector with the safety and reliability features required for International regulated telephone applications. When connected to the voice pair (Tip and Ring) of an ordinary telephone line, the M-949-06 provides a 1 Form A relay closure in response to current above 15 mA flowing through the wires. This closure can be used by control circuitry for on-hook/off-hook monitoring, switchhook flash detection, and rotary dial pulse counting. The Teltone M-949-06 is mechanically and electrically designed to meet or exceed coil-to-contact spacing and breakdown requirements common to International applications.

Features

- Senses telephone line current from 15 to 170 mA
- Low coil resistance (9 ohms)
- Includes 1 Form A relay contact
- Maximum closure time 1 ms including bounce
- Achieves 70 dB typical longitudinal balance
- Provides 9.5 mm coil-to-contact lead spacing
- Provides 2250 Vrms coil-to-contact isolation
- Relay is magnetically shielded

Applications

- Central office products
- PBX and key systems
- Rotary dial monitoring devices
- Subscriber loop applications

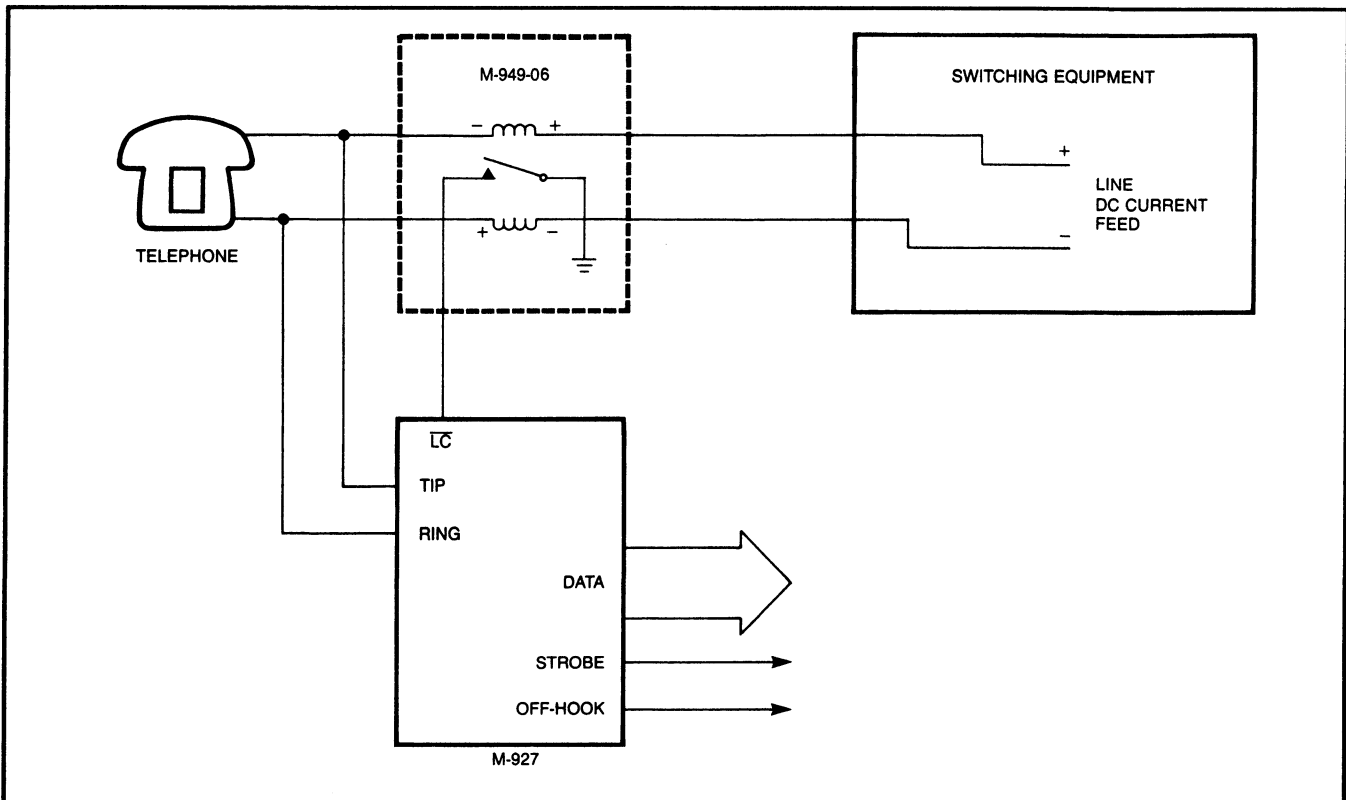**Figure 1 Electrical Configuration**

Figure 2 Typical Application: Dialed Digit Monitor

Table 1 Specifications

Parameter		Conditions	Min	Max	Units	Notes
Dual Coils	Pick Up Current	0° to 70°C ambient	15	—	mA	1
	Drop Out Current	0° to 70°C ambient	6	—	mA	1
	Coil Current	20°C ambient	—	170	mA	2
	Coil Resistance		—	9	ohms	
	Coil Inductance		—	4	mH	3
	·Longitudinal Balance		63	—	dB	4
	Excitation to Closure Time (Including Bounce)		—	1	ms	5
	Excitation Removal to Open Time		—	0.5	ms	
Relay Contact	Voltage Rating		200	—	V	
	Current Rating		500	—	mA	
	Power (Resistive) Rating		10	—	W	
	Rated Life		10^7	—	operations	6
Dielectric Strength	Open Contacts		250	—	VDC	
	Coil to Coil		1000	—	VDC	
	Coil to Contact		2250	—	Vrms	
Ambient Temperature	Operating	85% RH	0	70	°C	
	Non-operating	95% RH	−20	70	°C	

Notes:

1. With coils in series-aiding configuration.
2. With the current continuously applied.
3. At 1 kHz.
4. With current of 20—100 mA at 200—3000 Hz.
5. With current of 20 mA and coils in series-aiding configuration.
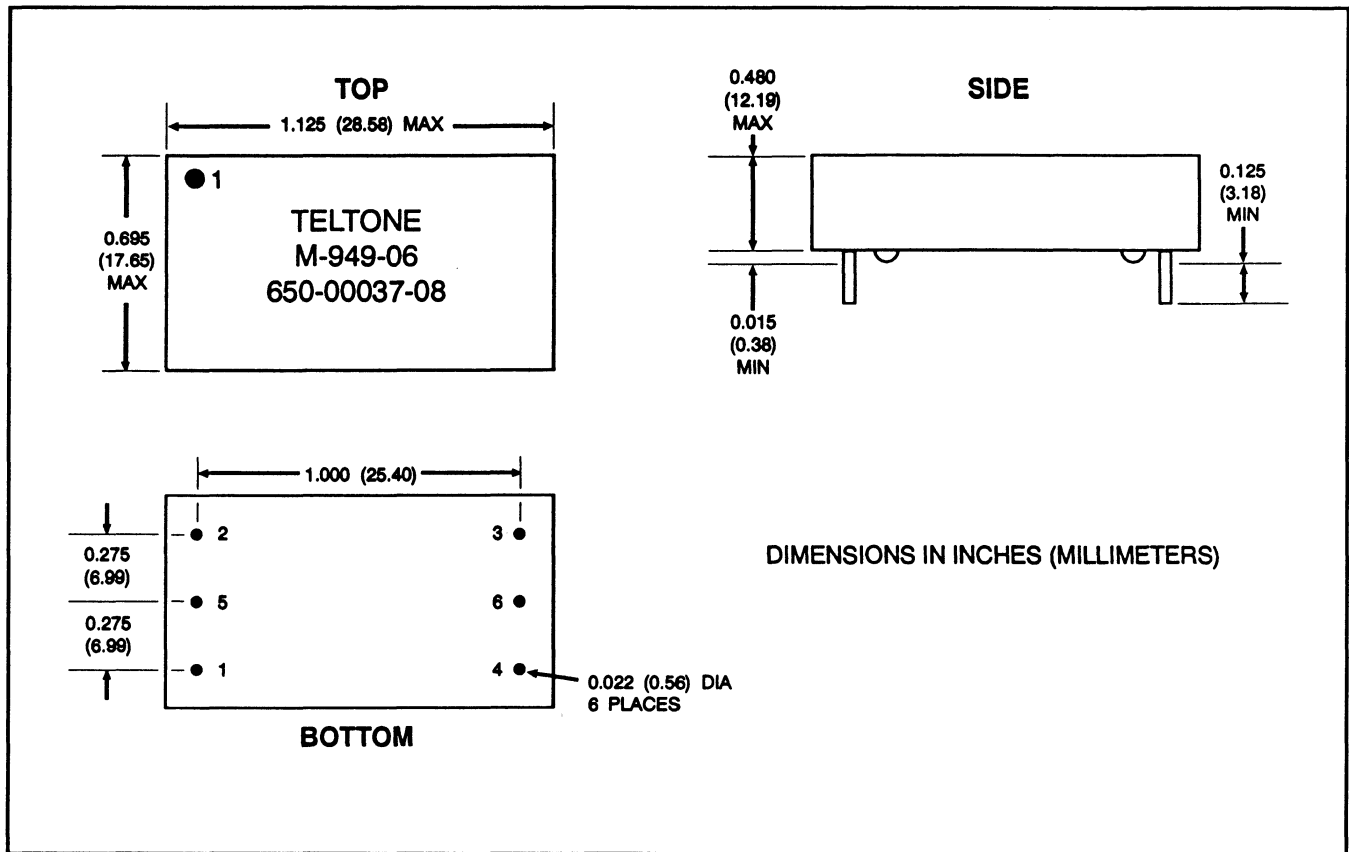6. At 10 W (resistive).

Figure 3 Package Dimensions

M-949-10 LINE SENSE RELAY

The Teltone® M-949-10 Line Sense Relay is a small PWB-mount loop current detector with the safety and reliability features required for FCC Part 68 regulated telephone applications. When connected to the voice pair (Tip and Ring) of an ordinary telephone line, the M-949-01 provides a 1 Form A relay closure in response to current above 17.5 mA flowing through the wires. This closure can be used by control circuitry for on-hook/off-hook monitoring, switchhook flash detection, and rotary dial pulse counting. Simple in design and rugged in construction, the M-949-10 is ideally suited for use with the Teltone M-927, M-948, M-967, and other loop current controlled telephone dialing receivers.

Features

- Senses telephone line current from 17.5 to 125 mA
- Includes 1 Form A relay contact
- Maximum closure time 1 ms including bounce
- Achieves 63 dB minimum longitudinal balance
- Provides 1500 VDC coil-to-contact isolation

Applications

- Central office products
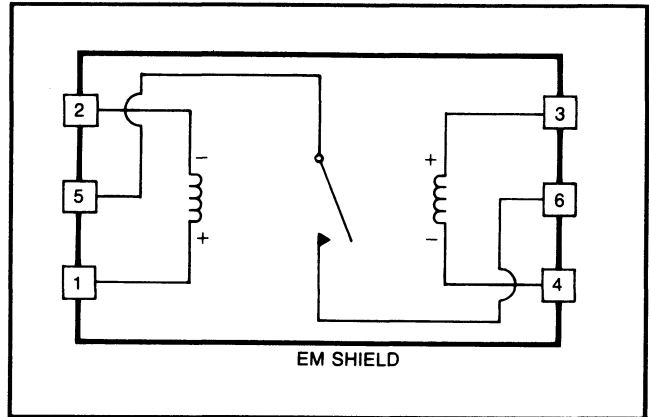- PBX and key systems
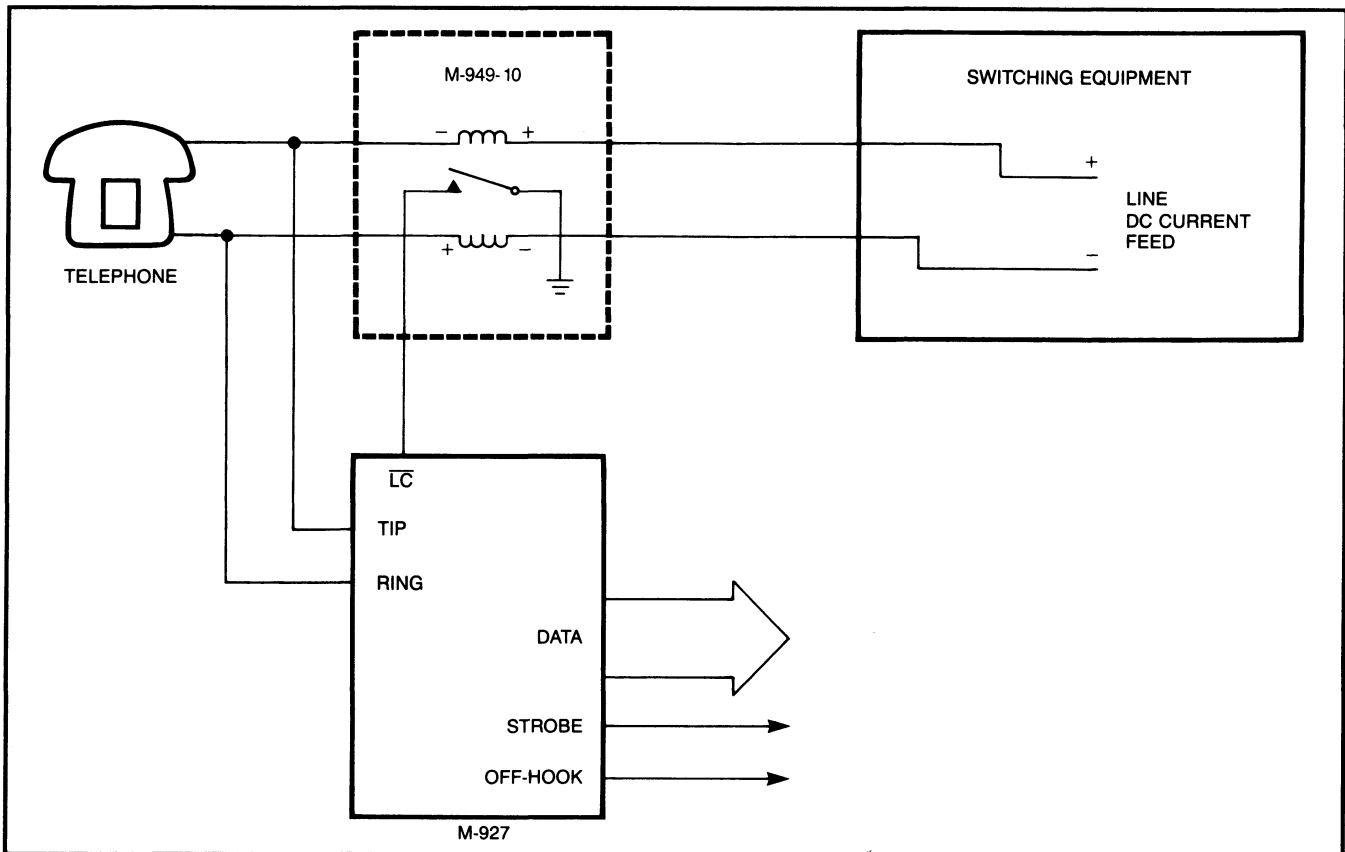- Rotary dial monitoring devices

Figure 1 Electrical Configuration

Figure 2 Typical Application: Dialed Digit Monitor

Table 1 Specifications

	Parameter	Conditions	Min	Max	Units	Notes
Dual Coils	Pick Up Current	0° to 70°C ambient	17.5	—	mA	1
	Drop Out Current	0° to 70°C ambient	—	8	mA	1
	Coil Current	20°C ambient	—	125	mA	2
	Coil Resistance		—	20	ohms	
	Coil Inductance		—	4	mH	3
	·Longitudinal Balance		63	—	dB	4
	Excitation to Closure Time (Including Bounce)		—	1	ms	5
	Excitation Removal to Open Time		—	0.5	ms	
Relay Contact	Voltage Rating		200	—	VDC	
	Current Rating		500	—	mA	
	Power (Resistive) Rating		10	—	W	
	Rated Life		10^7	—	operations	6
Dielectric Strength	Open Contacts		300	—	VDC	
	Coil to Coil		1000	—	VDC	
	Coil to Contact		1500	—	Vrms	
Ambient Temperature	Operating	85% RH	0	70	°C	
	Non-operating	95% RH	−20	70	°C	

Notes:

1. With coils in series-aiding configuration.
2. With the current continuously applied.
3. At 1 kHz.
4. With current of 20—100 mA at 200—3000 Hz.
5. With current of 20 mA and coils in series-aiding configuration.
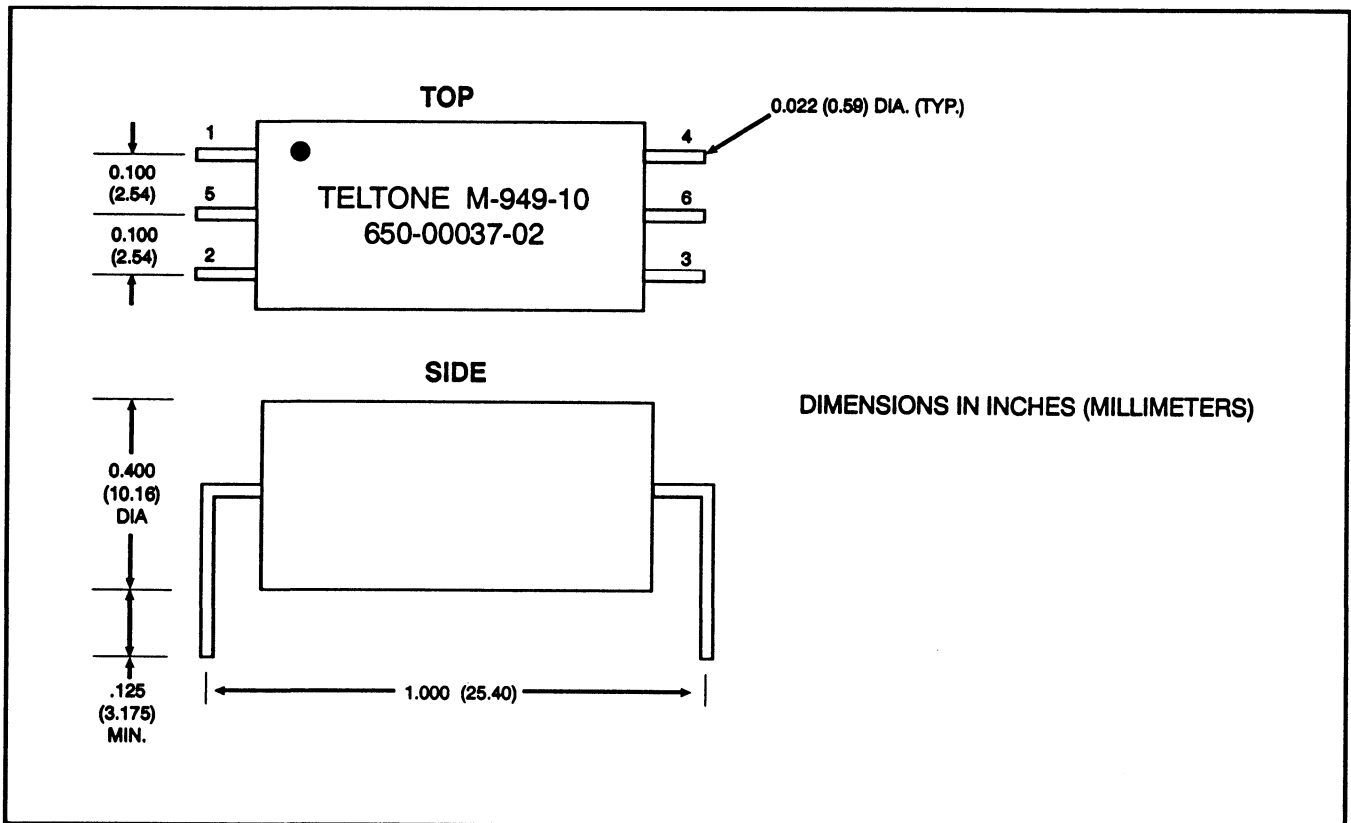6. At 10 W (resistive).

Figure 3 Package Dimensions

M-959 DIAL PULSE COUNTER AND HOOK STATUS MONITOR

The Teltone® M-959 is a low-power dial pulse counter and hook status monitor. Contained in a 14-pin package, the M-959 requires no external components except a single 3.579 MHz television color burst crystal.

The M-959 is typically connected to a loop current sensing circuit, which is connected in series with the voice pair (Tip and Ring) of a telephone line. The M-959 receives pulses from the loop current sense circuit and translates them into logic level outputs indicating hook status and decoded dialed digits. Logic inputs to the M-959 select dialed digit speeds and control Data and Strobe outputs supporting bus interrupt driven implementations.

Features

* Time-guarded dial pulse counting
* 10 or 20 PPS dialing speeds pin selectable
* Data outputs tri-statable
* Valid data output strobe
* Data strobe control for use in interrupt-driven environments
* Independent hook status monitoring
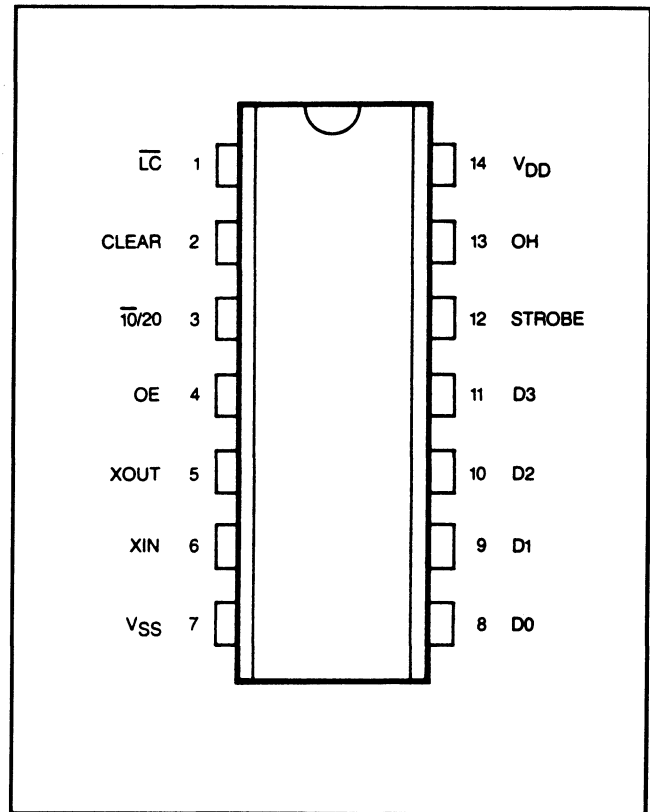* Low-power CMOS construction
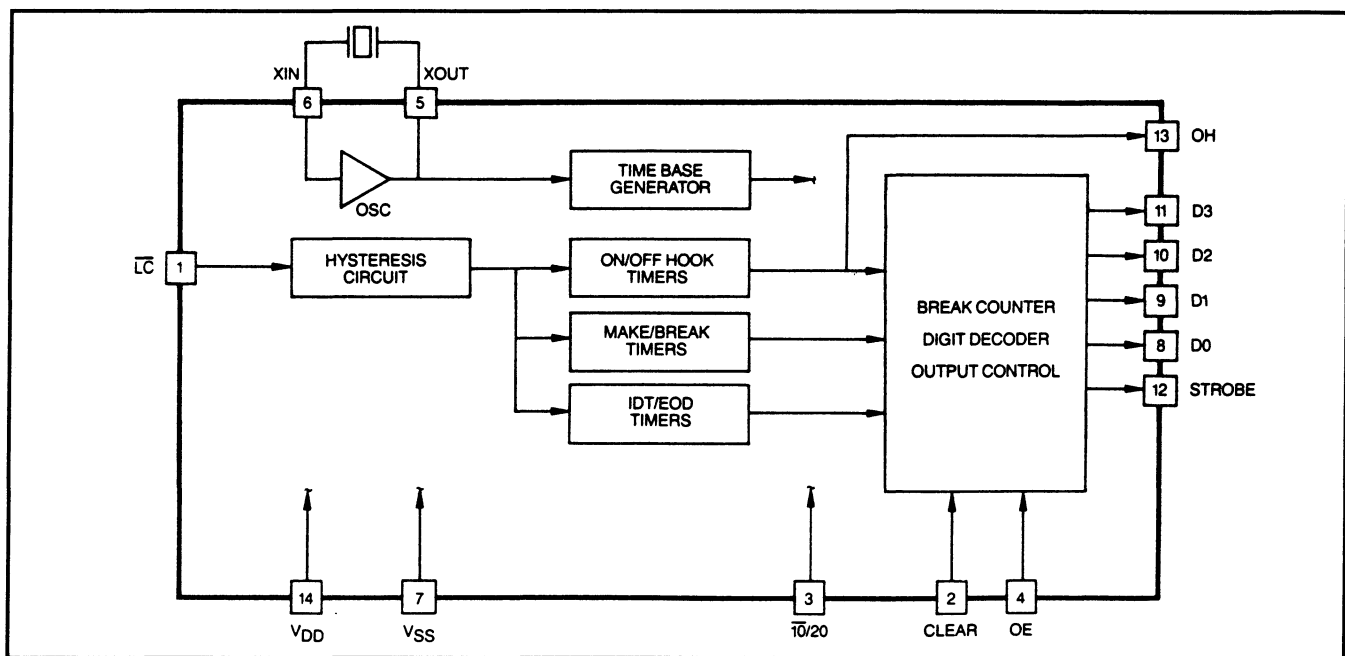

Figure 1 Pin Diagram

Figure 2 Block Diagram

Table 1 Pin Functions

PIN	FUNCTION
$\overline{LC}$	Loop Current Input. Signal from phone line to be monitored for dial pulse signalling and hook status. Active low, internally pulled high.
OH	Off Hook Output. Hook status of phone line. Active (off hook) high.
$\overline{10}$/20	Pulse Speed Input. Low for 10 pulse per second, high for 20 pulse per second. Internally pulled low.
D3-D0	Data Outputs. Binary decoded rotary dialed digit. Active during valid digit time (strobe high), low at any other time.

Digit Dialed	D3	D2	D1	D0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0

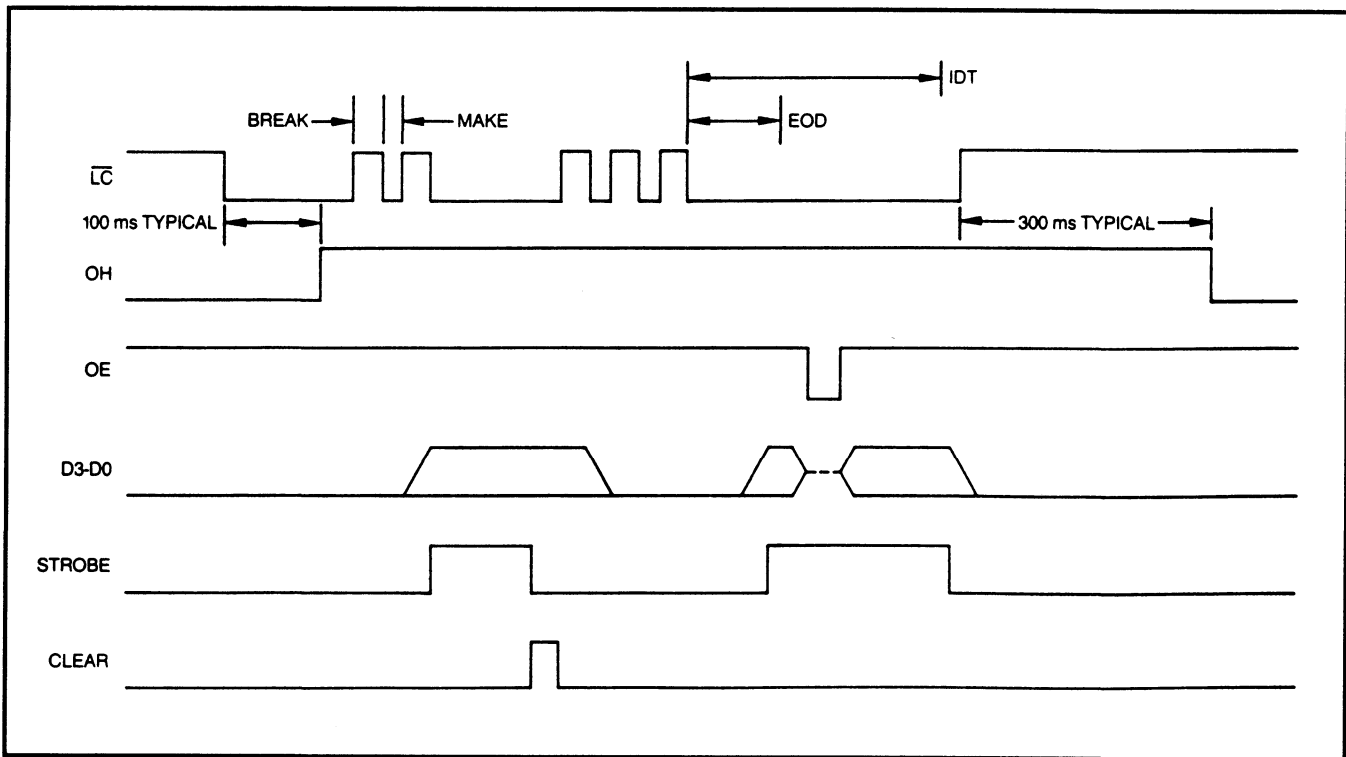| PIN	FUNCTION
OE	Output Enable Input. Active high, a logic low tri-states D3 through D0 outputs. Internally pulled high.
XIN	Crystal Oscillator Input.
XOUT	Crystal Oscillator Output.
CLEAR	Strobe Control Input. Momentary high during digit valid time resets STROBE latch output low until next valid digit is received. Internally pulled low.
STROBE	Digit Valid Output. Indicates valid digit data present on D3 through D0. Active high.

Figure 3 Timing Diagram

Table 2 Specifications

$V_{DD} - V_{SS} = 2.5$ through 6.0V unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Signal	Break Recognition	10 PPS	45	—	85	ms	
Timing		20 PPS	30	—	40	ms	
	Spurious Break Rejection	—	0	—	10	ms	
	Make Recognition	10 PPS	30	—	65	ms	
		20 PPS	15	—	24	ms	
	Interdigit Time	10 PPS	285	300	315	ms	
	(IDT)	20 PPS	142.5	150	157.5	ms	
	Off-Hook Delay	—	95	100	105	ms	
	On-Hook Delay	—	285	300	315	ms	
	LC Hysteresis	—	1	1.5	2	ms	
	EOD (End of Digit)	10 PPS	95	100	105	ms	
	Recognition	20 PPS	47.5	50	52.5	ms	
	STROBE Active	10 PPS	190	200	210	ms	
		20 PPS	95	100	105	ms	
	Data Change Before STROBE Active	—	1.0	1.5	2.0	ms	
Logic Input	Input Voltages	Logic 0	0.0	2.25	1.5	V	1, 2
Requirements		Logic 1	3.5	2.75	5.0	V	1, 3
	Input Current	—	—	—	±30	μA	
	Pull Up/Down Resistance	—	200K	—	—	ohms	
Logic Output	Output Voltages	Logic 0	0.0	—	0.5	V	1, 4
Characteristics		Logic 1	4.5	—	5.0	V	1, 4
	Output Currents	Vout = 2.5V	−2.1	−4.2	—	mA.	1
		Vout = 4.6V	−0.44	−0.88	—	mA	1
		Vout = 0.4V	0.44	0.88	—	mA	1
	Tri-State Leakage	—	—	—	±1.0	μA	
Power Requirement	Supply Current	—	—	—	2.0	mA	

Notes

1. $V_{DD} - V_{SS} = 5.0V$.

2 Maximum is 30% of $V_{DD} - V_{SS}$.

3. Minimum is 70% of $V_{DD} - V_{SS}$.

4. No load.

5. Typical column for reference only.

Table 3 Absolute Maximum Ratings (Note 1)

DC Supply Voltage 6.0V

Any Input Voltage Relative to V_{DD}. . . . . +0.3V

Any Input Voltage Relative to V_{SS}. . . . . −0.3V

Operating Temperature Range. . . . . −40° to +85°C

Storage Temperature Range. . . . . −55° to +125°C

Note:

1. Exceeding these ratings may permanently damage the M-959.
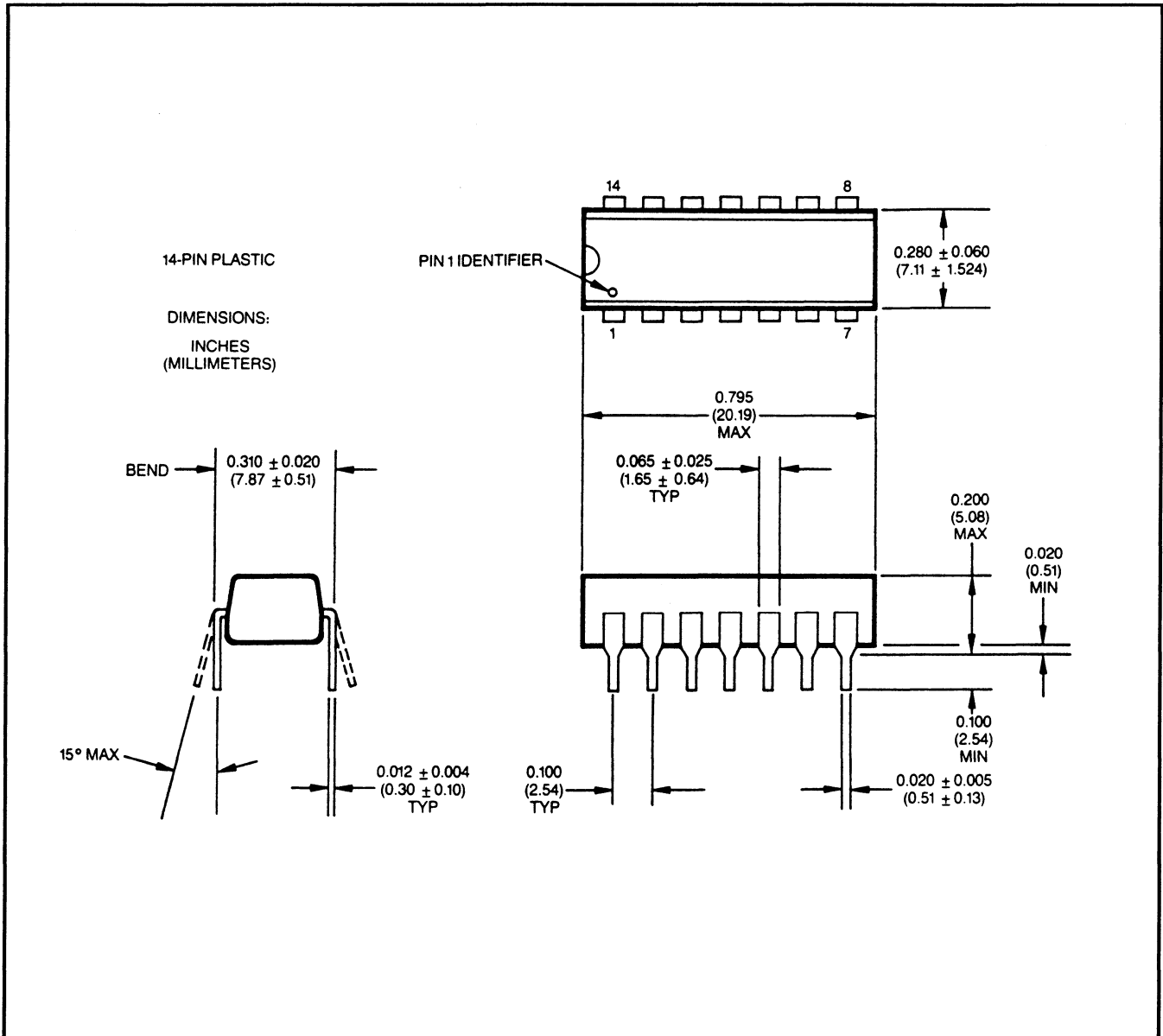
Figure 4 Package Dimensions

Section 7

Sustained Products

M-900 DTMF FILTER AND DECODER SET

The Teltone® M-900 is a two-LSI chip set that decodes Dual-Tone Multifrequency (DTMF) telephone signals. The set consists of a TT6177 DTMF Filter and a TT6174 Digital Tone Receiver, as shown in Figure 1. Input is from Touch-Tone® telephones, radio, prerecorded tape, or other sources. Output formats are 2 of 8, 1 of 12, binary, or blank. Outputs drive CMOS, low-power Schottky TTL, or transistor drivers.

The set includes a buffer amplifier, dial tone filter, bandsplit filters, and a crystal-controlled digital frequency detector capable of detecting all 16 DTMF digits. A dial pulse counter detects rotary dial digits. The set can be programmed to accept DTMF signals only, rotary dial pulses only, or mixed DTMF and rotary dial input. DTMF signaling is ideal when long distance audio level transmission is required.

The M-900 is manufactured under U.S. Patent 4,145,576.

Features
* Meets CEPT overall performance requirement of less than one false operation per 10,000 digits dialed
* Meets CCITT recommendations for tone receivers
* Provides superior signal-to-noise characteristics and speech immunity
* Flexible gain parameters
* Input filter rejects high-frequency noise
* Buffered clock outputs
* Performance not layout sensitive, no specific trace pattern required between the chips

Telephone Switching Applications
* Central office products
* PBX and intercom systems
* Consumer-oriented special feature phones and systems
* Radio equipment interface to telephone network

Access and Control Applications
* Answering and recording devices
* Radio communication remote switching
* Remote control of machinery or microprocessors
* Monitoring equipment

Data Entry Applications
* Remote computer and peripheral systems interface
* Consumer credit and shopping systems
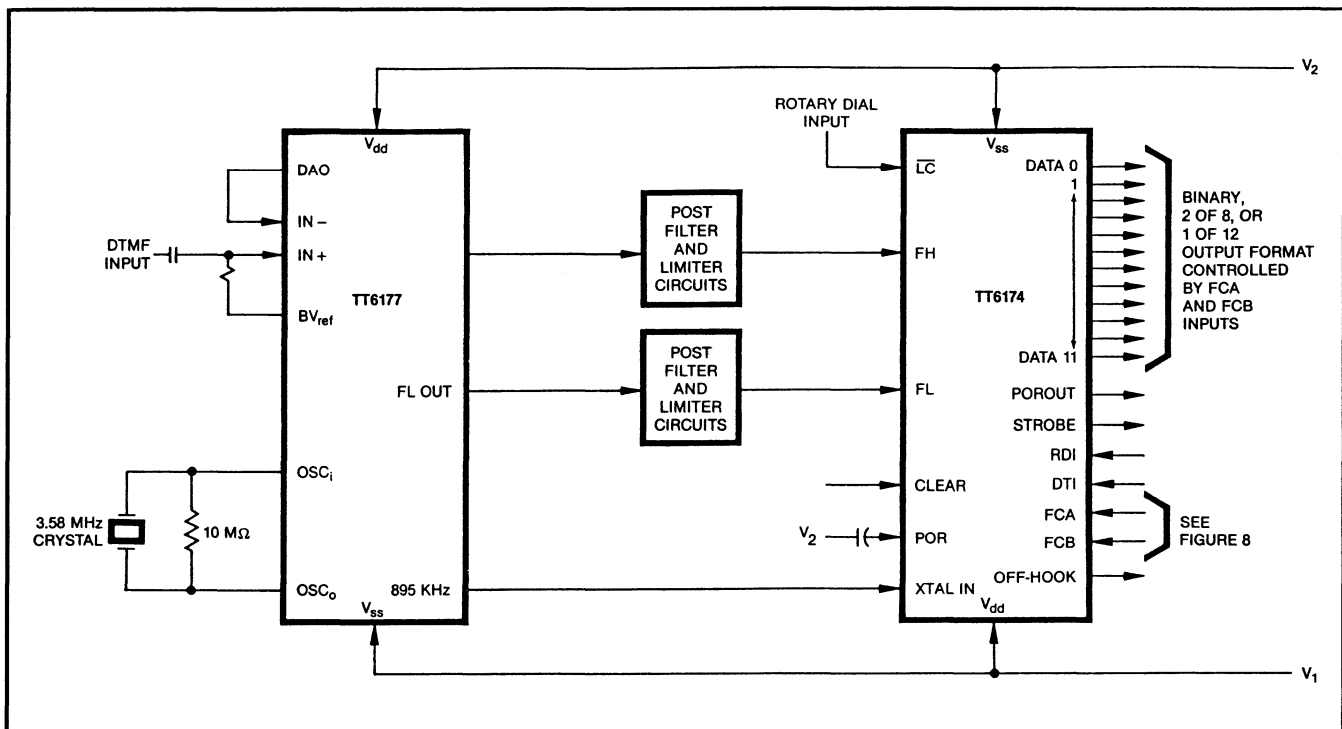* Telephone banking, credit, and bill-paying systems

Figure 1   Block Diagram
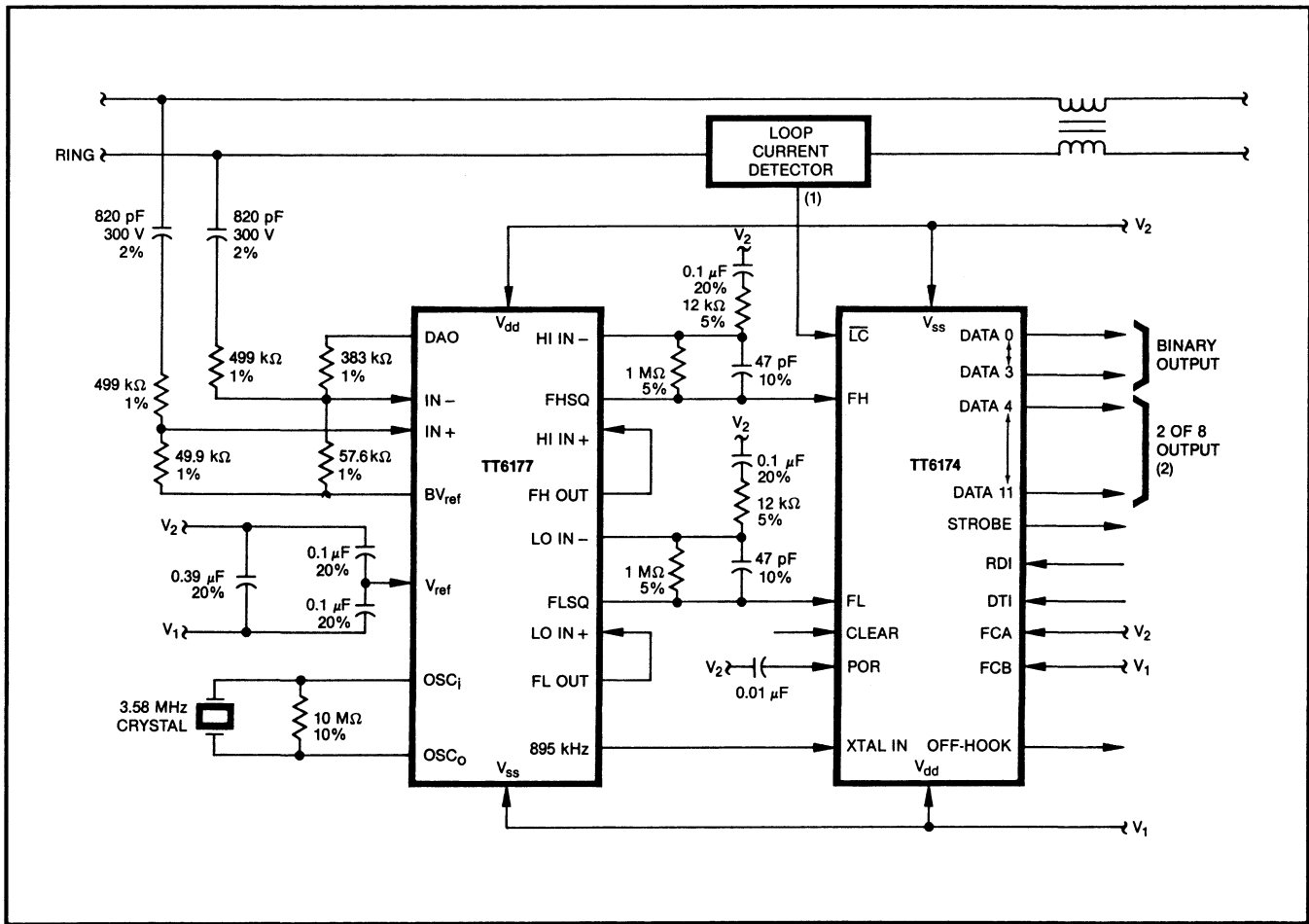
Figure 2 M-900 Typical Application

Table 1 Ordering Information

Ordering Number	Description	Part Number
M-900-01	TT6174-03 Receiver, 40-Pin Plastic TT6177-01 Filter, 18-Pin Plastic	617-00004-03 617-00007-01
M-900-02	TT6174-11 Receiver, 28-Pin Plastic TT6177-01 Filter, 18-Pin Plastic	617-00004-11 617-00007-01
M-900-03	TT6174-04 Receiver, 40-Pin Cer-DIP TT6177-02 Filter, 18-Pin Cer-DIP	617-00004-04 617-00007-02
M-900-04	TT6174-12 Receiver, 28-Pin Cer-DIP TT6177-02 Filter, 18-Pin Cer-DIP	617-00004-12 617-00007-02

Table 2 Typical Application Specifications

Parameter	Typical (Note 1)	Units	Conditions
Input Impedance	500	k ohm	at 1 kHz
Common Mode Noise, 15 Hz to 100 Hz	60	Vrms	
Dial Tone Tolerance	-5	dBm	$f \le 500$ Hz
Precise Dial Tone Tolerance	0	dBm	each tone, 350 Hz and 440 Hz
Signal Detect Level	-30 to $+6$	dBm	per tone
Signal Reject Level	-40	dBm	per tone
Twist	± 10	dB	
Signal-to-Noise Ratio	15	dB	Note 2
Signal Detect Time	38	ms	
Signal Reject Time	27	ms	
Interdigital Pause Detect Time	35	ms	
Interdigital Pause Reject Time	22	ms	

NOTES:
1. These values may vary with your particular circuit arrangements.
2. With the signal level -25 dBm per tone, the signal 50 ms on and 50 ms off, no twist or frequency deviation, all 16 digits signalled randomly, 0 thru 3 kHz flat Gaussian noise, and an error rate of less than one in 10,000. This is essentially the test method of EIA, USITA, and AT & T.

TT6177 Filter

Features

- Internal input amplifier accepts either differential or single-ended signals and provides programmable gain
- Uncommitted op-amps available for use as limiters with programmable gain
- Buffered reference voltage internally derived and externally available
- Greater than 50 dB rejection of each precise dial tone component (350 and 440 Hz)
- Greater than 15 dB of attenuation at 600 Hz
- Greater than 30 dB of intergroup attenuation
- Single or dual power supply operation

Functional Description

As shown in Figure 4, the TT6177 consists of clock circuits, an analog ground circuit, and a multistage DTMF filter circuit with optional limiters.

The clock circuits require only a low-cost 3.579545 MHz television color burst crystal and a 10-megohm resistor as external components. The 149.148 kHz and 27.965 kHz clocks provide the sampling frequencies for the switched-capacitor filter circuits. The buffered 894.886 kHz clock is used to drive the TT6174 Receiver.

The analog ground circuit provides the buffered reference voltage for the switched-capacitor filter circuits. If required, the external capacitors shown in Figure 2 may be added to reduce noise on V_{ss} and V_{dd}. The buffered reference voltage is available externally to bias the Tip and Ring inputs to the DTMF filter and can serve as a reference to compatible external circuits.

The input stages of the DTMF filter circuit consist of a differential amplifier which provides common mode rejection, a low-pass filter which provides high-frequency noise rejection, and a high-pass filter which provides dial tone rejection. The output stages of the DTMF filter consist of two bandsplit filters for separating the high- and low-group DTMF signal components, two low-pass smoothing filters, and two uncommitted operational amplifiers. When connected as shown in Figure 2, the op-amps provide post filtering, gain, and square-wave inputs to the TT6174.
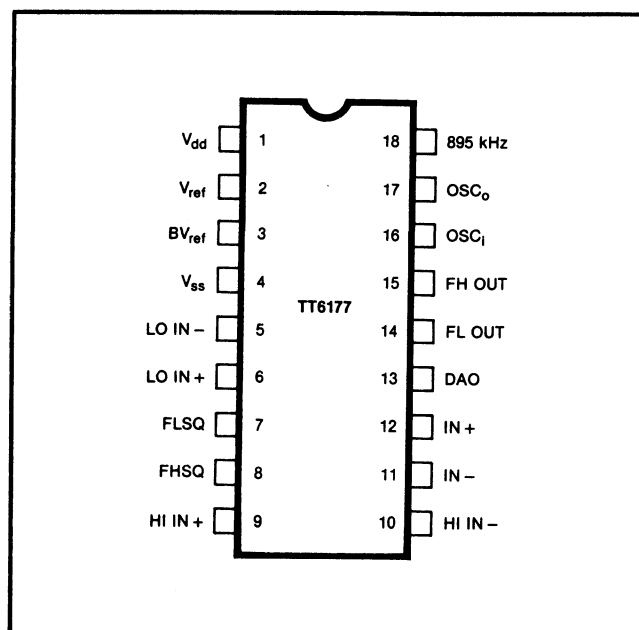
Figure 3 TT6177 Pin Configuration

Table 3 TT6177 Pinouts

Pin Number	Designation	Description	
1	V_{dd}	Positive power supply (+ V)	
2	V_{ref}	Reference voltage (input)	
3	BV_{ref}	Buffered reference voltage (output)	
4	V_{ss}	Negative power supply (– V)	
5	LO IN –	Low group limiter inverting input	These two uncommitted op amps may be used for purposes other than limiting.
6	LO IN +	Low group limiter noninverting input	
7	FLSQ	Low group limiter output	
8	FHSQ	High group limiter output	
9	HI IN +	High group limiter noninverting input	
10	HI IN –	High group limiter inverting input	
11	IN –	Differential amplifier inverting input (Ring)	
12	IN +	Differential amplifier noninverting input (Tip)	
13	DAO	Differential amplifier output	
14	FL OUT	Low group smoothing filter output	
15	FH OUT	High group smoothing filter output	
16	OSC_I	Oscillator input	A 3.579545-MHz crystal in parallel with a 10-megohm resistor completes the internal oscillator.
17	OSC_O	Oscillator output	
18	895 kHz	894.886-kHz clock output for use with the TT6174	

Figure 4 TT6177 Block Diagram
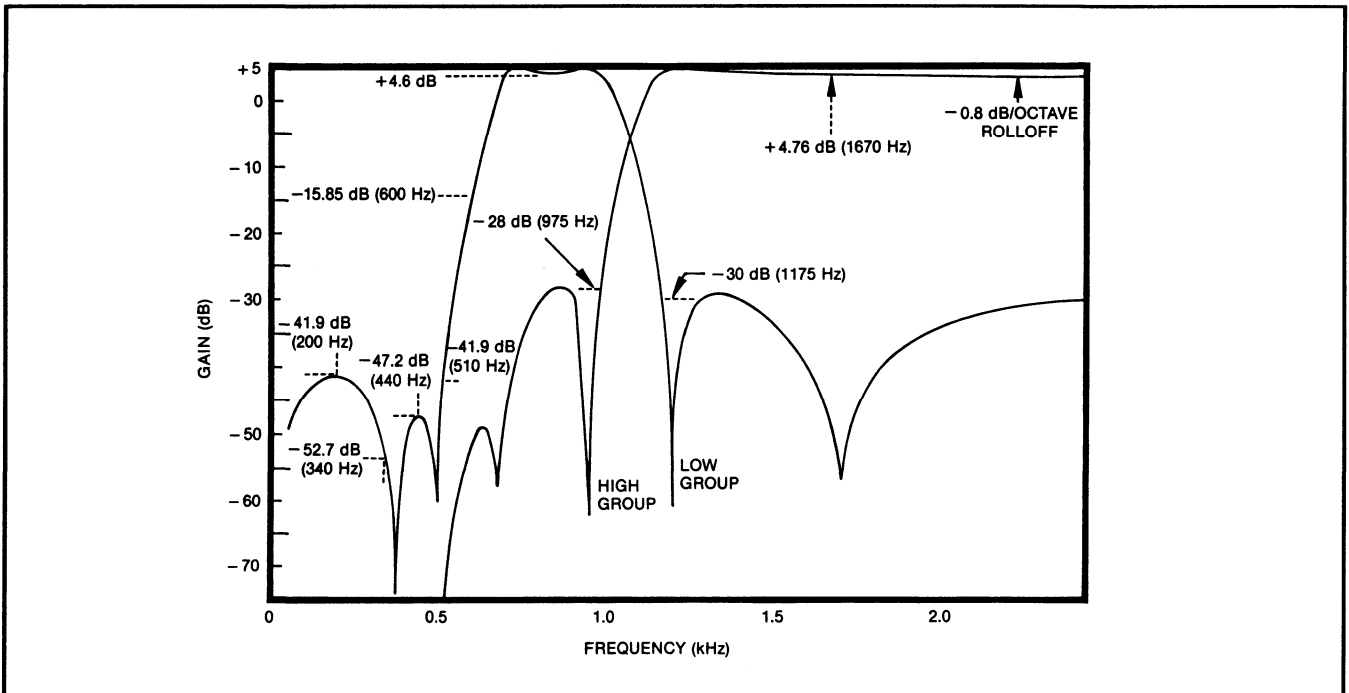
Figure 5 Filter Characteristics

Table 4 TT6177 Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2) . . . . .13.5 V
Power Dissipation . . . . .610 mW
Voltage on Any Pin . . . .$(V_2 + 0.3 \text{ V})$ to $(V_1 - 0.3 \text{ V})$
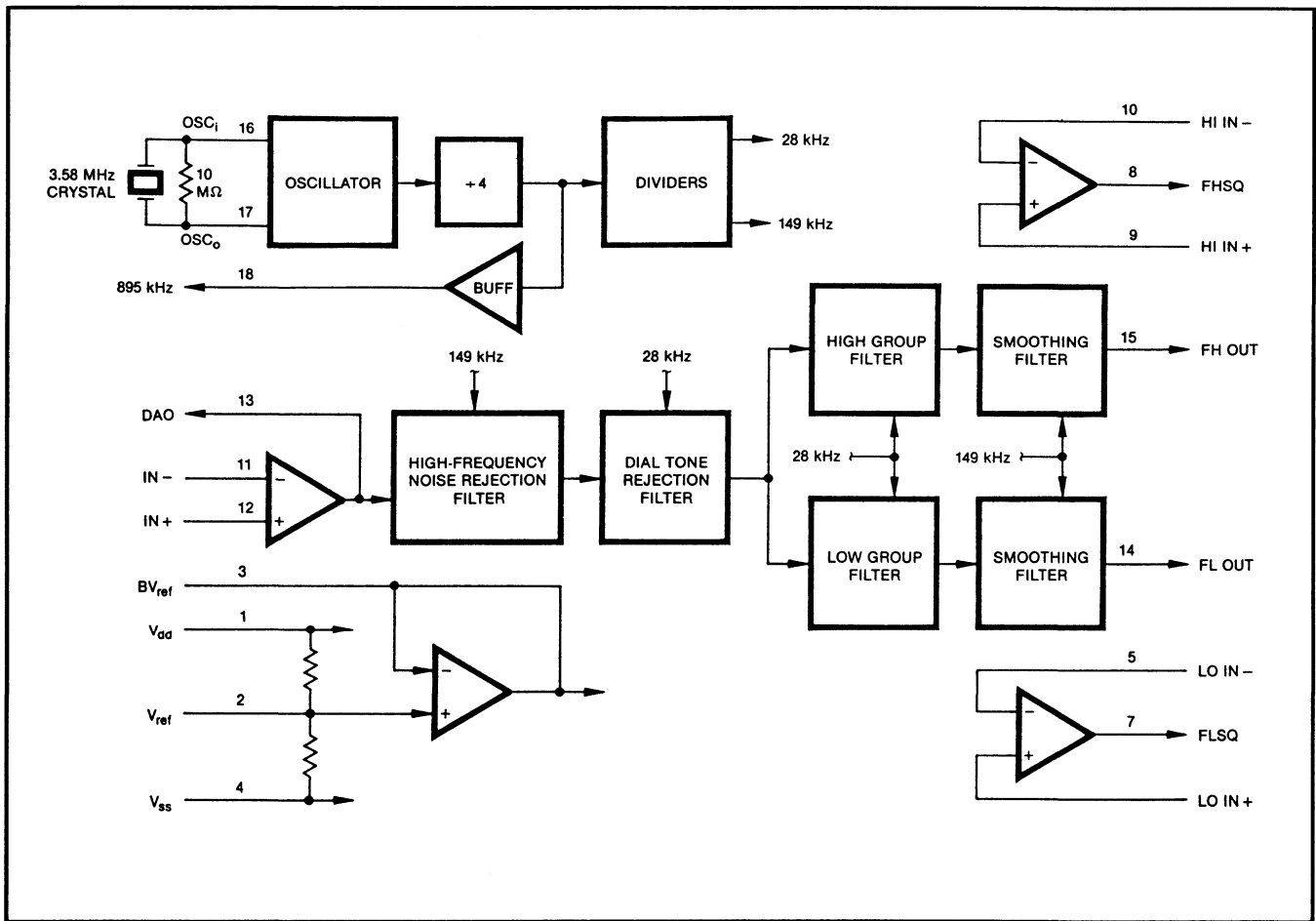Storage Temperature . . . . $-55°$ to $125°C$
Operating Temperature. . . . . $0°$ to $70°C$ ambient air
Lead Soldering Temperature . . . . $260°C$ for 5 seconds at 0.035 inches from package

Notes:
1. Exceeding these ratings may cause permanent damage.
2. V_2 (positive supply) referenced to V_1 (negative supply). V_2 may be at ground.

Table 5 TT6177 DC Electrical Characteristics

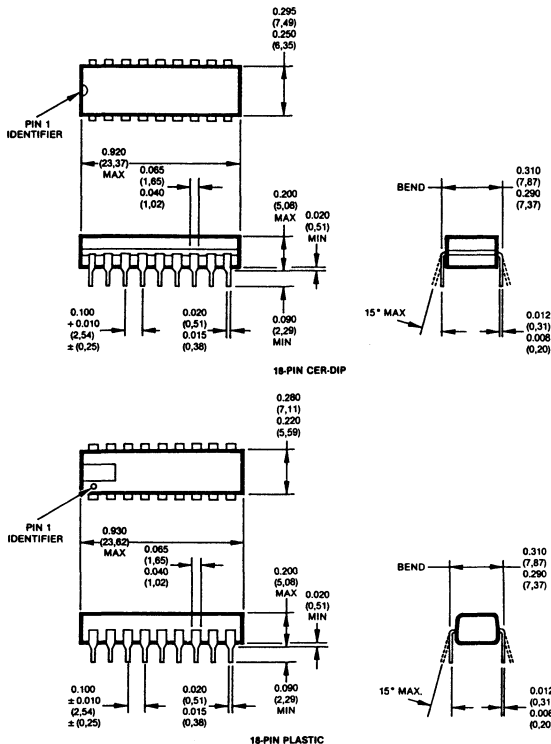|	Parameter	Min	Typ	Max	Units
SUPPLY	Supply Current		30	45	mA
	Supply Voltage	9.5		13.5	V
	BV$_{ref}$	5.9	6.0	6.1	V
	Ripple Voltage			50	mV
OP AMPS (See note)	Input Resistance	10			MΩ
	Input Offset Voltage		10	25	mV
	Output Signal Voltage		1.5	10.5	V
	Common Mode Voltage	1.5		9.5	V
	Output Load Resistance	40			kΩ
	Output Load Capacitance			10	pF

Note:
Op amps include the input differential amplifier single-ended input and the two uncommitted amplifiers connected as limiters in Figure 2.

Table 6 TT6177 AC Electrical Characteristics

	Parameter		Min	Typ	Max	Units	Conditions
FILTER	Distortion Components				-40	dBm	Signal level at Pin 13 (DAO) no greater than $+3$ dBm per tone (Note 1)
	Idle Channel Noise				-57	dBm	
	Low Group Bandwidth	low limit		684		Hz	-2 dB from max
		high limit		957		Hz	-2 dB from max
	High Group Bandwidth	low limit		1188		Hz	-2 dB from max
		high limit		1660		Hz	-2 dB from max
	Inband Ripple				2	dB	
	Intergroup Rejection		31			dB	
	300-450 Hz Dial Tone Rejection	low group	50			dB	
		high group	70			dB	
	600 Hz Rejection	low group	15			dB	
		high group	50			dB	
	Passband Gain		5.5	6.0	6.5	dB	Amplitude within 1 dB of final value
	Group Delay			4.5	6	ms	
OP AMPS (Note 2)	Open Loop Gain		80			dB	
	Input Capacitance				15	pF	
	Unity Gain Bandwidth		1.5			MHz	
	Common Mode Rejection		70			dB	

Notes:
1. Voltage levels stated in dBm are obtained using a standard voltmeter calibrated to provide a scaled voltage measurement in dBm for a 600-ohm impedance. No termination should be applied for this measurement.
2. Op amps include the input differential amplifier which can be used with a single-ended input and the two uncommitted amplifiers connected as limiters in Figure 2.

Package Dimensions

Teltone Corporation / 10801-120th Avenue NE, Kirkland, WA 98033   Phone: 1-800-426-3926 or 206-827-9626   Fax: 206-827-6050   TWX: 910-449-2862
Teltone Limited / 3375-14th Avenue, Markham, Ontario, Canada L3R 2L6   Phone: 416-475-0837   Fax: 416-474-9151   Envoy User Name: TTL.HQ

7-5

TT6174 Tone Receiver

Features

- Decodes all 16 DTMF digits
- Provides fully time-guarded rotary dial pulse counting
- Three different enable/disable inputs
- Digit presence outputs
- Selectable output formats
- Precision clock outputs

Functional Description

As shown in Figure 9, the TT6174 consists of a multistage digit validation circuit, digit presence logic, an output register/decoder, and a clock circuit. See Table 7 for a complete description of all inputs and outputs.

The digit validation circuit consists of a control stage which enables or inhibits other receiver circuits as determined by its inputs, a DTMF stage which compares the FLSQ and FHSQ outputs of the TT6177 Filter with internal models of the DTMF frequencies, and a rotary dial stage which times and counts makes and breaks of loop current. Detection of a valid digit causes an indication of the digit's presence to be forwarded to the digit presence logic and the identity of the digit to be forwarded to the output register/decoder. The output register/decoder translates the digit into the output format specified by the FCA and FCB inputs. See Figure 8. The 895 kHz output from the TT6177 Filter drives the clock circuit of the TT6174, which in turn provides outputs for use by other devices.
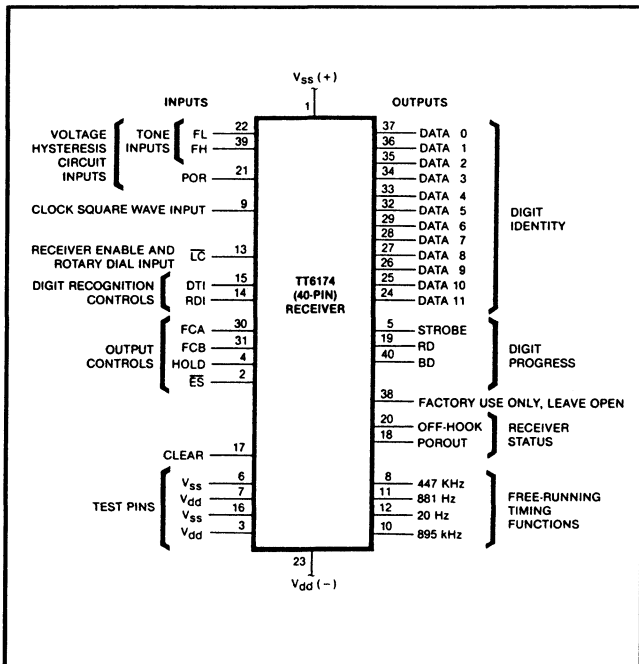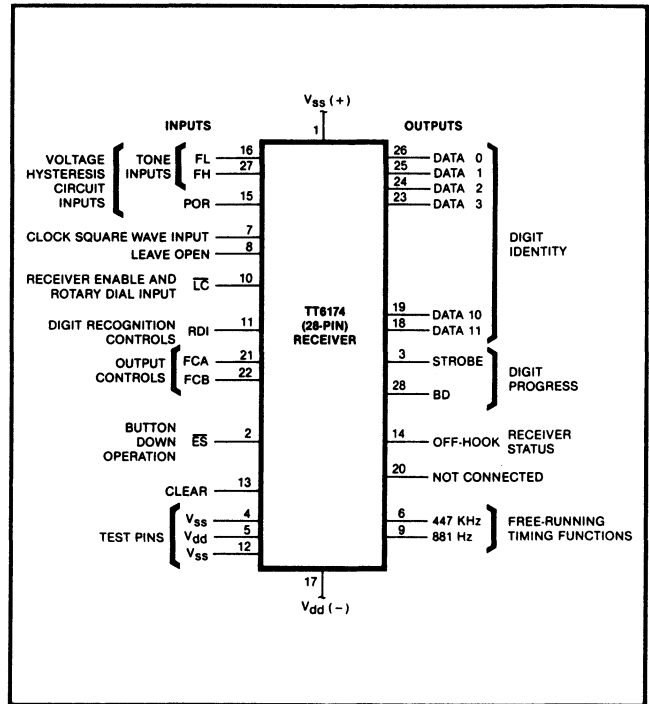
Figure 7 28-pin Receiver Configuration
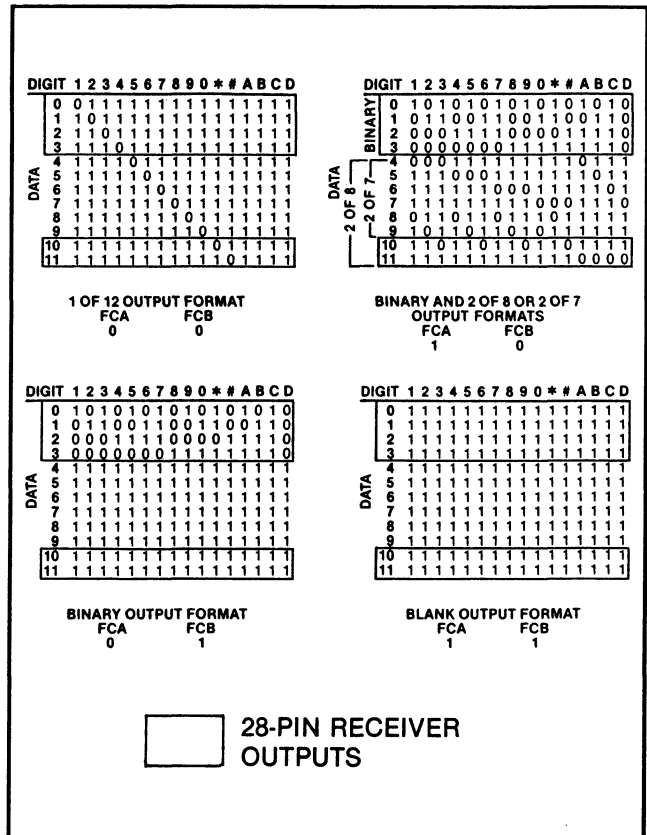
Figure 6 40-pin Receiver Configuration

Figure 8 Output Formats
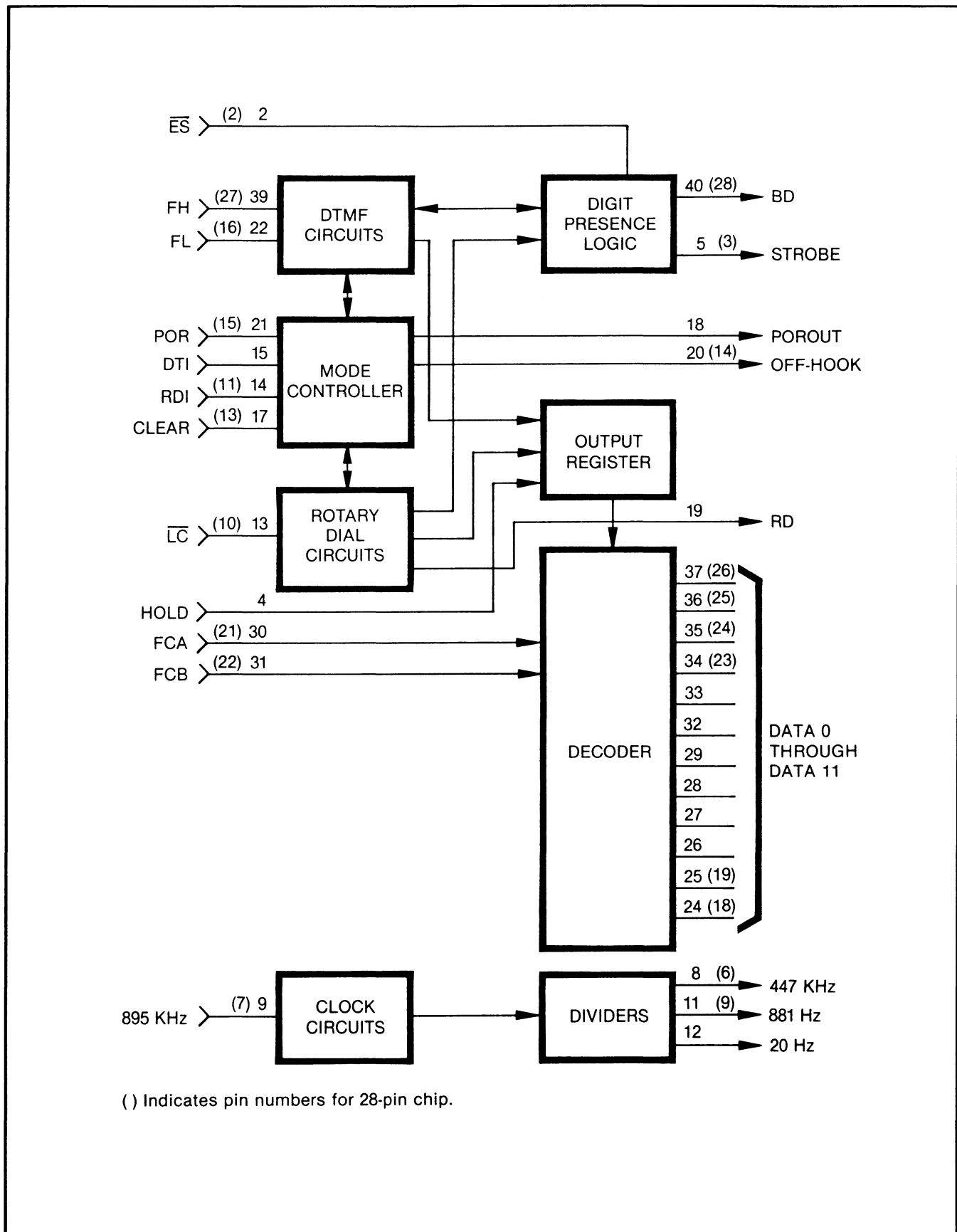
Figure 9 TT6174 Block Diagram

Table 7 TT6174 Pinouts (Part 1 of 2)

Pin Number	Mnemonic	Description
1 (1)	V_{SS}	Positive power supply (V_2)
2 (2)	$\overline{ES}$	Early Split Not input. When pulled to logic 0 (V_1), ES enables the early tone presence (BD) output.
3		Connect to logic 0.
4	HOLD	Input. For applications where the output data has to remain unchanged for an extended time period, whether or not additional digits have been received, pull HOLD to logic 1 after STROBE goes to logic 1.
5 (3)	STROBE	Valid data output. When DTMF digits are being detected, STROBE goes to the logic 1 state 10 microseconds after the DATA outputs change and returns to the logic 0 state 25 milliseconds (ms) after the end of DTMF detection. When rotary dial digits are being detected, STROBE goes to logic 1 for 200 ms after the interdigital pause is recognized. To read DATA during DTMF signal presence, use the leading edge of STROBE (button-down operation). To read DATA after DTMF signal presence, use the trailing edge of STROBE (button-up operation).
6 (4)		Test input. Connect to logic 1.
7 (5)		Test input. Connect to logic 0.
8 (6)	447 kHz	50-percent duty cycle, PMOS logic level signal for external use. Actual frequency is the clock frequency divided by 2.
9 (7)	CLOCK IN	895-kHz input from the TT6177 Filter.
10 (8)	XTAL OUT	Not used. Leave open.
11 (9)	881 Hz	50-percent duty cycle, PMOS logic level signal for external use. Actual frequency is the clock frequency divided by 1016.
12	20 Hz	50-percent duty cycle, PMOS logic level signal for external use. Actual frequency is the clock frequency divided by 44,704.
13 (10)	$\overline{LC}$	Loop Current Not input. $\overline{LC}$ is both a receiver enable/disable input and the rotary dial pulse input. The TT6174 interprets a logic 0 as an off-hook condition, interdigital pause, or a make period. The TT6174 interprets a logic 1 as an on-hook condition or break period. For DTMF operation only, $\overline{LC}$ can be connected to V_1; then, with POR connected as described below, the receiver is enabled as long as CLEAR is at logic 0.
14 (11)	RDI Rotary Dial Inhibit Input	For mixed DTMF and rotary dial operation, connect DTI and RDI to logic 0. For rotary dial operation only, connect DTI to logic 1. For DTMF operation only, connect RDI to logic 1. For mode locking on the first digit detected, connect both DTI and RDI to STROBE. The mode lock will be held until the detection circuits are reset.
15	DTI DTMF Inhibit Input	
16 (12)		Test input. Connect to logic 1.
17 (13)	CLEAR	Receiver enable/disable input. A logic 1 applied to the CLEAR input instantaneously resets all detection circuits and forces the DATA outputs to the "D" column of the currently enabled output format (see Figure 8).
18	POROUT	POR output. Responds to input on POR pin.
19	RD	Rotary Dial output. RD provides an early dial pulse presence signal that starts at the leading edge of the first break pulse and ends 100 ms after the trailing edge of the last pulse.
20 (14)	OFF-HOOK	Output. OFF-HOOK goes to the logic 1 state 100 ms after $\overline{LC}$ is pulled to logic 0. OFF-HOOK goes to the logic 0 state 300 ms after $\overline{LC}$ is pulled to logic 1.
21 (15)	POR	Power-On Reset, receiver enable/disable input. A 0.01 µF capacitor connected to V_2 and POR (see Figure 2) causes POROUT to go to logic 1 (V_2) for approximately 10 ms after power is applied. This pulse resets all detection circuits and forces the DATA outputs to the "D" column of the currently enabled output format (see Figure 8).
22 (16)	FL	FLSQ input from the TT6177 Filter
23 (17)	V_{dd}	Negative power supply (V_1)
24 (18)	DATA 11	
25 (19)	DATA 10	
26	DATA 9	Data outputs. See Figure 8 for the outputs associated with each output format. A DTMF digit is outputted when it has persisted for 35 ms. A rotary dial digit is outputted when an interdigital pause is recognized.
27	DATA 8	
28	DATA 7	
29	DATA 6	
(20)		Not used.
30 (21)	FCA Format Control A input	As shown in Figure 8, FCA and FCB determine the DATA output format. FCA and FCB can also be used as a data strobe. By holding both inputs at logic 1, all data outputs will remain at logic 1 until FCA and/or FCB are pulled to logic 0.
31 (22)	FCB Format Control B input	

Note: Pin numbers for 28-pin receivers are shown in parentheses.

Table 7 TT6174 Pinouts (Part 2 of 2)

Pin Number	Mnemonic	Description
32	DATA 5	
33	DATA 4	
34 (23)	DATA 3	See description to DATA 6 through 11.
35 (24)	DATA 2	
36 (25)	DATA 1	
37 (26)	DATA 0	
38		Leave open.
39 (27)	FH	FHSQ input from the TT6177 Filter
40 (28)	BD	Button Down output. When enabled by $\overline{ES}$ being at logic 0, BD goes to the logic 1 state within 16 ms after a tone pair is detected. BD then returns to the logic 0 state 25 ms after the tone pair ends.

1. TO TTL OR CMOS AT A LOWER SUPPLY VOLTAGE

2. TO LOW POWER SCHOTTKY TTL

3. TO RELAYS OR DISPLAYS (NEGATIVE SUPPLY)

4. TO TRANSISTOR DRIVERS

5. (NOT SHOWN) TO CMOS AT THE SAME SUPPLY VOLTAGE—INTERFACE DIRECTLY (ALL OUTPUTS)
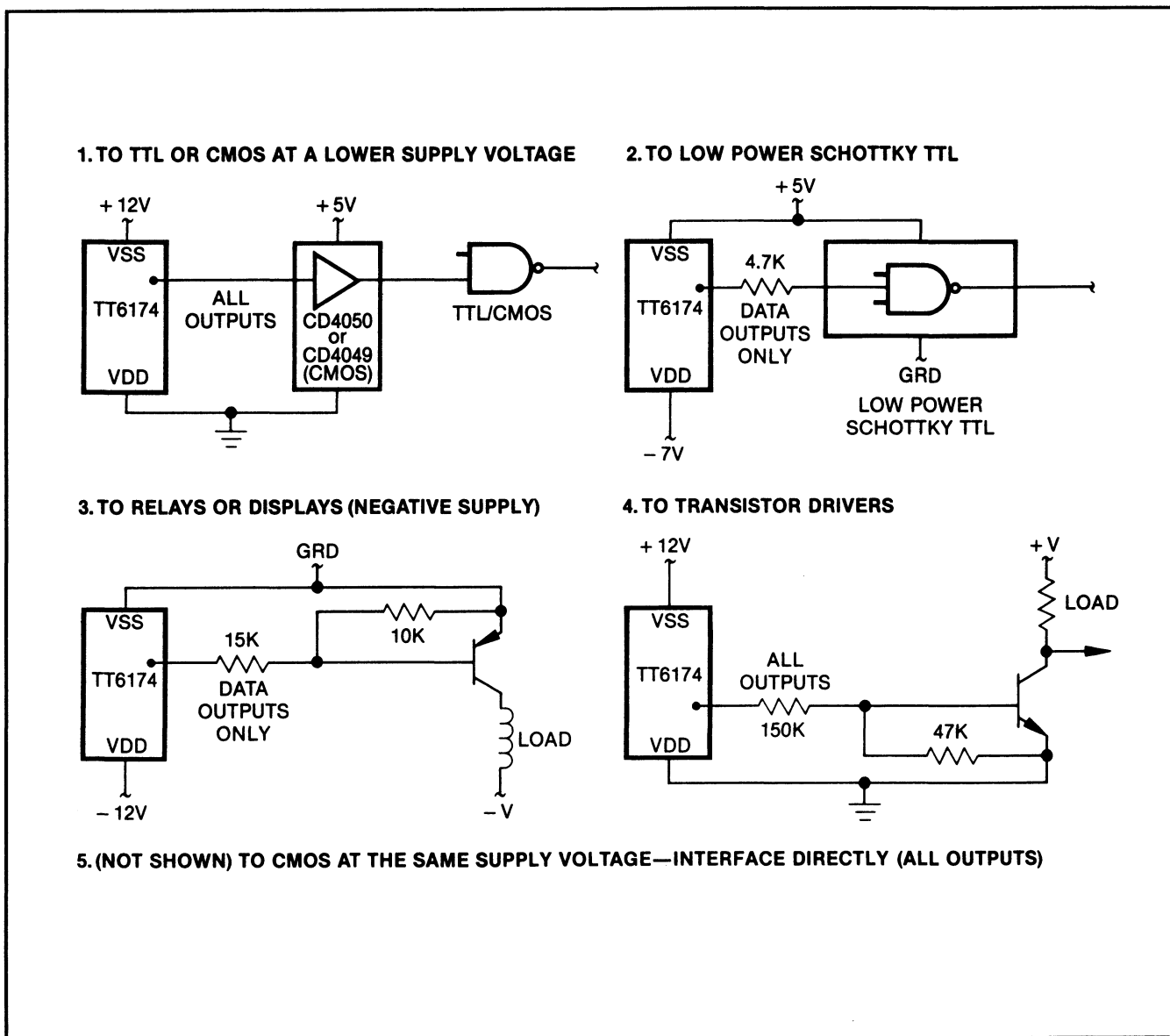
Figure 10 Output Interface Techniques

Table 8 TT6174 Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2) . . . . .14.5 V
Power Dissipation . . . . .600 mW
Voltage on Any Pin . . . . $(V_2 + 0.3\ V)$ to $(V_1 - 0.3\ V)$
Storage Temperature . . . .$-40°$ to $150°$ C
Operating Temperature. . . . .$0°$ to $70°$ C ambient air
Lead Soldering Temperature . . . . $260°$ C for 5 seconds at 0.035 inches from package

Notes:
1. Exceeding these ratings may cause permanent damage.
2. V_2 (positive supply) referenced to V_1 (negative supply). V_2 may be at ground.

Table 9 TT6174 DC Electrical Characteristics

	Parameter	Min	Typ	Max	Units	Conditions
Supply Requirements	Supply Voltage	$+11$	$+12$	$+14.5$	V	V_2 referenced to V_1 (Note 1)
	Ripple Voltage			250	mV	Measured peak-to-peak at 120 Hz
	Supply Current		25	35	mA	14.5 V at 0°C
Logic Inputs	Logic 0 Level			$V_1 + 3.2$	V	
	Logic 1 Level	$V_2 - 2.5$			V	
	Capacitance			15	pF	
	Input Current (Note 2)			50	μA	
Analog Inputs	Logic 0 Threshold	0.57 (ΔV)	0.65 (ΔV)	0.73 (ΔV)	V	$\Delta V = V_2 - V_1$
	Logic 1 Threshold	0.43 (ΔV)	0.35 (ΔV)	0.27 (ΔV)	V	$\Delta V = V_2 - V_1$
	Capacitance			15	pF	
	Input Current (Note 2)			±50	μA	
Data Outputs	Logic 0 Current Sink			1	mA	Output at $V_1 + 7$ V
	Logic 1 Current Source			100	μA	Output at $V_2 - 2$ V
Non-Data Outputs	Logic 0 Current Sink			100	μA	Output at $V_1 + 2$ V
	Logic 1 Current Source			100	μA	Output at $V_2 - 2$ V

Notes:
1. V_2 more positive than V_1. V_2 may be at ground.
2. The load current must be sourced or sunk to drive an input to its opposite state.

Table 10 TT6174 AC Electrical Characteristics

	Parameter	Min	Typ	Max	Units	Conditions
FL and FH Inputs	Signal Detect Time	27		30	ms	
	Interdigital Pause Detect Time (Note 1)	26		34	ms	
	Interdigital Pause Reject Time (Note 1)	26			ms	
	Signal Detect Bandwidth	-1.5% -2 Hz		$+1.5\%$ $+2$ Hz	Hz	Of each nominal DTMF frequency
	Signal Reject Bandwidth	-3.5%		$+3.5\%$	Hz	Of each nominal DTMF frequency
Inputs Other Than FL and FH	Pulse Width Required to Reset with CLEAR or POR Inputs			25	μs	
	Off-Hook Recognition	95	100	105	ms	$\overline{LC}$ at Logic 0
	Off-Hook Blanking (Note 2)	285	300	315	ms	$\overline{LC}$ at Logic 0
	Break Recognition	24.5		29.5	ms	$\overline{LC}$ at Logic 1
	Make Recognition	7	9	11	ms	$\overline{LC}$ at Logic 0
	End of Digit Recognition	95	100	105	ms	$\overline{LC}$ at Logic 0
	Rotary Interdigital Blanking	190	200	210	ms	
	On-Hook Recognition	290	300	310	ms	$\overline{LC}$ at Logic 1
Available Frequencies	447.433 kHz Pulse Width	2.232	2.234	2.237	μs	
	881 Hz Pulse Width	0.567	0.568	0.569	ms	
	20 Hz Pulse Width (Note 3)	24.95	24.98	25	ms	

Notes:
1. The Interdigital Pause Detect Time is that interval of loss of tones after which the return of the valid tone pair is considered a new digit. The Interdigital Pause Reject Time is the interval a valid tone pair can be interrupted without being treated as a new digit when it returns.
2. Off-Hook Blanking is the delay between $\overline{LC}$ going to logic 0, from being at logic 1 longer than 300 ms, and enabling the digit detection circuits.
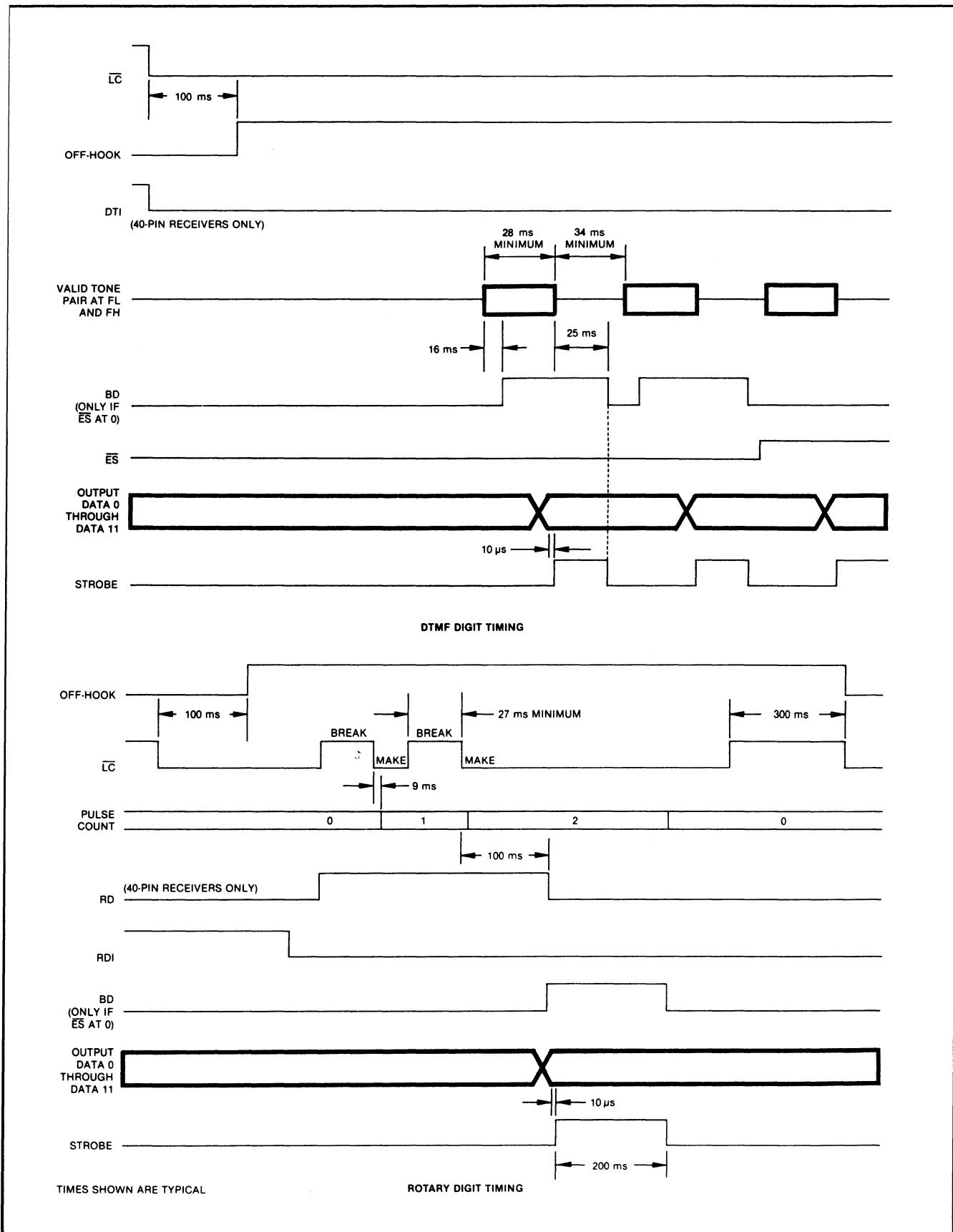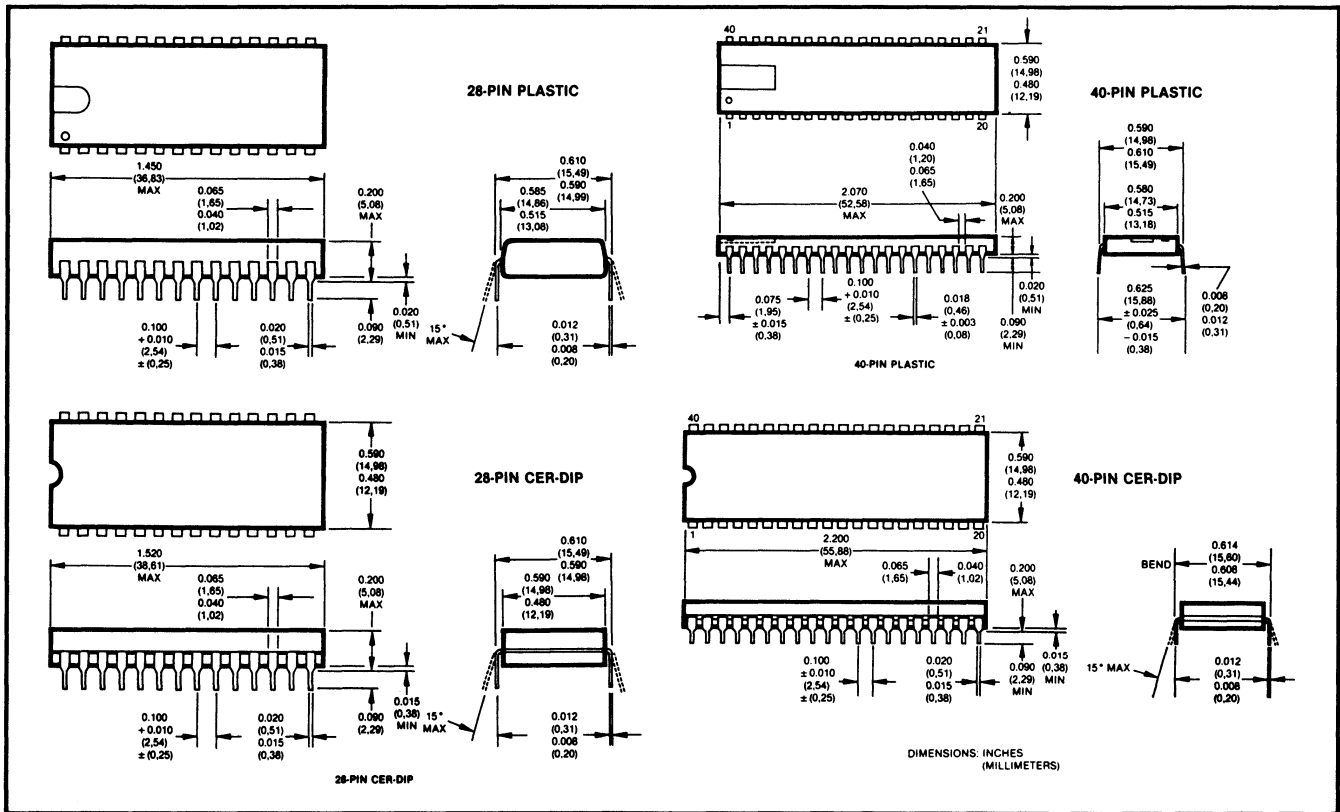3. 40-pin receivers only.

Figure 11 Timing Diagram

TIMES SHOWN ARE TYPICAL

DTMF DIGIT TIMING

ROTARY DIGIT TIMING

Figure 12   Package Dimensions

M-907 TONE DETECTOR AND ROTARY DIAL PULSE COUNTER

The Teltone® M-907 Receiver Assembly is designed for applications where a high-performance **central office grade** Touch-Tone (DTMF, Dual-Tone Multifrequency) and/or a rotary dial pulse counter is required. The receiver's compact size and low heat emission make it well suited for high-density packaging.

The receiver consists of a bridging buffer amplifier, dial tone filters, both high- and low-pass filters, dual limiters, and a crystal-controlled digital frequency detector capable of detecting all 16 DTMF digits. A dial pulse counter detects rotary dial digits. Figure 1 displays the functional block diagram. The unit can be programmed to accept DTMF signals only, rotary dial pulses only, or to provide mixed DTMF and rotary dial operation with the further capability of cross-inhibiting as determined by the first digit received.

Data outputs will interface with MOS or CMOS and will also drive one low-power Schottky TTL gate or low-power transistor. The externally selectable outputs are available in 2 of 8 or 2 of 7 (as described in Table 1), binary, or 1 of 12 formats. Figure 2 displays the outputs available. A number of options are available to answer a wide variety of requirements, such as strobing by external equipment. See Table 2.

The M-907 is manufactured under U.S. Patent 4,145,576

Features

- A complete LSI digital Touch-Tone® detector and rotary dial counter contained in an assembly requiring less than 4.52 x 3.02 x 0.6 inches (115 x 76.25 x 15.24 millimeters).
- Meets or exceeds telephone central office requirements for DTMF recognition and voice talkoff protection.
- Fully time-guarded rotary dial pulse counting.
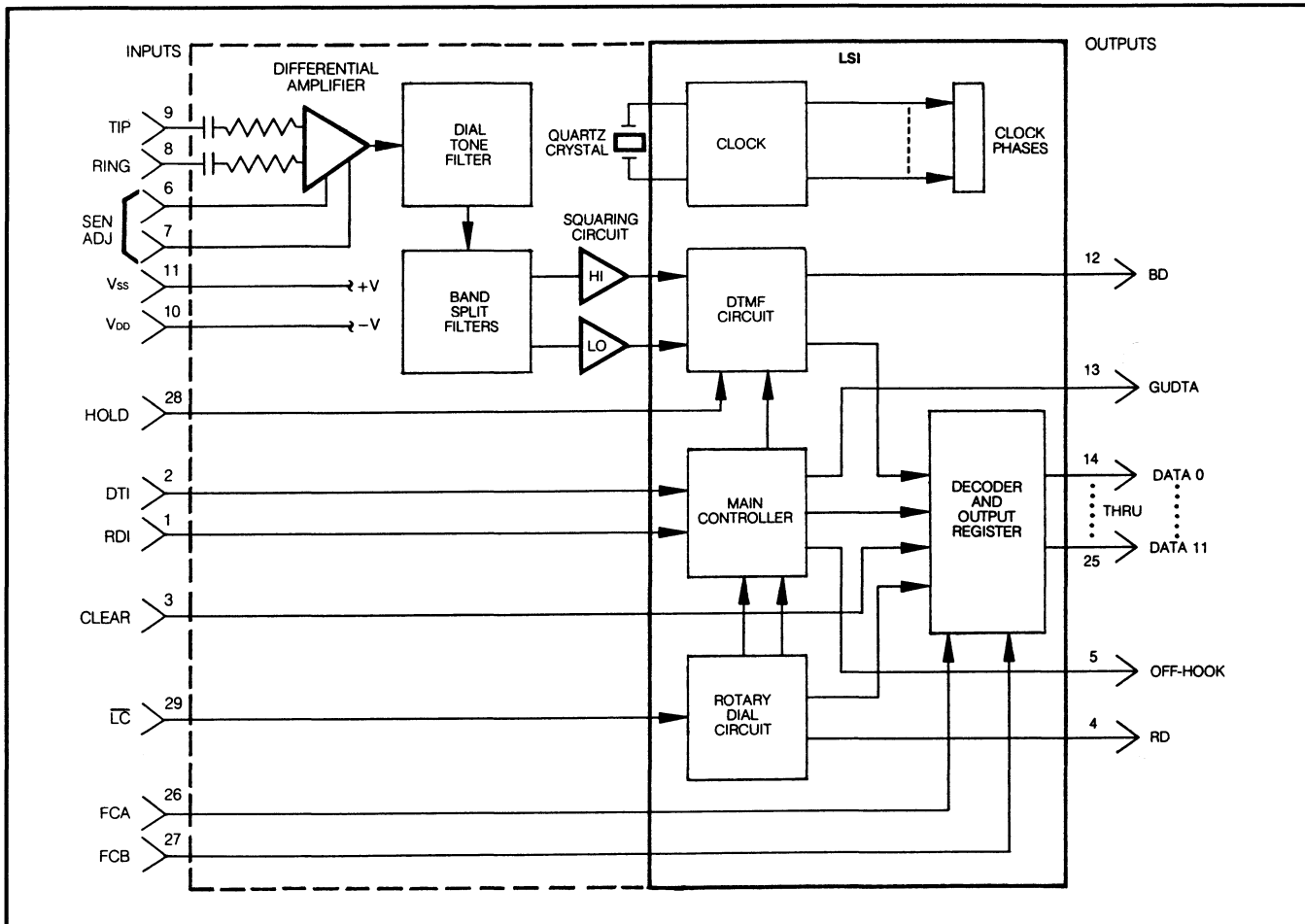- Decodes all 16 DTMF digits and counts rotary dial digits.

Figure 1 Block Diagram

- Crystal-controlled LSI digital circuitry assures maximum frequency detection accuracy and stability.
- Provision for tone detection sensitivity adjustment.
- Selectable output formats of binary, 2 of 8 (2 of 7), and 1 of 12.
- Selectable button-up or button-down operation.
- Separate outputs indicate dial pulse or early tone presence.
- Low power consumption: Typically 60 mA at 12 VDC.

Applications

- PBX and central office receivers
- Data transmission
- Tone and/or rotary dial controlled dictation links
- Radio telephone systems
- Other applications using a telephone dialing mechanism or analogous device to convey information

Table 1 DTMF Signal Format

HIGH GROUP OF FREQUENCIES

LOW GROUP OF FREQUENCIES

	H1 1209	H2 1336	H3 1477	H4 1633
L1 697	1	ABC 2	DEF 3	A
L2 770	GHI 4	JKL 5	MNO 6	B
L3 852	PRS 7	TUV 8	WXY 9	C
L4 941	✳	0	#	D

Note: A valid digit always contains one low tone and one high tone. This combination is often called 2 of 7 or 2 of 8. 1633 Hz is not present on 2 of 7 installations.
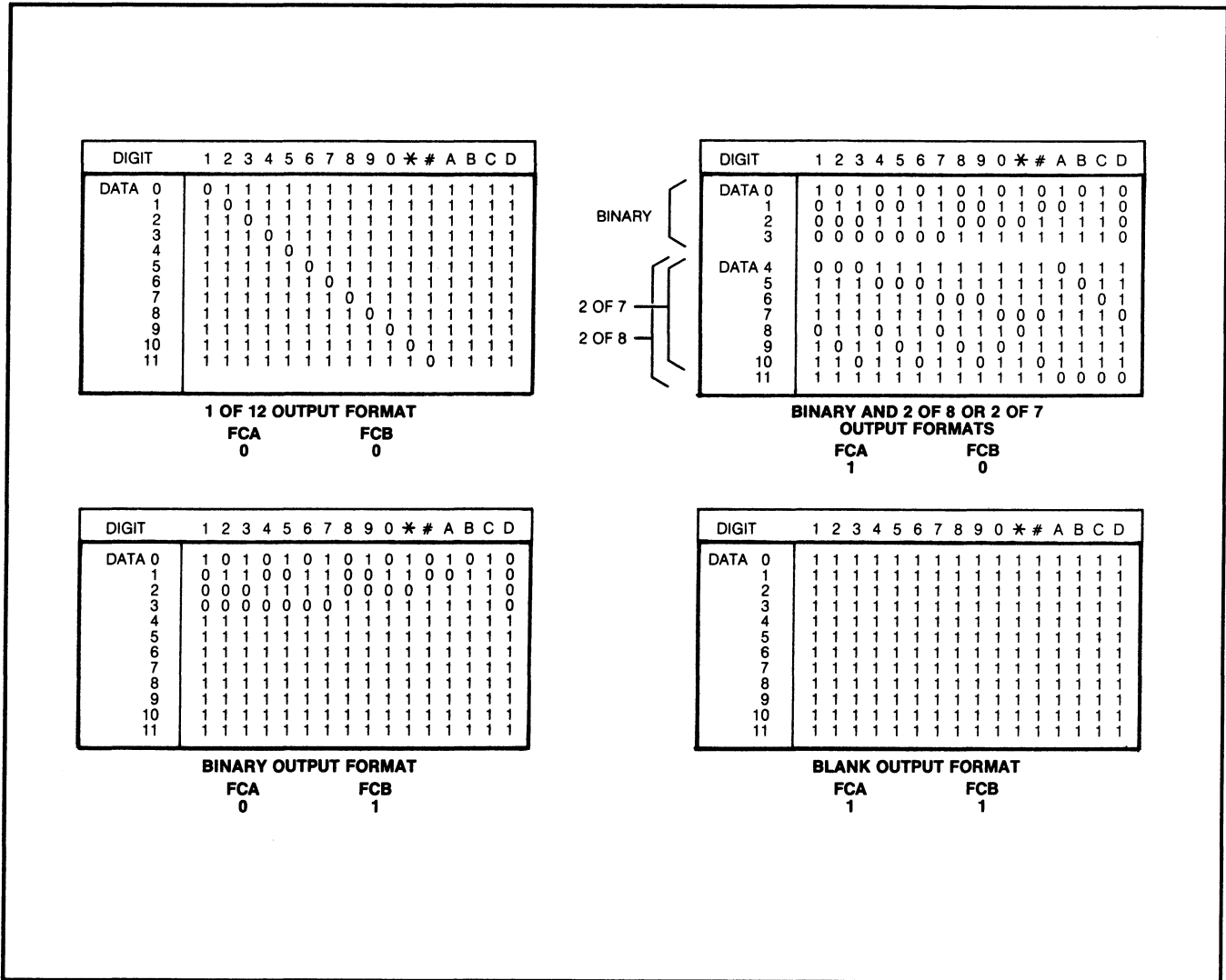
1 OF 12 OUTPUT FORMAT — FCA 0, FCB 0

DIGIT	1	2	3	4	5	6	7	8	9	0	✳	#	A	B	C	D
DATA 0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
3	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
4	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
5	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
6	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
7	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
8	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
9	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
10	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
11	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1

BINARY AND 2 OF 8 OR 2 OF 7 OUTPUT FORMATS — FCA 1, FCB 0

DIGIT	1	2	3	4	5	6	7	8	9	0	✳	#	A	B	C	D
DATA 0 (BINARY)	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
2	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
3	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
DATA 4 (2 OF 7)	0	0	0	1	1	1	1	1	1	1	1	1	0	1	1	1
5	1	1	1	0	0	0	1	1	1	1	1	1	1	0	1	1
6	1	1	1	1	1	1	0	0	0	1	1	1	1	1	0	1
7	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	0
8 (2 OF 8)	0	1	1	0	1	1	0	1	1	1	0	1	1	1	1	1
9	1	0	1	1	0	1	1	0	1	0	1	1	1	1	1	1
10	1	1	0	1	1	0	1	1	0	1	1	0	1	1	1	1
11	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0

BINARY OUTPUT FORMAT — FCA 0, FCB 1

DIGIT	1	2	3	4	5	6	7	8	9	0	✳	#	A	B	C	D
DATA 0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
2	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
3	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

BLANK OUTPUT FORMAT — FCA 1, FCB 1

DIGIT	1	2	3	4	5	6	7	8	9	0	✳	#	A	B	C	D
DATA 0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 2 Output Formats

Table 2 Pin Functions

Pin	Number	Function
BD	12	Button Down. Output. The BD option provides an early tone presence signal that starts 16 ms after a valid tone pair is detected and ends ~25 ms after the tone pair ends. See Figure 5. The BD output also appears at the same time as GUDTA when a rotary digit is accepted.
RD	4	Rotary Dial. Output. The RD option provides an early dial pulse presence signal that starts at the leading edge of the first break pulse and ends 100 ms after the trailing edge of the last pulse. See Figure 6.
$\overline{LC}$	29	Loop Current Not. Input. The $\overline{LC}$ input is the rotary dial pulse input lead. A logic 0 (-V) represents an off-hook condition or a make period. A logic 1 (+V) represents an on-hook condition or break period. For DTMF operation only, $\overline{LC}$ can be connected to (-V); then the receiver is enabled as long as the CLEAR input is at logic 0.
OFF-HOOK	5	Output. The off-hook output goes high (logic 1) 100 ms after the $\overline{LC}$ input goes low. The output goes low (logic 0) 300 ms after the $\overline{LC}$ input goes high.
DTI and RDI	2 and 1	Dual Tone Inhibit and Rotary Dial Inhibit. Input. For mixed DTMF and rotary dial operation, connect DTI and RDI to (-V). For rotary dial operation only, connect DTI to (+V). For DTMF operation only, connect RDI to (+V). For mode locking on the first digit detected, connect both DTI and RDI to GUDTA. The mode lock will be held until an on-hook condition occurs or a logic 1 is applied to the CLEAR input.
HOLD	28	Input. For applications where the output data has to remain unchanged for an extended time period, whether or not additional digits have been received, switch HOLD to logic 1 after GUDTA occurs.
CLEAR	3	Input. A logic 1 applied to the CLEAR input will instantaneously reset the Receiver's DTMF and rotary dial detection circuits. All DATA outputs will be forced to the condition shown in the D state columns (rightmost) as conditioned by the logic levels on FCA and FCB. See Figure 2.
FCA and FCB	26 and 27	Format Control A and B. Input. The format control inputs determine the DATA output format. Figure 2 displays the various outputs available, as determined by the logic levels at FCA and FCB. FCA and FCB can also be used as a data strobe. By holding both inputs at logic 1, all data outputs will remain at logic 1 until FCA and/or FCB are changed to logic 0.
GUDTA	13	Good Data. Output. After 35 milliseconds of valid DTMF detection, the DATA outputs change to the programmed output. GUDTA occurs within 10 microseconds after DATA change and persists 25 milliseconds after the end of DTMF detection. See Figure 6. For DTA to be read during DTMF signal presence, strobe the leading edge of GUDTA (button down). For DATA to be read after DTMF signal presence, strobe trailing edge of GUDTA (button up).
SEN ADJ	6 and 7	DTMF Sensitivity Adjustment controls. For applications where extended DTMF detection sensitivity is required, connect a resistive shunt across pins 6 and 7. A 50 k ohm shunt will increase the sensitivity by approximately 3.5 dB; a short will increase the sensitivity by approximately 7 dB. Since M-907 input signal level sensitivity varies slightly with supply voltage changes, critical operation over the specified voltage range may require a gain adjustment. Factory adjustment is made with a supply voltage of 12 ±0.1 V. A higher supply voltage will decrease the sensitivity. For example, at 15 V, sensitivity will be decreased by 2 dB. This decrease in gain can be offset by connecting a selected resistor across the SEN ADJ pins (6 and 7). To maintain the desired sensitivity thresholds, the supply voltage should be held within 1% of the selected value.
DATA 0 through DATA 11	14 through 25	Data outputs. Output. The data output states of all 16 digits for any possible condition of FCA and FCB are shown in Figure 2. Logic state 1 and logic state 0 are defined in Table 3, Performance Characteristics.

Installation Data

Refer to Figure 7 for maximum dimensions. Figure 8 displays the required PC component side layout and the relation to the assembly.

M-907s are shipped in electrically conductive bags to protect MOSFET components on the assemblies from static electricity. During and after removal from the bags, handle the assemblies by the edges and avoid touching circuit traces or components. This will minimize any possibility of damage to components from static electricity built up on the body of the installer. When returning an M-907, it should be placed in one of these protective bags.
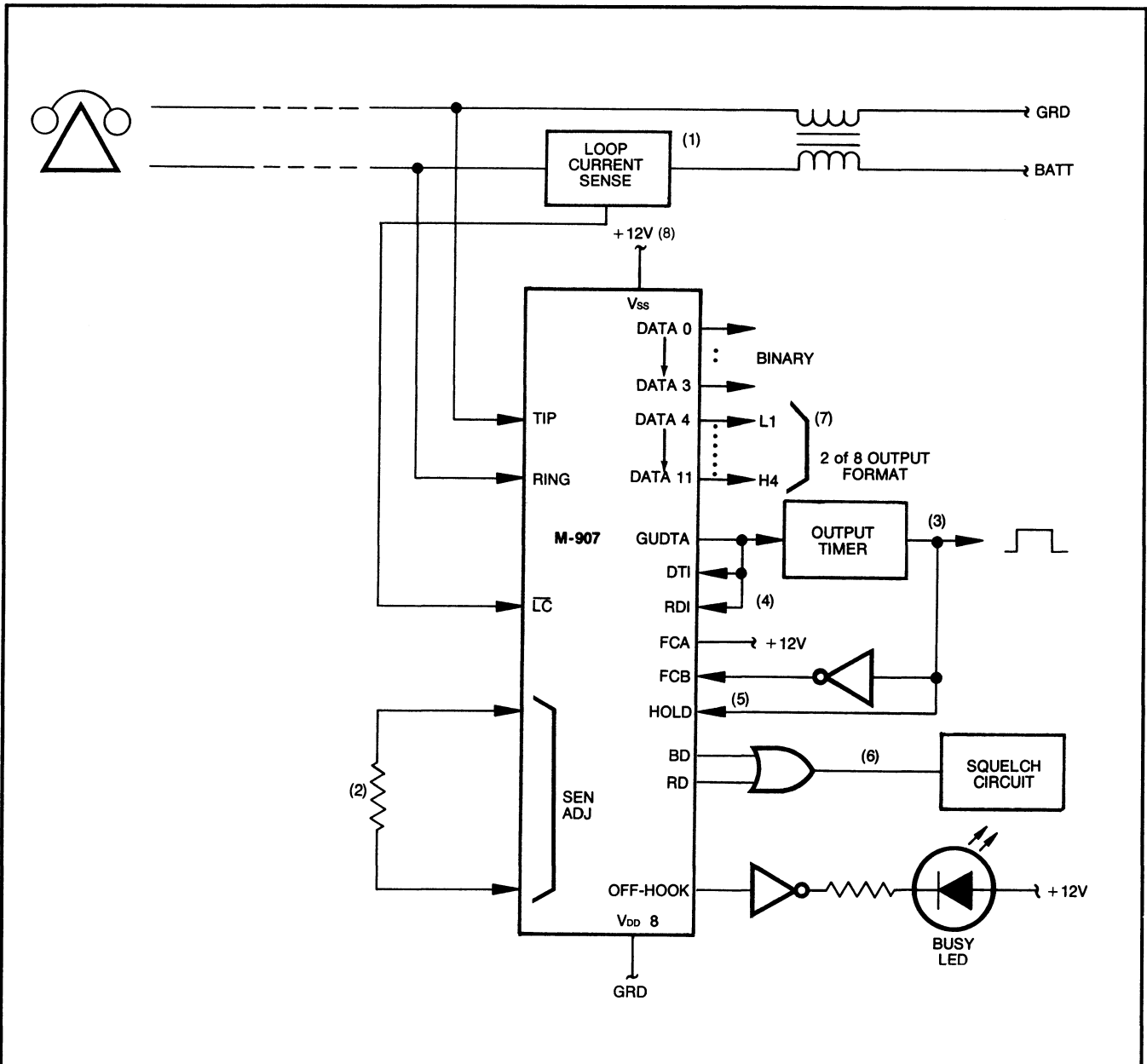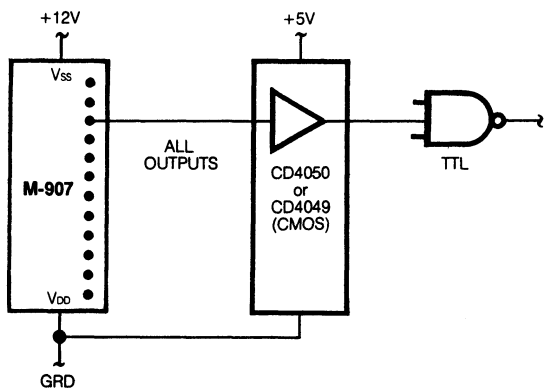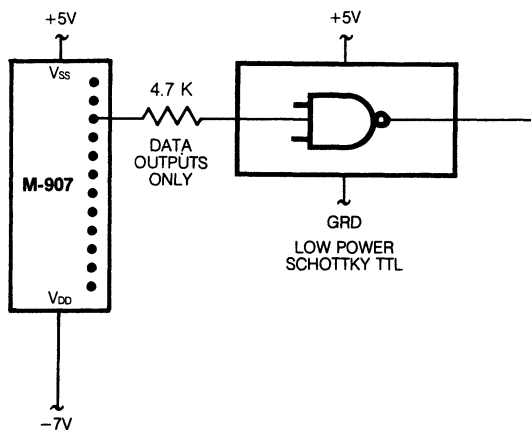
Notes:

1. If rotary dial counting is not required, omit loop current sense circuit and connect $\overline{\text{LC}}$ to GRD.

2. Refer to SEN ADJ in Table 2.

3. The output timer controls the duration of the data outputs. For button-down operation, trigger the timer with the rising edge of GUDTA. For button-up operation, trigger the timer with the trailing edge of GUDTA.

4. DTI and RDI are connected to GUDTA, providing cross-inhibit operation.

5. A connection to HOLD is required only when the output duration must be greater than 50 ms and the receiver is configured to operate at the maximum rate of 12 PPS.

6. For applications such as dictation control links the squelch circuit can be used to prevent DTMF tones from being recorded during the dictate mode or transmitted to a secondary receiver.

7. The 2 of 8 output is used in this example. Other output formats can be obtained by changing the signals applied to FCA and FCB as shown in Figure 2.

Figure 3 Typical Applications

1. TO TTL
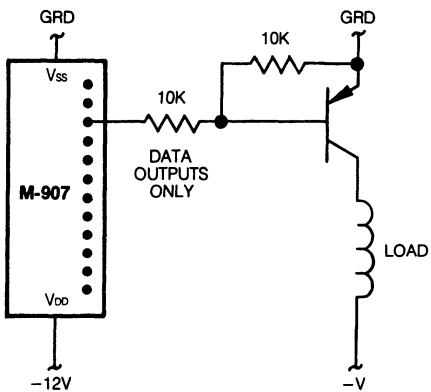
+12V   +5V

V_{SS} CD4050
                                        or
M-907   ALL   CD4049
             OUTPUTS   (CMOS)

V_{DD} TTL

GRD

2. TO LOW POWER SCHOTTKY TTL

+5V   +5V

V_{SS}
             4.7 K
M-907   DATA
             OUTPUTS
             ONLY

V_{DD} GRD

                                        LOW POWER
-7V   SCHOTTKY TTL

3. TO RELAYS OR DISPLAYS (NEGATIVE SUPPLY)

GRD   GRD
                        10K
V_{SS}
             10K
M-907   DATA
             OUTPUTS
             ONLY   LOAD

V_{DD}

-12V   -V

4. TO TRANSISTOR DRIVERS

+12V   +V

V_{SS}
                                        LOAD
M-907   ALL
             OUTPUTS

             100K
V_{DD}
                                        47K

GRD
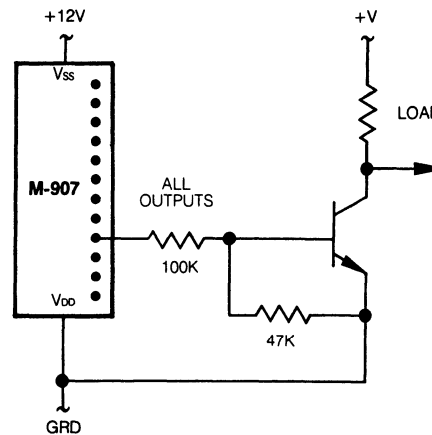
5. (NOT SHOWN) TO CMOS AT THE SAME SUPPLY VOLTAGE — INTERFACE DIRECTLY (ALL OUTPUTS)
6. (NOT SHOWN) TO CMOS AT A LOWER SUPPLY VOLTAGE — USE CD4050 OR CD4049

Figure 4 Suggested Output Interface Techniques
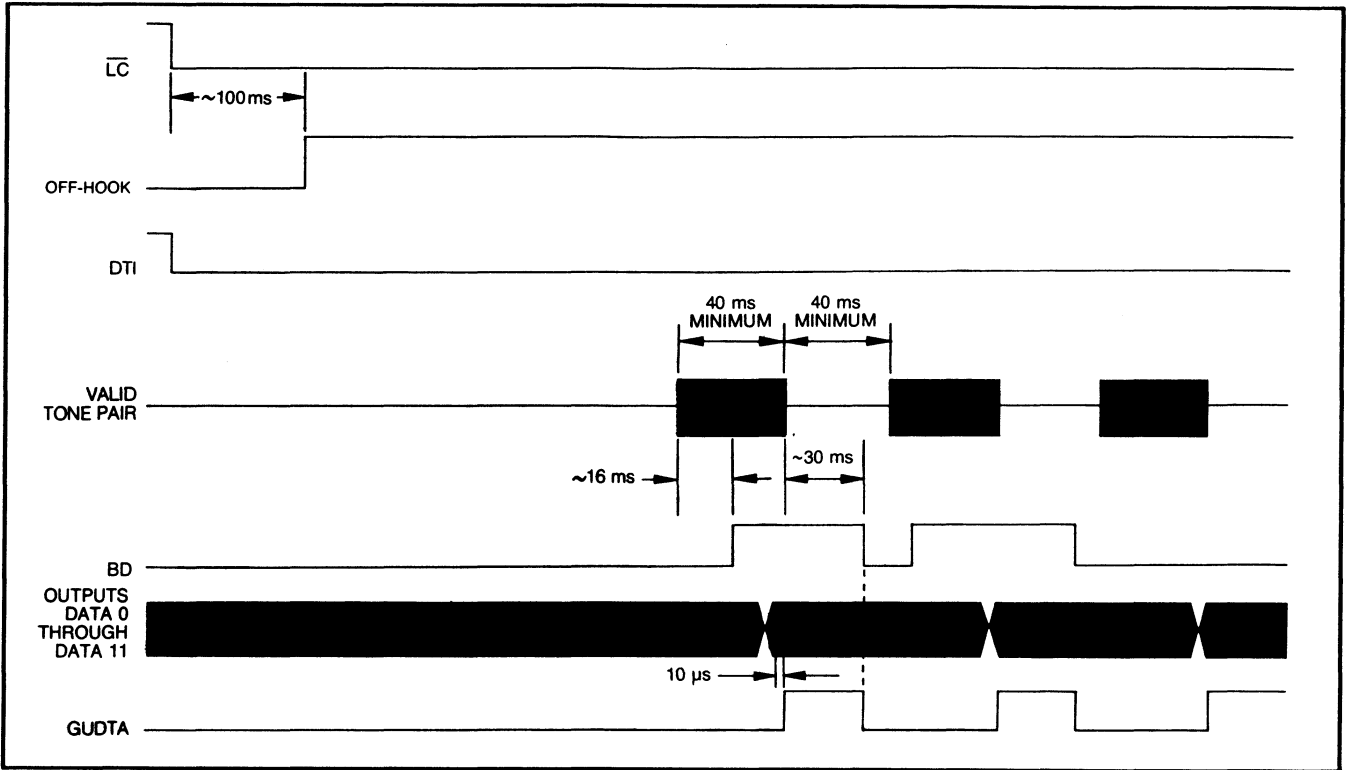
Figure 5 DTMF Digit Timing Chart
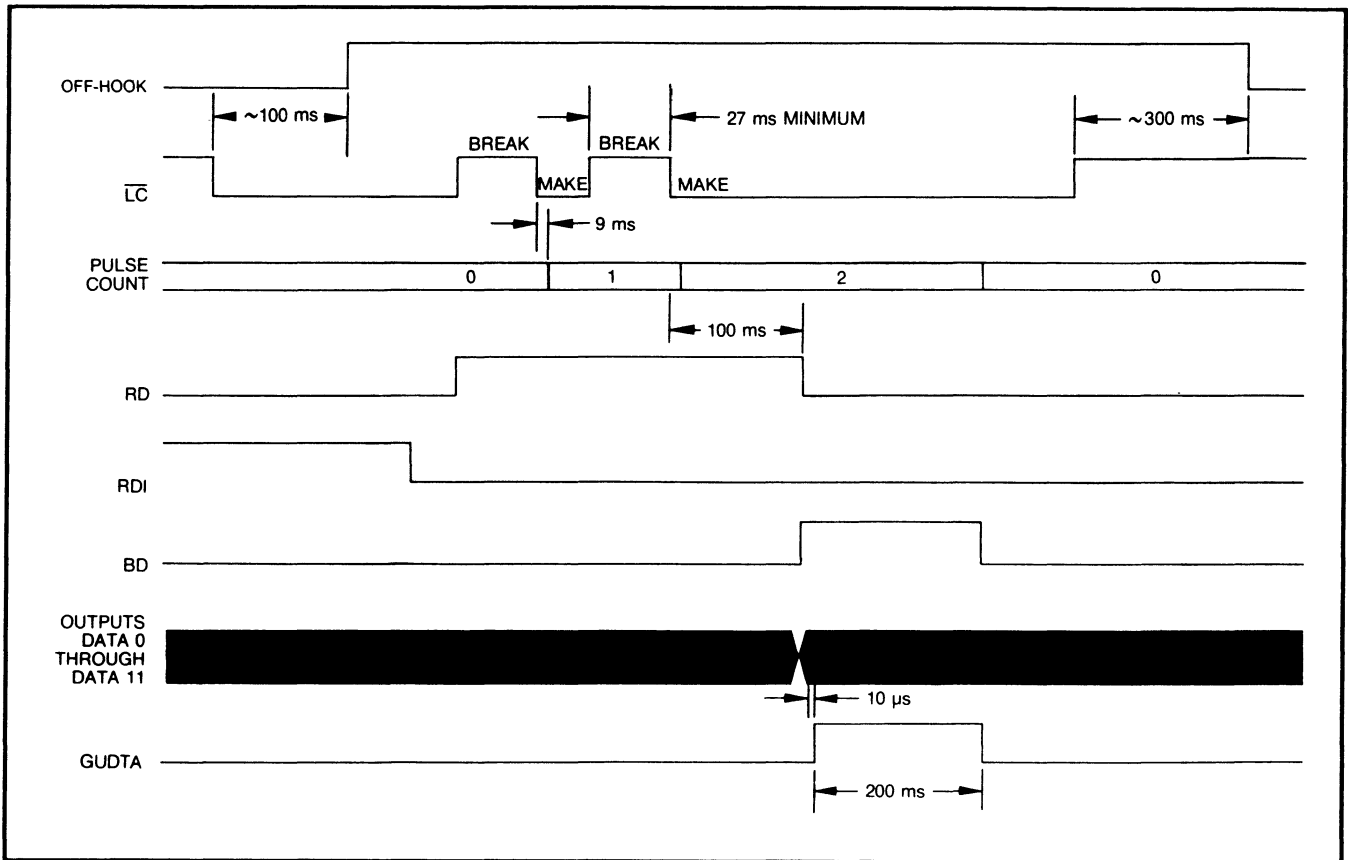
Figure 6 Rotary Dial Timing Chart

0.16
(4.06)

0.10
(2.54)

0.755
(19.18) TYPICAL

0.759
(19.28) MAXIMUM

0.630
(16.00)

0.00= INCHES
(00.0)= MILLIMETERS

0.06
(1.52)

PIN IS 0.025 SQUARE
(0.64)
29 PLACES

0.00 = INCHES
(00.0) = MILLIMETERS

4.10
(104.1)

1.17
(29.69)
MAXIMUM

1.14
(29.03)
TYPICAL

0.630
(16.00)

3.02 MAX
(76.7)

4.52 MAX
(114.9)

COMPONENT
SIDE

0.495
(12.57)

CONNECTOR DATA

Acceptable connectors are:
  Methode Electronics, Inc.,
    1000-007-2102 (2 required) and
    1000-022-2102 (1 required). The
    1600, 1700, and 1800 series are
    also acceptable.
  Molex Incorporated,
    22-18-2073 (2 required) and
    22-18-2223 (1 required) or
    similar connectors.

0.47
(11.94)

M-907-03
ONLY

NOTE:
The M-907-03 is identical to the M-907-01
except that the pins extend from the
opposite (solder) side of the board.

Figure 7 Clearance Dimensions

Table 3 Performance Characteristics

Parameter	Specification	Notes
Input Specifications		
DTMF Input Signal Requirements		
Input impedance	150 kilohms bridging	
Signal accept level (per frequency)	0.055 to 1.55 Vrms (-23 to +6 dBm)	
Signal accept level (extended range)	(-30 to +3 dBm)	Extended signal level is accomplished by shunting the SEN ADJ leads.
Signal reject level	0.017 Vrms (-33 dBm)	
Signal reject level (extended range)	0.008 Vrms (-40 dBm)	(see note above)
Signal accept duration	≥40 ms	
Signal reject duration	≤25 ms	
Interdigital pause accept duration	≥40 ms	
Interdigital pause reject duration	≤25 ms	
Signal cycle time	≥80 ms	
Tone accept bandwidth	±(1.5% + 2 Hz)	
Tone reject bandwidth	±3.5%	
Twist	+6, -8 dB	High frequency with respect to low frequency
Precise dial tone level (per tone)	≤0.195 Vrms (-12 dBm)	
Noise ratio (flat weighted)	≥20 dB	With respect to lower level of the two DTMF tones
DC Input Timing Requirements (DC input is via the $\overline{LC}$ lead))		
Off-hook recognition	100 ±5 ms	DTMF detection can start after off-hook recognition time. Rotary dial pulse detection is inhibited until off-hook blanking has passed.
Off-hook blanking	300 ±10 ms	
Dial pulse break recognition	27 ±2.5 ms	
Dial pulse make recognition	9 ±2.0 ms	
End-of-digit recognition	100 ±5 ms	
Interdigital blanking	200 ±8 ms	
On-hook recognition	300 ± 10 ms	
Logic Input Voltage Level Requirements		
All inputs: HOLD, DTI, RDI, CLEAR, $\overline{LC}$, FCA, FCB	See Figure 9	Terminate all unused logic inputs to Vss or VDD
Output Specifications		
Interface Capability	CMOS, low-power Schottky TTL, or Transistor Driver	
Voltage levels		
All outputs (including data outputs when sink or source current is ≤100 μA)	See Figure 10A	
Data outputs only (when sink current is 1.0 mA)	See Figure 10B	
Power Requirements		
Voltage (Vss positive with respect to VDD)	11 to 15 VDC	
Current	50 mA typical	
Environmental Requirements		
Temperature limits	0 to 65 °C	
Relative humidity limit	85% maximum	
Maximum Physical Dimensions		
Height	See Figure 7.	
Width	4.52 inches (114.9 mm)	
Depth	3.02 inches (76.7 mm)	
Weight	2.40 ounces (61 grams)	

10.	Vᴅᴅ (−V)		Vss (+V)	11.
9.	+ TIP		+ BD	12.
8.	RING		GUDTA	13.
7.	+ SEN ADJ		+ DATA 0	14.
6.	SEN ADJ		DATA 1	15.
	+		DATA 2	16.
	+		DATA 3	17.
	+		DATA 4	18.
	+		DATA 5	19.
	+		DATA 6	20.
	+		DATA 7	21.
	+		DATA 8	22.
	+		DATA 9	23.
	+		DATA 10	24.
	+		DATA 11	25.
	+		+	
	+		FCA	26.
5.*	OFF-HOOK		FCB	27.
4.	+ RD		HOLD	28.
3.	CLEAR		LC	29.
2.	DTI		+	
1.	RDI		+	

*Be Sure the connector used for pin 5 does not extend beyond pin 5.
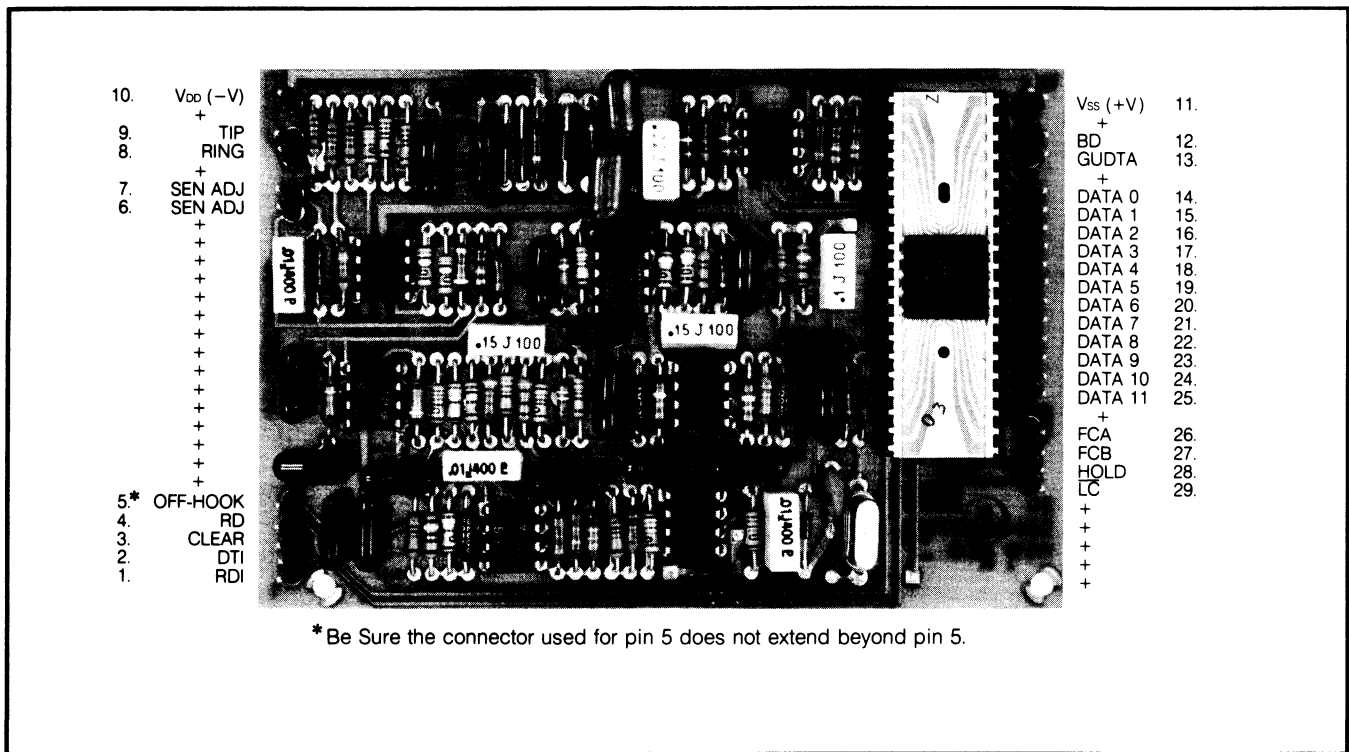
Figure 8 PC Layout
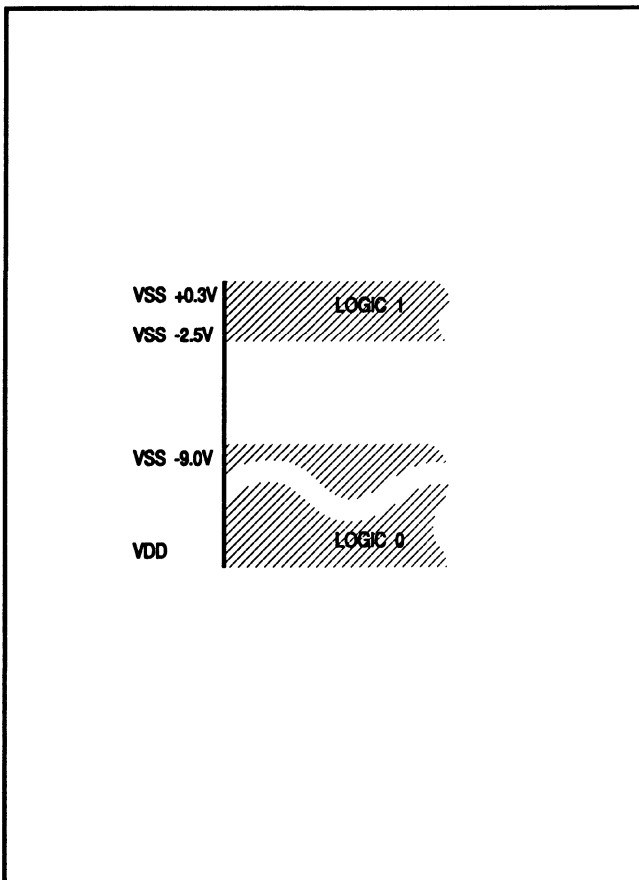
Figure 9 Logic Input Levels

ALL OUTPUTS
(WHEN SINK AND SOURCE
CURRENTS ARE ≤100 µA)

DATA OUTPUTS ONLY
(WHEN SINK CURRENT
IS 1.0 mA)

Figure 10 Output Levels

Teltone Corporation / 10801-120th Avenue NE, Kirkland, WA 98033   Phone: 1-800-426-3926 or 206-827-9626   Fax: 206-827-6050   TWX: 910-449-2862
Teltone Limited / 3375-14th Avenue, Markham, Ontario, Canada L3R 2L6   Phone: 416-475-0837   Fax: 416-474-9151   Envoy User Name: TTL.HQ

7-22
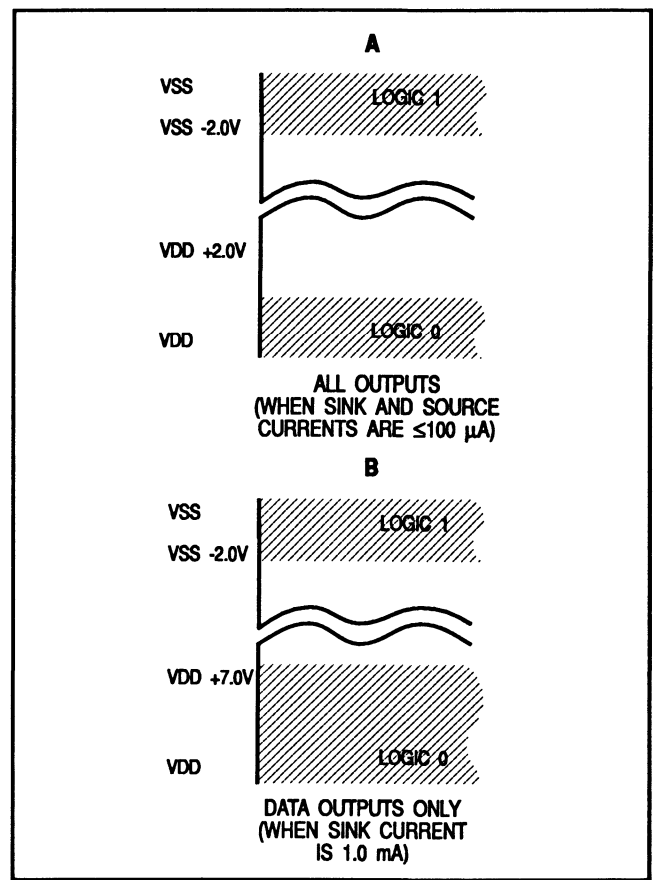
M-917 DTMF DECODER AND DIAL PULSE COUNTER

The Teltone® M-917 Receiver Module is designed for applications where a high-performance **central office grade** Touch-Tone® DTMF (Dual-Tone Multifrequency) detector and/or a rotary dial pulse counter is required. The receiver's compact size and low heat emission make it well suited for high-density packaging.

The receiver, as functionally displayed in Figure 2, consists of a bridging buffer amplifier, dial tone filter, bandsplit filter, and a crystal-controlled digital frequency detector capable of detecting all 16 DTMF digits. A dial pulse counter detects rotary dial digits. The unit can be programmed to accept DTMF signals only, rotary dial pulses only, or to provide mixed DTMF and rotary dial operation.

Data outputs interface with a variety of external devices. These outputs are available in partial 2 of 8 (for use in inhibiting * and # outputs), partial 1 of 12 (for use in inhibiting A, B, C, and D outputs), binary, or blank formats. Figure 3 displays related DTMF digit codes.
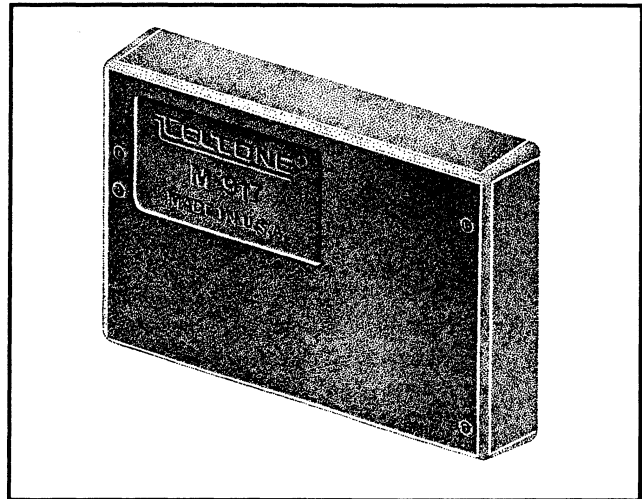
Figure 1 M-917 Receiver

Figure 2 Block Diagram

HIGH GROUP OF FREQUENCIES

	H1 1209	H2 1336	H3 1477	H4 1633
L1 697	1	ABC 2	DEF 3	A
L2 770	GHI 4	JKL 5	MNO 6	B
L3 852	PRS 7	TUV 8	WXY 9	C
L4 941	*	0	#	D

LOW GROUP OF FREQUENCIES

Note: A valid digit always contains one low tone and one high tone. This combination is often called 2 of 7 or 2 of 8. 1633 Hz is not present on 2 of 7 installations.
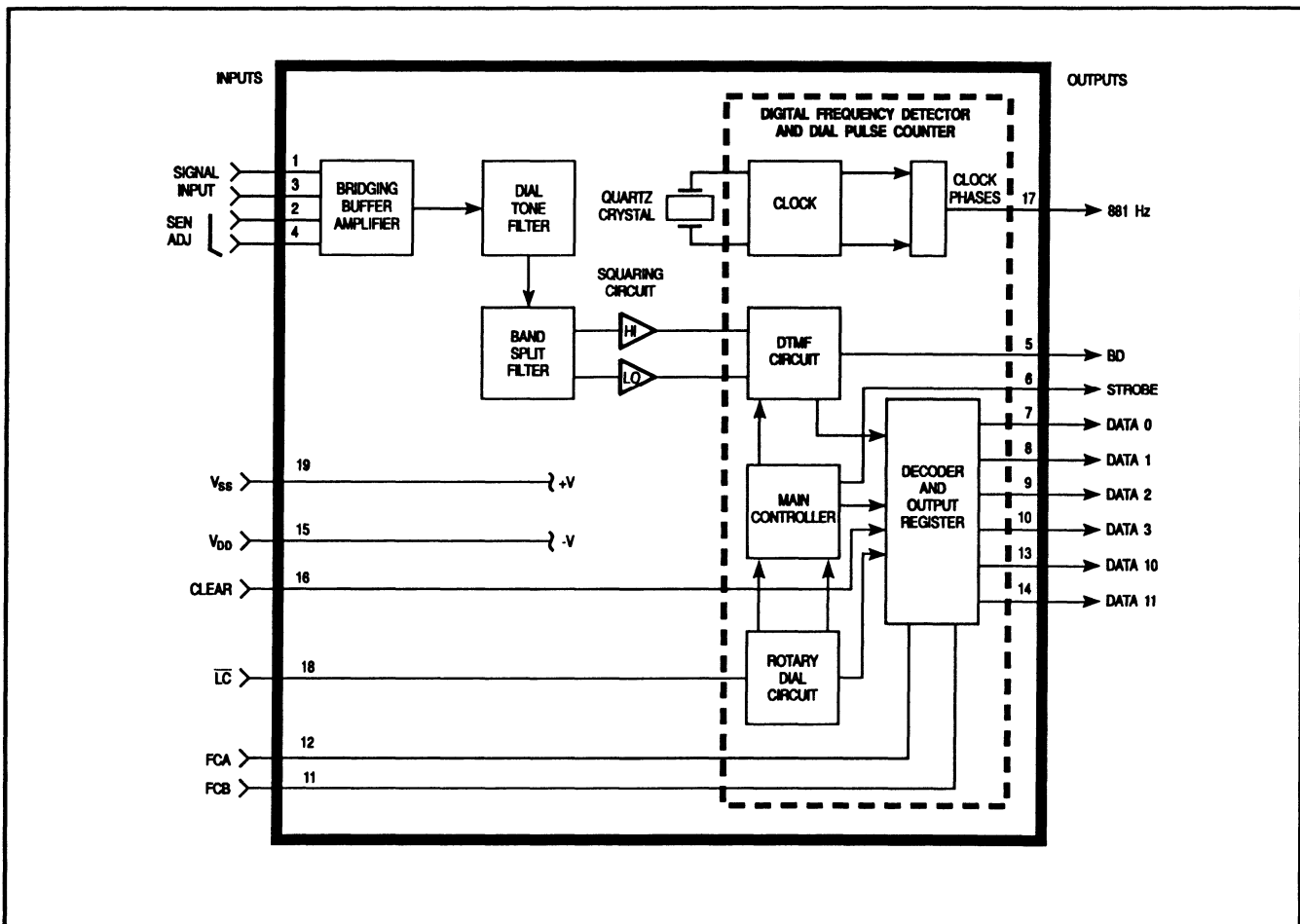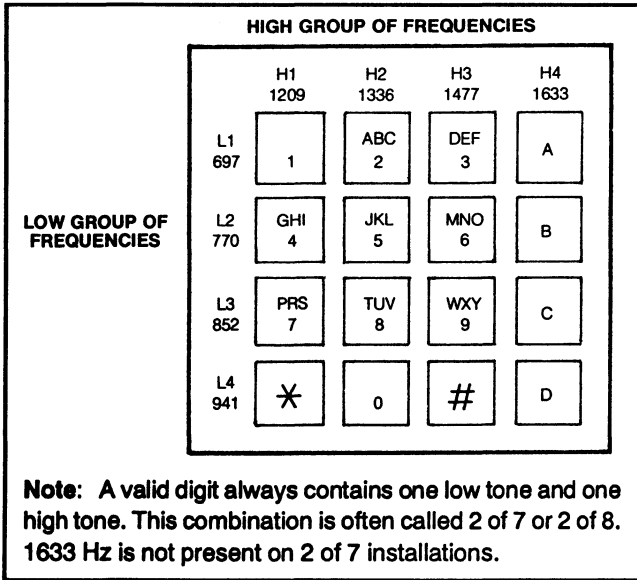
Figure 3 DTMF Signal Format

Notes:

(1) If rotary dial counting is not required, omit Loop Current Sense circuit and connect LC to GRD (Pin 18 to Pin 15). Disconnect DTMF inputs if rotary dial counting only is desired.

(2) Refer to SEN ADJ in the Pinout description table.

(3) To inhibit A, B, C, D outputs:

(4) To inhibit "*" and "#" digits:

Figure 4 Applications

The M-917 provides maximum flexibility in a variety of customized applications. Input/output features are illustrated in Figure 4. Refer to Figure 5 for output interfacing techniques.

Features

- A complete LSI digital Touch-Tone detector and rotary dial counter contained in a module requiring less than 3.25 x 2.25 x 0.635 inches.
- Meets or exceeds telephone central office requirements for DTMF recognition and voice talkoff protection.
- Fully time-guarded rotary dial pulse counting.

Table 1 Output Formats

DIGIT	1	2	3	4	5	6	7	8	9	0	*	#	A	B	C	D
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
3	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
10	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	
11	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	

(Column at left labeled **DATA**)

Partial 1 of 12 Output Format
(FCA=0, FCB=0)

DIGIT	1	2	3	4	5	6	7	8	9	0	*	#	A	B	C	D
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
2	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
3	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
10	1	1	0	1	1	0	1	1	0	1	1	0	1	1	1	
11	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	

(Column at left labeled **DATA**)

Binary and Partial 2 of 8 Output Format
(FCA=1, FCB=0)

DIGIT	1	2	3	4	5	6	7	8	9	0	*	#	A	B	C	D
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
2	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
3	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
10	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Column at left labeled **DATA**)

Binary Output Format
(FCA=0, FCB=1)

DIGIT	1	2	3	4	5	6	7	8	9	0	*	#	A	B	C	D
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Column at left labeled **DATA**)

Blank Output Format
(FCA=1, FCB=1)

☐ BINARY DATA

- Decodes all 16 DTMF digits and counts rotary dial digits.
- Crystal-controlled LSI digital circuitry assures maximum frequency detection accuracy and stability.
- Provision for adjusting tone detection sensitivity.
- Precision clock output at 881 Hz.
- Selectable output format.
- Selectable button-up or button-down operation.
- Separate output indicates early tone presence.
- Single voltage operation (12 VDC).
- Low power consumption: typically 420 mW (35 mA at 12 VDC).

Applications

- PBX and central office receivers
- Data transmission
- Tone and/or rotary dial controlled dictation links.
- Radio telephone systems.
- Other applications using a telephone dialing mechanism or an analogous device to convey information.

Installation Data

Mounting pin assignments and dimensions for the M-917 are shown in Figure 6.

The M-917 module is packed in an electrically conductive bag to protect MOSFET components from static electricity damage. The module should not be removed from this bag until ready for use. During or after removal, avoid touching M-917 connector pins. Observe static electricity precautions whenever handling the module.

Table 2 Absolute Maximum Ratings	
Supply voltage (V_{SS} referenced to V_{DD})	15 V
Lightning protection, analog inputs, differential and common modes (CCITT Rec. K.17.2)	1500 VDC
Analog inputs (constant voltage, differential and common modes)	300 VDC
Digital inputs (V_{DD} = 0 V)	-0.3 V to (V_{SS} +0.3V)
Operating temperature range (T_A)	0 to 55 °C
Storage temperature range (T_S)	-40 to 85 °C
Lead soldering temperature (0.035-inch from package for 10 seconds)	256 °C
Relative humidity limits	0 to 85%
Meets environmental requirements of CEPT T/CS 213.	

1. TO TTL OR CMOS AT A LOWER SUPPLY VOLTAGE

2. TO LOW POWER SCHOTTKY TTL

3. TO RELAYS OR DISPLAYS (NEGATIVE SUPPLY)

4. TO TRANSISTOR DRIVERS

5. (NOT SHOWN) TO CMOS AT THE SAME SUPPLY VOLTAGE—INTERFACE DIRECTLY (ALL OUTPUTS)
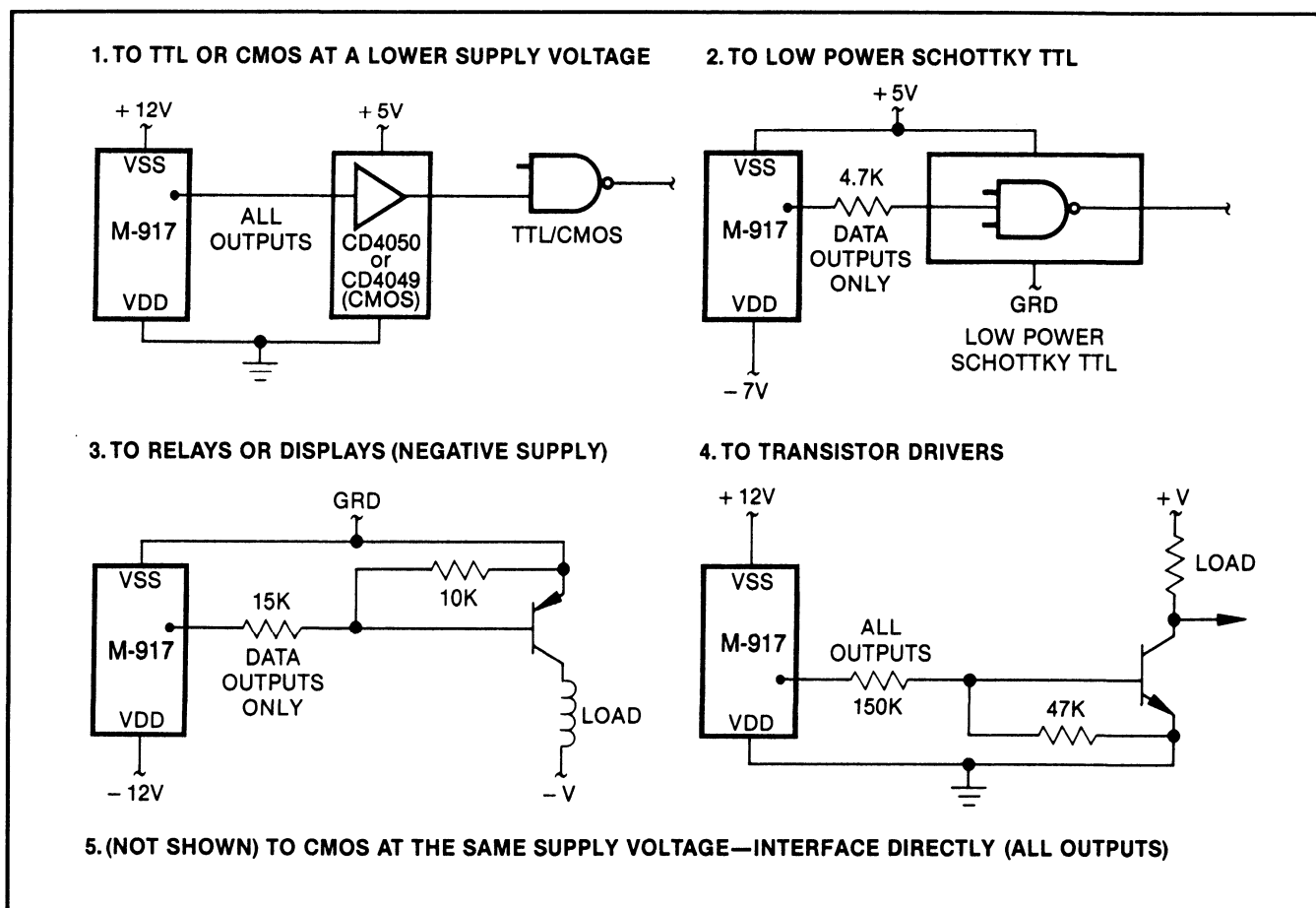
Figure 5 Suggested Output Interface Techniques

Table 3 DC Electrical Characteristics
(VSS=12V, VDD=OV, TA=0−55°C)

Characteristic	Symbol[1]	Test Conditions	Min.	Typ.	Max.	Units
Supply voltage	VSS[2]		11	12	15	V
Supply current	ISS		30	35	45	mA
Input voltage[3] low level	VIL		VDD−0.3		VDD+2	V
Input voltage[3] high level	VIH		VSS−2		VSS+0.3	V
Output voltage[3] low level	VOL	IOL = 100 uA, all outputs			VDD+2	V
		IOL = 1 mA, DATA outputs only			VDD + 7	
Output voltage[3] high level	VOH	IOH = 100 uA, all outputs	VSS−2			V
Output current, low level	IOL	All outputs, (except DATA outputs)	0.1			mA
		DATA outputs only	1			mA
Output current, high level	IOH	All outputs	−0.1			mA
Off-hook recognition	t$_{OH}$	$\overline{LC}$ at 0V	95	100	105	ms
Off-hook blanking	t$_{OHB}$	$\overline{LC}$ at 0V	285	300	315	ms
Break recognition	t$_{BK}$	$\overline{LC}$ at 12V	24.5	27	29.5	ms
Make recognition	t$_{MK}$	$\overline{LC}$ at 0V	7	9	11	ms
End of digit recognition	t$_{EOD}$	$\overline{LC}$ at 0V	95	100	105	ms
Interdigital blanking (rotary dial only)	t$_{IDB}$	$\overline{LC}$ at 0V	192	200	208	ms
On-hook recognition	t$_{ONH}$	$\overline{LC}$ at 12V	290	300	310	ms

Notes follow Table 4.

Table 4 AC Electrical Characteristics
(VSS=12V, VDD=OV, TA=0−55°C)

Characteristic	Symbol[1]	Test Conditions	Min.	Max.	Units
Input impedance		f = 1 kHz	150		kohm
Common mode noise voltage		f = 15 to 100 Hz / f = 100 to 20 kHz		25 / 0.5	Vrms / Vrms
Dial tone rejection		f = 500 Hz	−24		dB
Signal level, accept[2]		SEN ADJ open / SEN ADJ shorted	−23 (.0548) / −30 (.0245)	+6 (1.546) / +3 (1.095)	dBm²(V) / dBm(V)
Signal level, reject		SEN ADJ open / SEN ADJ shorted		−33 (.0174) / −40 (.0078)	dBm(V) / dBm(V)
Signal bandwidth, accept			−1.5%−2	+1.5%+2	Hz
Signal bandwidth, reject			−3.5%	+3.5%	Hz
Twist acceptance		VFH > VFL	−8	+6	dB
Signal to noise ratio		band limited white noise (300-3400 Hz)		20	dB
Signal reject time	t$_{SR}$		20		ms
Signal recognition time	t$_{SR}$			40	ms
Signal pause reject time	t$_{SP}$		20		ms
Signal pause accept time	t$_{SP}$			40	ms
Signal cycle time	t$_{SC}$		80		ms
Early signal presence	t$_{ES}$	BD		16	ms
Strobe output delay	t$_{STD}$	Data outputs Stable to strobe	10		us
Button-up guard	t$_{BU}$		25	40	ms

Notes: (Tables 3 and 4)

1. Symbol definition portrayed in Figure 7.

2. M-917 sensitivity may change with a shift in VSS. Specifications given pertain to VSS of 12V±0.1V. Refer to SEN ADJ in Pinout Table for effects of greater VSS variations.

3. See Figure 8.

4. Voltage levels stated in dBm are obtained using a standard voltmeter calibrated to provide a scaled voltage measurement in dBm for a 600 ohm impedance. No termination should be applied for this measurement.

Table 5 Pin Functions

Mnemonic	Pin Number	Description
BD	5	Button Down Output—during DTMF operation, provides an early tone presence that starts 16 ms after a valid tone pair is detected and ends approximately 25 ms after the tone pair ends. During rotary dial operation, BD follows the STROBE output.
CLEAR	16	Clear Input—a logic 1 applied to the CLEAR input will reset the Receiver's DTMF and rotary dial detection circuits. All DATA outputs will be forced to the digit D state. The Receiver is enabled again when the CLEAR input returns to a logic 0.
DATA 0, 1, 2, 3, 10, 11	7, 8, 9, 10, 13, 14	Data Outputs—Refer to the Data Output Table for data output states. Refer to the DC Electrical Characteristics Table for logic 1 and logic 0 levels.
FCA	12	Format Control A input (See Note)
FCB	11	Format Control B input (See Note)
$\overline{LC}$	18	Loop Current Not—the rotary dial pulse input. A logic 0 (−V) represents either an off-hook condition or a make period. A logic 1 (+V) represents either an on-hook condition or a break period. For DTMF operation only, $\overline{LC}$ can be connected to −V; the receiver will then be enabled as long as the CLEAR input is at logic 0.
SEN ADJ	4, 2	Sensitivity Adjust—For applications where extended DTMF detection sensitivity is required, a resistive shunt can be connected across these pins. A 50K ohm shunt increases sensitivity by approximately 3.5dB; a short increases sensitivity by approximately 7 dB. Sensitivity changes due to variations within the specified supply voltage (VSS) range may be compensated by connecting a selected resistor across the SEN ADJ terminals. A higher VSS decreases sensitivity by 2dB at VSS = 15VDC.
SIGNAL INPUT	3, 1	DTMF Inputs (Tip and Ring), as defined under specifications.
STROBE	6	STROBE Output. After approximately 35 ms of valid DTMF detection, the DATA outputs change to the corresponding output. STROBE occurs within 10 us after DATA change and will persist approximately 25 ms after the end of DTMF detection. For DATA to be read during DTMF signal presence, read the leading edge of STROBE. For DATA to be read after DTMF signal presence, read the trailing edge of STROBE.
VDD	15	−V Input
VSS	19	+V Input (11 to 15 VDC with respect to VDD).
881 Hz	17	This square wave output, controlled by the M-917 internal crystal, may be used to derive other applicable timings.

Note:
Format Control input levels dictate the Data Output Format as follows:

FCA	FCB	Output Format
0	0	Partial 1 of 12
0	1	Binary
1	0	Binary and Partial 2 of 8
1	1	Blank
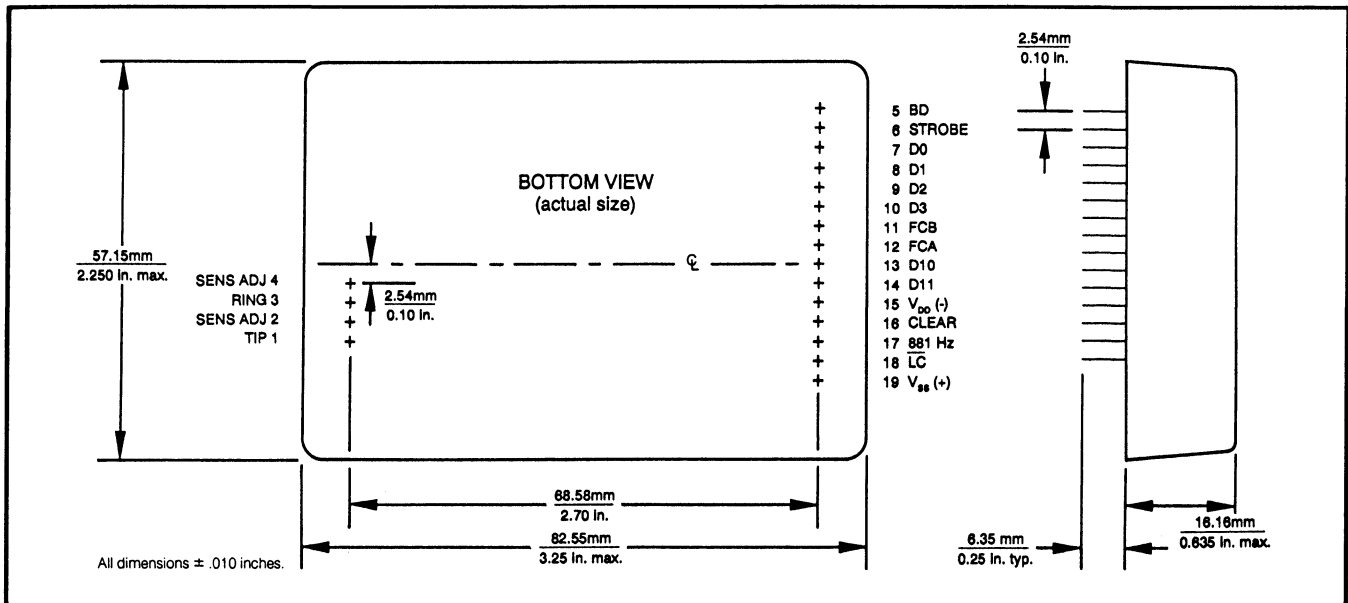
Figure 6 Dimensions and Pin Assignments

Pin Assignments:
5 BD
6 STROBE
7 D0
8 D1
9 D2
10 D3
11 FCB
12 FCA
13 D10
14 D11
15 V_{DD} (-)
16 CLEAR
17 881 Hz
18 LC
19 V_{ss} (+)

SENS ADJ 4
RING 3
SENS ADJ 2
TIP 1

57.15mm / 2.250 In. max.

68.58mm / 2.70 In.

82.55mm / 3.25 In. max.

2.54mm / 0.10 In.

6.35 mm / 0.25 In. typ.

16.16mm / 0.635 In. max.

All dimensions ± .010 inches.
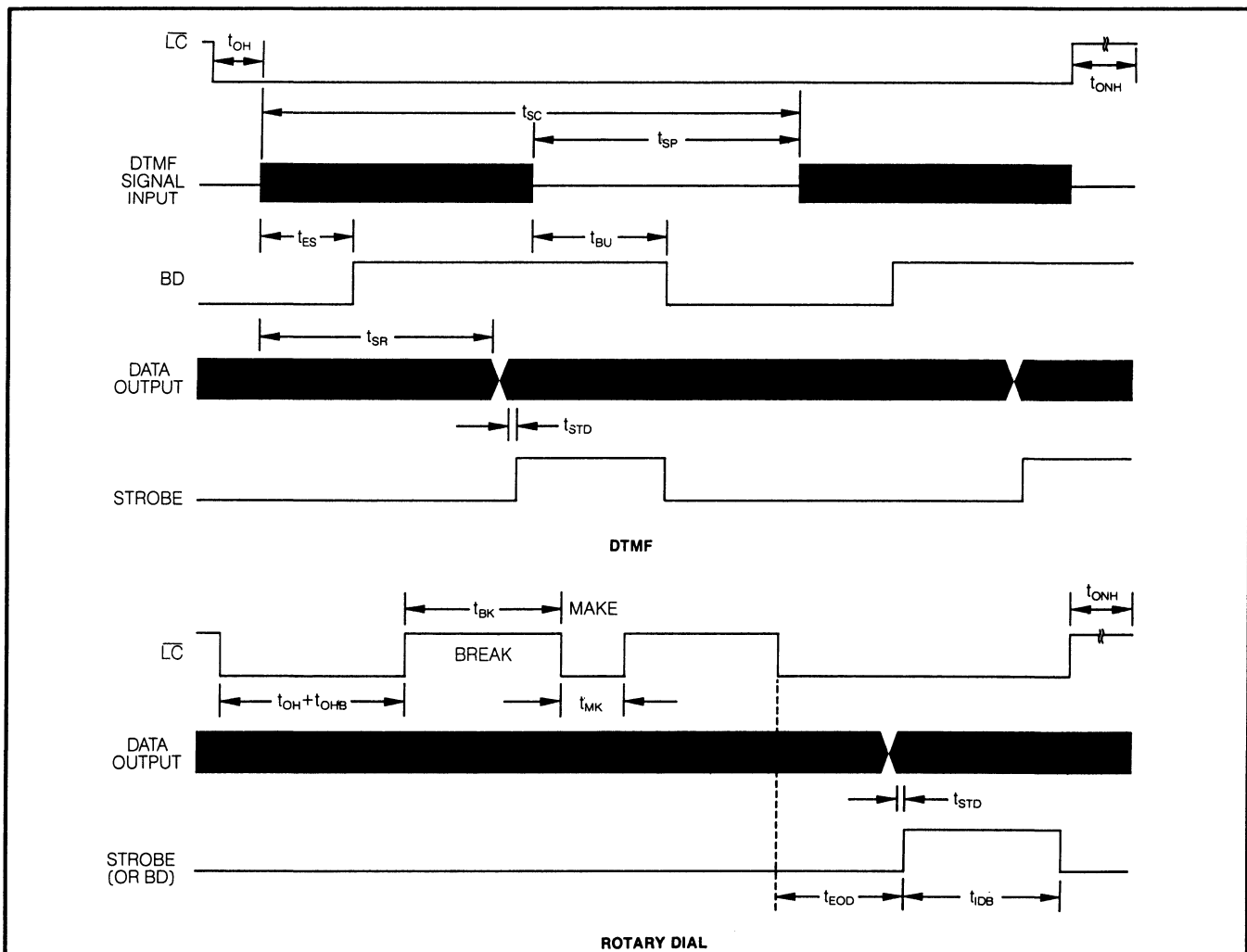
DTMF

ROTARY DIAL

Figure 7 Timing Diagram
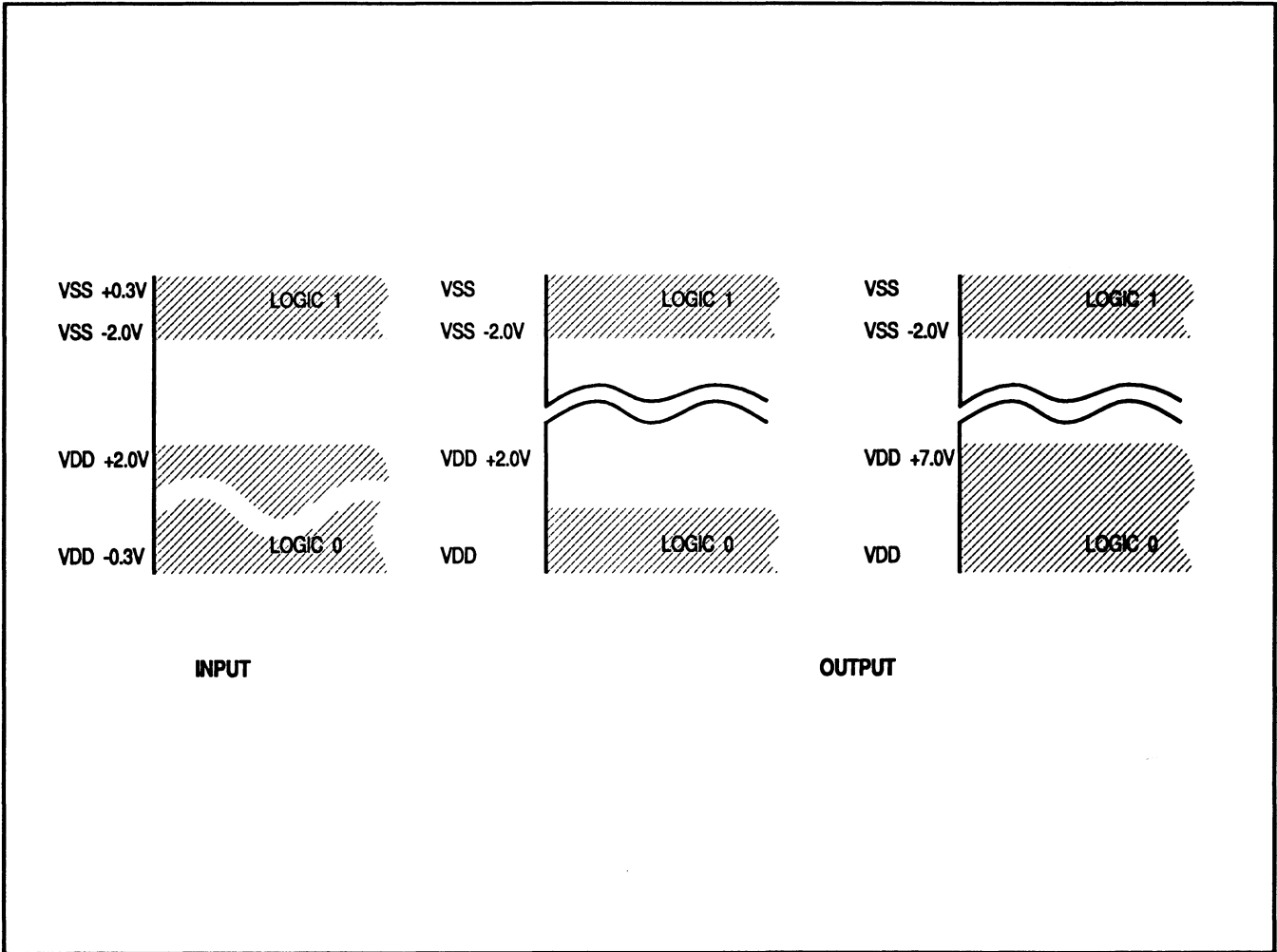
Figure 8 Logic Levels

M-927 DTMF RECEIVER

The Teltone® M-927 is a high-quality Dual-Tone Multi-frequency (DTMF) digital receiver and/or rotary dial pulse counter. The M-927 is contained in a 40-pin package and requires no external components except a single 3.579 MHz television color burst crystal.

As shown in Figure 2, the M-927 is typically connected in parallel with the voice pair (Tip and Ring) of a telephone line. It receives signals from a DTMF generator or pulsing mechanism and translates them into logic level outputs for use by other devices, permitting applications such as data entry via telephone or instrument and control system access and activation. For applications such as DTMF-to-rotary conversion, additional outputs provide early indications of signal presence. Logic inputs to the M-927 enable or disable the receiver, inhibit or enable the reception of DTMF or rotary signals, and select from the output formats listed in Table 1.

The M-927 is manufactured under U.S. Patent 4,145,576.

Features

- Meets CEPT overall performance requirement of less than one false operation per 10,000 digits dialed
- Meets CCITT recommendations for tone receivers
- Decodes all 16 DTMF digits
- Time-guarded rotary dial pulse counting
- Selectable output formats: binary, 2 of 8 (2 of 7), 1 of 12, or blank
- Accepts differential or single-ended input with no additional components
- Provides superior signal-to-noise characteristics and speech immunity
- Three different chip enable/disable inputs
- Separate outputs indicating dial pulse or early DTMF tone presence
- Valid data output strobe
- Stable, free-running clock outputs: 447 kHz, 881 Hz, and 20 Hz

Telephone Switching Applications

- Central office products
- PBX and intercom systems
- Consumer-oriented special feature phones and services
- Radio equipment interface to telephone network

Access and Control Applications

- Answering and recording devices
- Radio communication remote switching

- Remote control of machinery or microprocessors
- Monitoring equipment

Data Entry Applications

- Remote computer and peripheral systems interface
- Consumer credit and shopping systems
- Telephone banking, credit, and bill-paying systems

Figure 1 Block Diagram

Figure 2 Typical Application

Notes:
1. If rotary dial counting is not required, omit Loop Current Detector and connect LC to − V.
2. Other output formats can be obtained by changing the signals applied to FCA and FCB as shown in Table 1.

Table 1 Output Formats

1 OF 12 OUTPUT FORMAT — FCA 0, FCB 0

DIGIT	1	2	3	4	5	6	7	8	9	0	*	#	A	B	C	D
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
3	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
4	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
5	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
6	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
7	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
8	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
9	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
10	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
11	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1

BINARY AND 2 OF 8 OR 2 OF 7 OUTPUT FORMATS — FCA 1, FCB 0

BINARY OUTPUT FORMAT — FCA 0, FCB 1

BLANK OUTPUT FORMAT — FCA 1, FCB 1

Figure 3 Output Interface Techniques

1. TO TTL OR CMOS AT A LOWER SUPPLY VOLTAGE
2. TO LOW POWER SCHOTTKY TTL
3. TO RELAYS OR DISPLAYS (NEGATIVE SUPPLY)
4. TO TRANSISTOR DRIVERS
5. (NOT SHOWN) TO CMOS AT THE SAME SUPPLY VOLTAGE—INTERFACE DIRECTLY (ALL OUTPUTS)

Table 2 Pin Functions

Pin	Number	Description
– V + V	13 30	Negative and positive power supply connections (11 to 13.5 VDC).
POR POROUT	12 9	Power-On Reset. Receiver enable/disable input and output. A logic 1 applied to pin 12 drives pin 9 to logic 1, resets all detection circuits, drives the OFF-HOOK output to logic 0, and forces the DATA outputs to the "D" column of the currently enabled output format (see Table 1). A logic 0 applied to pin 12 enables the detection circuits, provided that $\overline{LC}$ has been at logic 0 for 100 ms, causing OFF-HOOK to go to logic 1.
CLEAR	8	Receiver enable/disable input. A logic 1 applied to the CLEAR input instantaneously resets all detection circuits and forces the DATA outputs to the "D" column of the currently enabled output format (see Table 1). A logic 0 applied to the CLEAR input immediately enables the detection circuits, provided that $\overline{LC}$ has remained at logic 0 or has not been at logic 1 for longer than 300 ms.
$\overline{LC}$	38	Loop Current Not input. $\overline{LC}$ is both a receiver enable/disable input and a rotary dial pulse input. A logic 0 represents an off-hook condition, an interdigital pause, or a make period. A logic 1 represents an on-hook condition or a break period. For DTMF operation only, $\overline{LC}$ can be connected to – V; then, with POR connected as shown in Figure 3, the receiver is enabled as long as CLEAR is at logic 0.
TIP RING	40 1	AC-coupled, balanced DTMF or single-ended input to the differential amplifier.
DAO	2	Differential Amplifier Output. Primarily used for testing.
FHO FLO	3 6	High Frequency group and Low Frequency group bandsplit filter outputs. Used only for testing.
$\overline{ES}$	31	Early Split Not input. When pulled to logic 0, $\overline{ES}$ enables the BD output.
	32	For factory use only. Connect to logic 0.
BD	29	Button Down output. When enabled by $\overline{ES}$ being at logic 0, BD goes to the logic 1 state 16 ms after a tone pair is detected. BD then returns to logic 0 approximately 25 ms after the tone pair ends.
	28	For factory use only. Leave open.
RD	10	Rotary Dial output. RD provides an early dial pulse presence signal that starts at the leading edge of the first break pulse and ends 100 ms after the trailing edge of the last pulse.
OFF-HOOK	11	Output. OFF-HOOK goes to the logic 1 state 100 ms after $\overline{LC}$ is pulled to logic 0. OFF-HOOK goes to the logic 0 state 300 ms after $\overline{LC}$ is pulled to logic 1.
DTI RDI	7 39	DTMF Inhibit input and Rotary Dial Inhibit input. For mixed DTMF and rotary dial operation, connect DTI and RDI to – V. For rotary dial operation only, connect DTI to + V. For DTMF operation only, connect RDI to + V. For mode locking on the first digit detected, connect both DTI and RDI to STROBE. The mode lock will be held until the detection circuits are reset by the POR, CLEAR, or $\overline{LC}$ inputs.
FCA FCB	20 21	Format Control A input and Format Control B input. As shown in Table 1, FCA and FCB determine the DATA output format. By holding both inputs at logic 1, all DATA outputs will remain at logic 1 until FCA and/or FCB are pulled to logic 0.
DATA 0 DATA 1 DATA 2 DATA 3 DATA 4 DATA 5 DATA 6 DATA 7 DATA 8 DATA 9 DATA 10 DATA 11	27 26 25 24 23 22 19 18 17 16 15 14	Data outputs. See Table 1 for the outputs associated with each output format. A DTMF digit is recognized when it has persisted for 40 ms. A rotary dial digit is recognized when an interdigital pause is detected.
STROBE	34	Valid data output. When DTMF digits are being detected, STROBE goes to the logic 1 state 10 microseconds after the DATA outputs change, and returns to the logic 0 state 25 ms after the loss or change of either tone constituting the detected digit. When rotary dial digits are being detected, STROBE goes to logic 1 for 200 ms after the interdigital pause is recognized. To read DATA during DTMF signal presence, use the leading edge of STROBE. To read DATA after DTMF signal presence, use the trailing edge of STROBE.
HOLD	33	Input. For applications where the output data has to remain unchanged for an extended time period, whether or not additional digits have been received, pull HOLD to logic 1 after STROBE goes to logic 1.
XTAL IN XTAL OUT	4 5	Input and output connections for a 3.579 MHz color burst television crystal.
447 kHz 881 Hz 20 Hz	35 36 37	For external use. Actual frequencies are XTAL frequency divided by 8, XTAL frequency divided by 4064, and XTAL frequency divided by 178,816. These are 50 percent duty cycle, PMOS logic level signals.

Table 3 Specifications

(−V = 0 V   +V = 12 V   Ambient Temperature = 25° C)

	Parameter	Min	Typ	Max	Units	Conditions
Logic Inputs	Logic 0 Voltage	− 0.3	—	2	V	
	Logic 1 Voltage	10	—	12.3	V	
	Capacitance	—	—	15	pF	
	Input Current	—	—	± 50	μA	
DC Signaling at LC Input	Logic 0 Voltage	− 0.3	—	2	V	
	Logic 1 Voltage	10	—	12.3	V	
	Off-Hook Recognition	95	—	105	ms	$\overline{LC}$ at 0 V
	Off-Hook Blanking (Note 1)	285	—	315	ms	$\overline{LC}$ at 0 V
	Break Recognition	24.5	—	29.5	ms	$\overline{LC}$ at 12 V
	Make Recognition	7	—	11	ms	$\overline{LC}$ at 0 V
	End of Digit Recognition	95	—	105	ms	$\overline{LC}$ at 0 V
	Rotary Interdigital Blanking	190	—	210	ms	$\overline{LC}$ at 0 V
	On-Hook Recognition	290	—	310	ms	$\overline{LC}$ at 12 V
TIP and RING Inputs	Input Impedance	450	—	—	kohm	at 1 kHz
	Common Mode Noise Tolerance, 15 to 100 Hz	60	—	—	Vrms	
	Dial Tone Tolerance	− 5	—	—	dBm (Note 2)	f ≤ 500 Hz
	Precise Dial Tone Tolerance	0	—	—	dBm (Note 2)	each tone, 350 and 440 Hz
	Signal Detect Level	− 30	—	+ 6	dBm (Note 2)	per tone
	Signal Reject Level	− 40	—	—	dBm (Note 2)	per tone
	Signal Detect Bandwidth	− 1.5% − 2	—	+ 1.5% + 2	Hz	
	Signal Reject Bandwidth	− 3.5%	—	+ 3.5%	Hz	
	Twist	—	± 10	—	dB	
	Noise Tolerance	− 43	—	—	dBm	(Note 4)
	Signal-to-Noise Ratio	—	—	18	dB	(Note 4)
	Signal Detect Time	—	—	40	ms	
	Signal Reject Time	20	—	—	ms	
	Interdigital Pause Detect Time	—	—	40	ms	
	Interdigital Pause Reject Time	22	—	—	ms	
DATA Outputs	Logic 0 Voltage	—	—	7	V	with 1 mA output current
	Logic 1 Voltage	10	—	—	V	with − 100 μA output current
	Logic 0 Current	1	—	—	mA	
	Logic 1 Current	− 0.1	—	—	mA	
	STROBE Output Delay	10	—	—	μs	measured from appearance of digit at DATA outputs
	BD Output Delay	—	—	16	ms	measured from appearance of tones at receiver
Non-DATA Outputs	Logic 0 Voltage	—	—	2	V	with 100 μA output current
	Logic 1 Voltage	10	—	—	V	with − 100 μA output current
	Logic 0 Current	0.1	—	—	mA	
	Logic 1 Current	− 0.1	—	—	mA	
Power	Supply Voltage (Operating)	11	12	13.5	V	+ V referenced to − V
	Supply Ripple (Note 3)	—	—	30	mV	
	Supply Current	—	—	85	mA	

Notes:
1. Off-hook blanking is the delay between $\overline{LC}$ going to logic 0 (after having been at logic 1 for more than 300 ms) and enabling of the digit detection circuits.
2. dBm = decibels above or below a reference power of one milliwatt into a 600-ohm load.
3. A bypass capacitor may be necessary. The internal digital logic of the M-927 may generate ripple voltages.
4. With the signal level − 25 dBm per tone, the signal 50 ms on and 50 ms off, no twist or frequency deviation, all 16 digits signalled randomly, 0 through 3 kHz flat Gaussian noise, and an error rate of less than one in 10,000. This is essentially the test method of EIA, USITA, and AT&T, except that the signal level is decreased to reflect the increased sensitivity of the M-927.
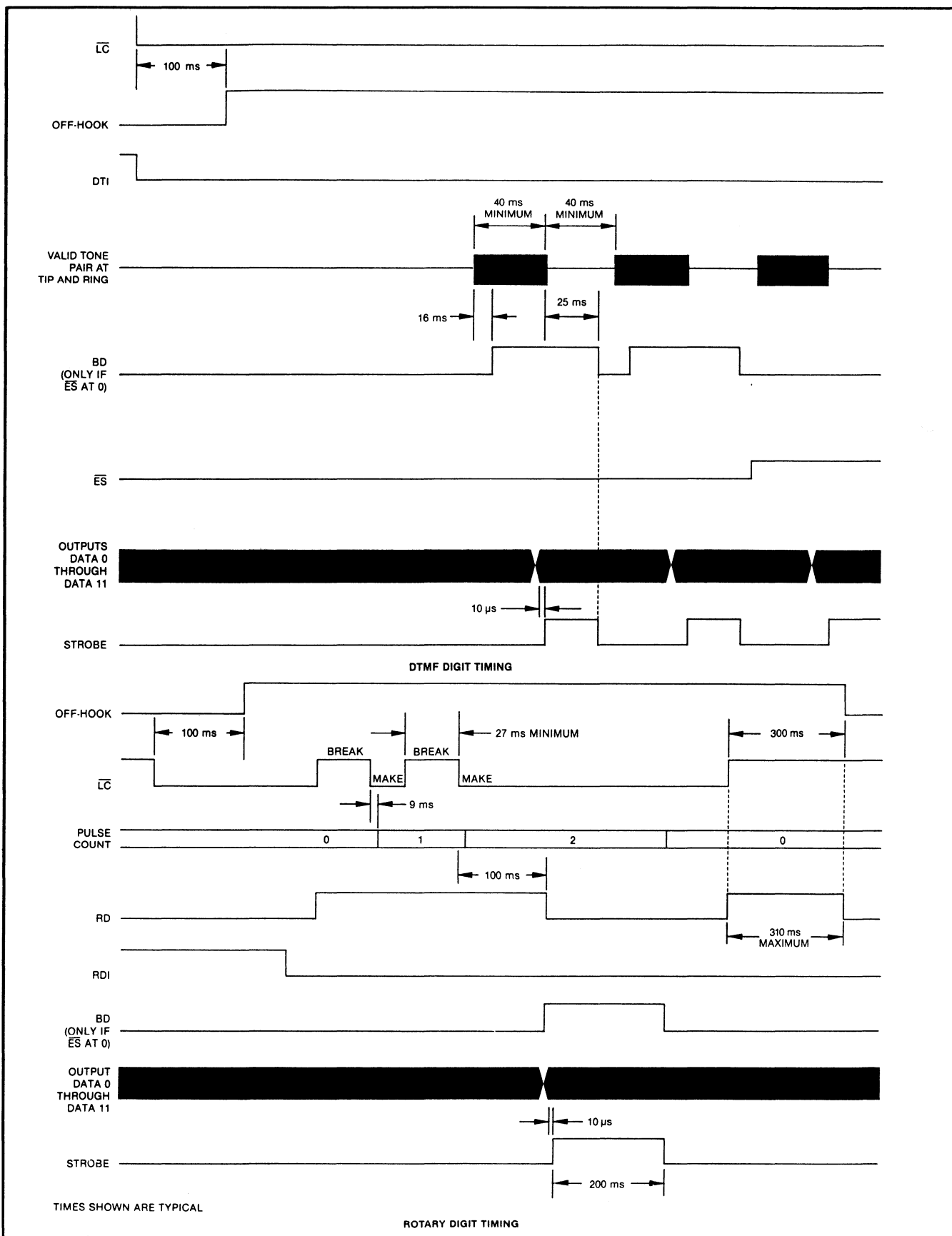
Figure 4 Timing Diagram
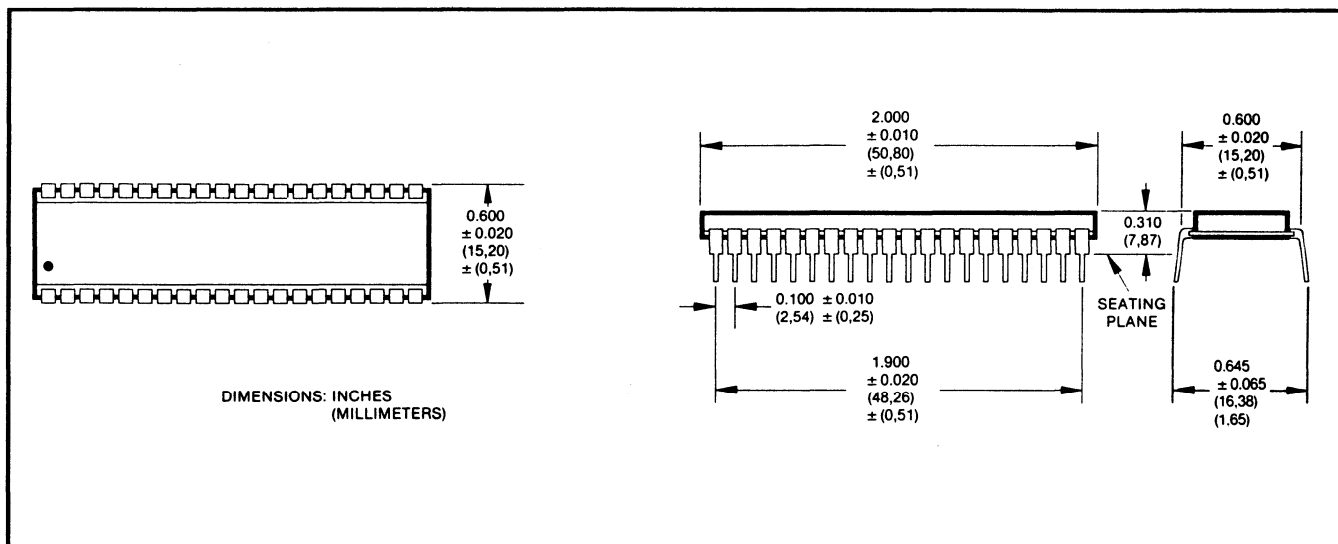
Figure 5 Package Dimensions
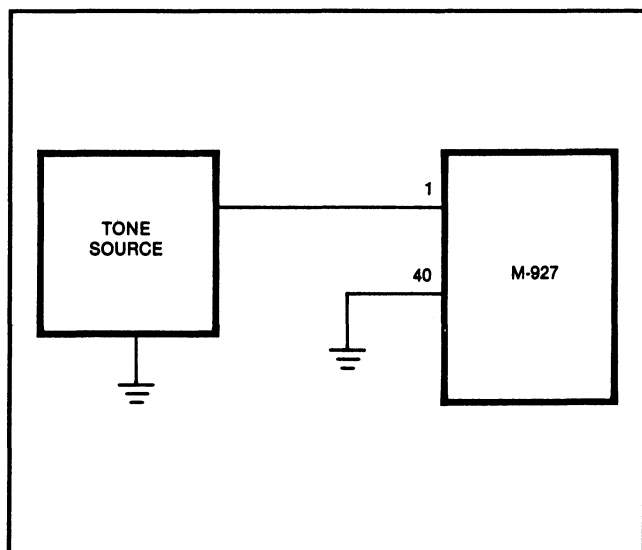
Figure 6 Single-Ended Input
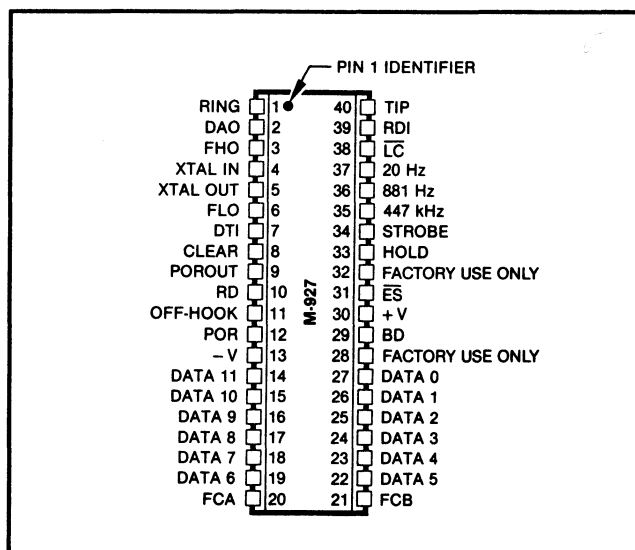
Figure 7 Pin Configuration

Table 4 Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2) .... 14.5 V
Power Dissipation .... 1.3 W
Voltage on Pins 1 and 40 .... (+ V + 250 V) to (− V − 250 V)
Voltage on Any Pin Except 1 and 40 .... (+ V + 0.3 V) to (− V − 0.3 V)
Storage Temperature Range .... − 40° to 150° C
Operating Temperature Range .... 0° to 70° C
Lead Soldering Temperature .... 260° C for 5 seconds at 0.035 inches from package

Notes:
1. Exceeding these ratings may damage the M-927.
2. + V referenced to − V. − V may be at ground.

M-937 HIGH-PERFORMANCE DTMF RECEIVER

The Teltone® M-937 is a high-quality Dual-Tone Multi-frequency (DTMF) digital receiver and rotary dial pulse counter. When connected to the voice pair (Tip and Ring) of a telephone line, the M-937 converts incoming signals to logic level outputs for use by other devices. The M-937's superior speech immunity makes it ideally suited for applications (such as telephone banking) where it must be connected to the line for extended periods of time.

The M-937 is manufactured under U.S. Patents 4,145,576 and 4,412,299.

Features

- Meets Danish specifications for B-subscribers
- Meets CEPT and CCITT recommendations for DTMF receivers
- Speech immunity improved by a factor of four over the industry-standard Teltone M-907
- Decodes all 16 DTMF signals
- Time-guarded rotary dial pulse counting
- Selectable output formats: binary, 2 of 8 (2 of 7), 1 of 12, or blank
- Separate dial pulse and early DTMF tone presence outputs
- Valid data output strobe
- Two different enable/disable inputs
- Wide dynamic range of 45 dB (+10 dBm maximum)
- Sensitivity externally adjustable from -46 to -20 dBm
- Pin-for-pin compatibility with the M-907
- Single 12 VDC supply operation
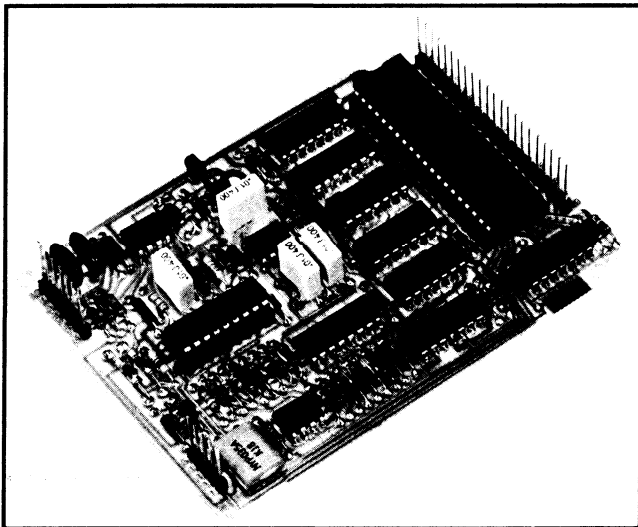
Figure 1 M-937 DTMF Receiver

Telephone Switching Applications

- Central office products
- PBX and intercom systems
- Consumer-oriented special feature phones and systems
- Radio equipment interface to the telephone network

Access and Control Applications

- Answering and recording devices
- Radio communication remote switching
- Remote control of machinery or microprocessors
- Monitoring equipment

Data Entry Applications

- Remote computer and peripheral systems interface
- Consumer credit and shopping systems
- Telephone banking, credit, and bill-paying systems
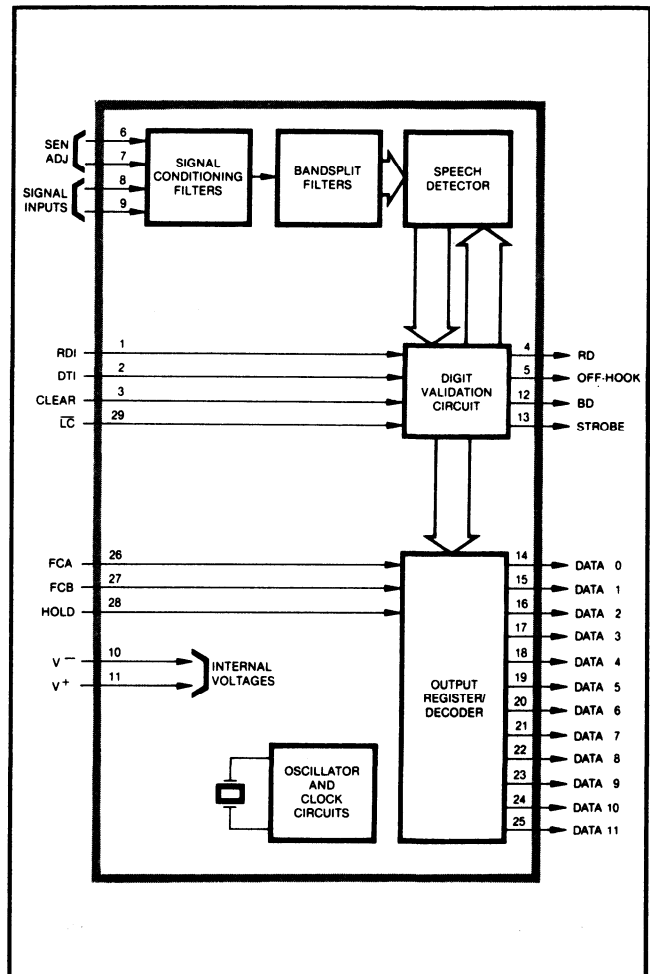
Figure 2 Block Diagram

Functional Description

As shown in Figure 2, the M-937 consists of a multistage DTMF input circuit, a digit validation circuit, and an output register/decoder.

The DTMF input circuit includes a signal conditioning stage, which provides common mode rejection, gain control, and dial tone and high-frequency noise rejection; a bandsplit stage, which separates the high-frequency DTMF component from the low-frequency DTMF component; and a speech detection circuit, which provides supplemental speech immu-

nity. The SEN ADJ inputs provide external control over the receiver's sensitivity.

The digit validation circuit compares the filtered tones to internal models of the DTMF frequencies. It also times and counts makes and breaks of loop current. The RDI and DTI inputs determine whether the unit will accept DTMF tones only or rotary dial pulses only, respond to signals of either kind, or provide mode locking on the first kind of digit detected.

The output register/decoder translates validated digits into the output format specified by the FCA and FCB inputs.

```
        1 OF 12 OUTPUT FORMAT              BINARY AND 2 OF 8 OR 2 OF 7
          FCA        FCB                       OUTPUT FORMATS
           0          0                     FCA          FCB
                                             1            0

DIGIT 1 2 3 4 5 6 7 8 9 0 * # A B C D   DIGIT 1 2 3 4 5 6 7 8 9 0 * # A B C D
    0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1        0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0
    1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1        1 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0
    2 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1        2 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0
    3 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1        3 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 0
    4 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1        4 0 0 0 1 1 1 1 1 1 1 1 1 0 1 1 1
    5 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1        5 1 1 1 0 0 0 1 1 1 1 1 1 1 1 0 1
    6 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1        6 1 1 1 1 1 1 0 0 0 1 1 1 1 1 0 1
    7 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1        7 1 1 1 1 1 1 1 1 1 0 0 0 1 1 1 0
    8 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1        8 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 1
    9 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1        9 1 0 1 1 0 1 1 0 1 0 1 0 1 1 1 1
   10 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1       10 1 1 0 1 1 0 1 1 0 1 0 1 1 0 1 1
   11 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1       11 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0


        BINARY OUTPUT FORMAT                    BLANK OUTPUT FORMAT
          FCA        FCB                       FCA          FCB
           0          1                         1            1

DIGIT 1 2 3 4 5 6 7 8 9 0 * # A B C D   DIGIT 1 2 3 4 5 6 7 8 9 0 * # A B C D
    0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0        0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
    1 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0        1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
    2 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0        2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
    3 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 0        3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
    4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1        4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
    5 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1        5 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
    6 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1        6 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
    7 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1        7 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
    8 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1        8 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
    9 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1        9 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
   10 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1       10 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
   11 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1       11 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
```

Figure 3 Output Formats

Table 1 Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	14.0 V
Voltage on Pins 8 and 9	$(V^+ + 300V)$ to $(V^- - 300 V)$
Voltage on Pins 8 and 9 (CCITT Rec K. 17.2)	1500 V
Voltage on Any Pin Except 8 and 9	$(V^+ + 0.3 V)$ to $(V^- - 0.3 V)$
Storage Temperature Range	$- 40°$ to $85°$ C
Operating Temperature Range	$0°$ to $70°$ C
Lead Soldering Temperature	$260°$ C for 5 seconds at 0.035 inches from package

Notes:
1. Exceeding these ratings may damage the M-937.
2. V^+ referenced to V^-. V^- may be at ground.

Table 2 Pin Functions

Pin	Number	Description
RDI DTI	1 2	Rotary Dial Inhibit input and DTMF inhibit input. For mixed DTMF and rotary dial operation, connect DTI and RDI to V⁻. For rotary dial operation only, connect DTI to V⁺. For DTMF operation only, connect RDI to V⁺. For mode locking on the first digit detected, connect both DTI and RDI to STROBE. The mode lock will be held until the detection circuits are reset by the CLEAR or $\overline{LC}$ inputs.
CLEAR	3	Receiver enable/disable input. A logic 1 (V⁺) applied to the CLEAR input instantaneously resets all detection circuits and forces the DATA outputs to the "D" column of the then enabled output format (see Figure 3). A logic 0 (V⁻) applied to the CLEAR input immediately enables the detection circuits, provided that $\overline{LC}$ has either remained at logic 0 or has not been at logic 1 for longer than 300 ms.
RD	4	Rotary Dial output. RD provides an early dial pulse presence signal that starts at the leading edge of the first break pulse and ends 100 ms after the trailing edge of the last pulse.
OFF-HOOK	5	Output. OFF-HOOK goes to the logic 1 state 100 ms after $\overline{LC}$ is pulled to logic 0. OFF-HOOK goes to the logic 0 state 300 ms after $\overline{LC}$ is pulled to logic 1.
SEN ADJ	6,7	Sensitivity Adjustment. SEN ADJ provides external control over the receiver's Accept Level range. With pins 6 and 7 open, the range is − 20 dBm to + 10 dBm. With pins 6 and 7 shorted, the range is − 46 dBm to − 1 dBm. By using resistive shunts, the range is continuously variable between these extremes. For example, a 25-kohm shunt will result in a range of about − 30 dBm to + 10 dBm.
SIGNAL INPUTS	8,9	AC-coupled, balanced DTMF input to the signal conditioning filters. These inputs may be connected directly to Tip and Ring.
V⁻ V⁺	10 11	Negative and positive power supply connections. V⁺ is 11 to 13.5 VDC more positive than V⁻.
BD	12	Button Down output. During DTMF operation, BD goes to the logic 1 state 16 ms after a tone pair is detected and returns to logic 0 approximately 25 ms after the tone pair ends. During rotary dial operation, BD follows the STROBE output.
STROBE	13	Valid data output. When DTMF digits are being detected, STROBE goes to the logic 1 state 10 microseconds after the DATA outputs change, and returns to the logic 0 state 25 ms after the loss or change of either tone constituting the detected digit. When rotary dial digits are being detected, STROBE goes to logic 1 for 200 ms after the interdigital pause is recognized. To read DATA during DTMF signal presence, use the leading edge of STROBE. To read DATA after DTMF signal presence, use the trailing edge of STROBE.
DATA 0 1 2 3 4 5 6 7 8 9 10 11	14 15 16 17 18 19 20 21 22 23 24 25	Data outputs. See Figure 3 for the outputs associated with each output format. A DTMF digit is recognized when it has persisted for 40 ms. A rotary dial digit is recognized when an interdigital pause is detected.
FCA FCB	26 27	Format Control A input and Format Control B input. As shown in Figure 3, FCA and FCB determine the DATA output format. Holding both inputs at logic 1 holds all DATA outputs at logic 1 until FCA and/or FCB are pulled to logic 0.
HOLD	28	Input. For applications where the output data has to remain unchanged for an extended time period, whether or not additional digits have been received, HOLD should be pulled to logic 1 after STROBE goes to logic 1.
$\overline{LC}$	29	Loop Current Not input. $\overline{LC}$ is both a receiver enable/disable input and the rotary dial pulse input. A logic 0 represents an off-hook condition, an interdigital pause, or a make period. A logic 1 represents an on-hook condition or a break period. For DTMF operation only, $\overline{LC}$ can be connected to V⁻; the receiver is then enabled as long as CLEAR is at logic 0.
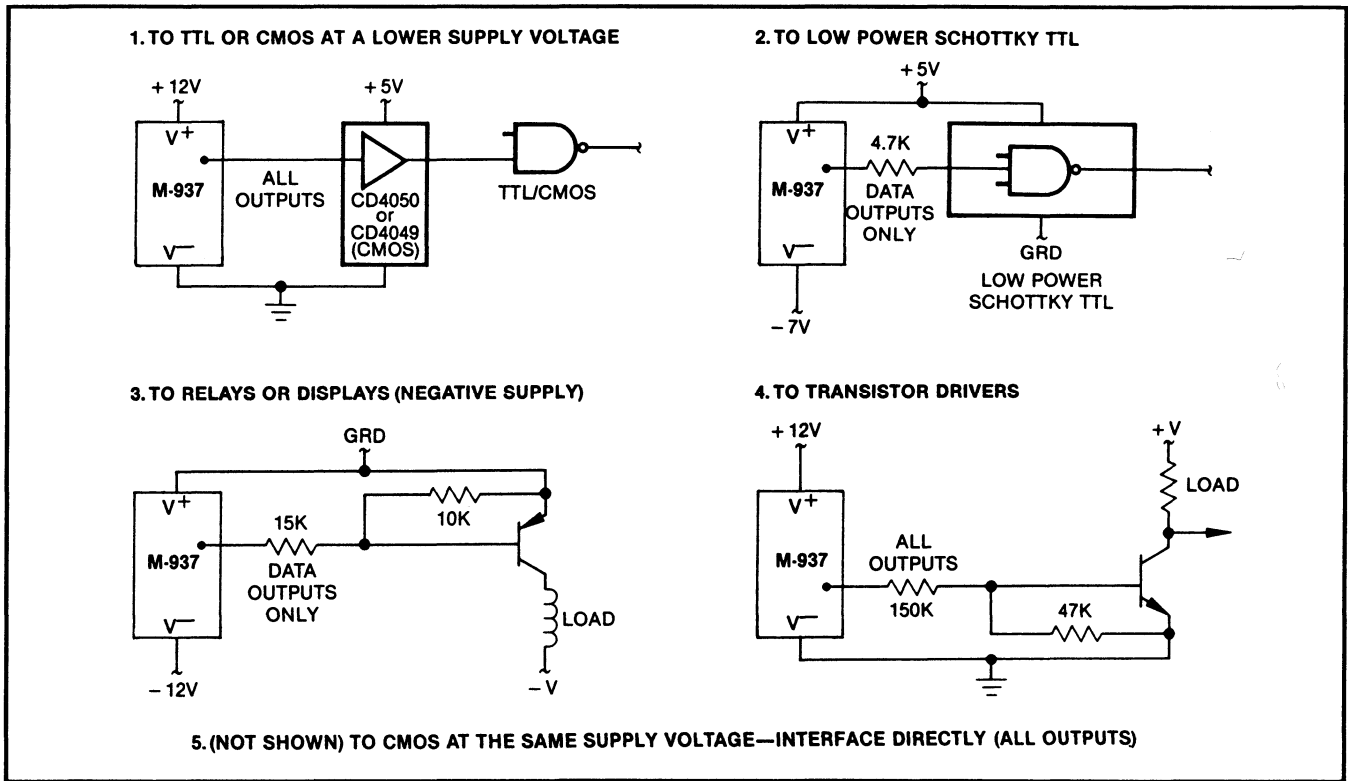
Figure 4 Output Interface Techniques
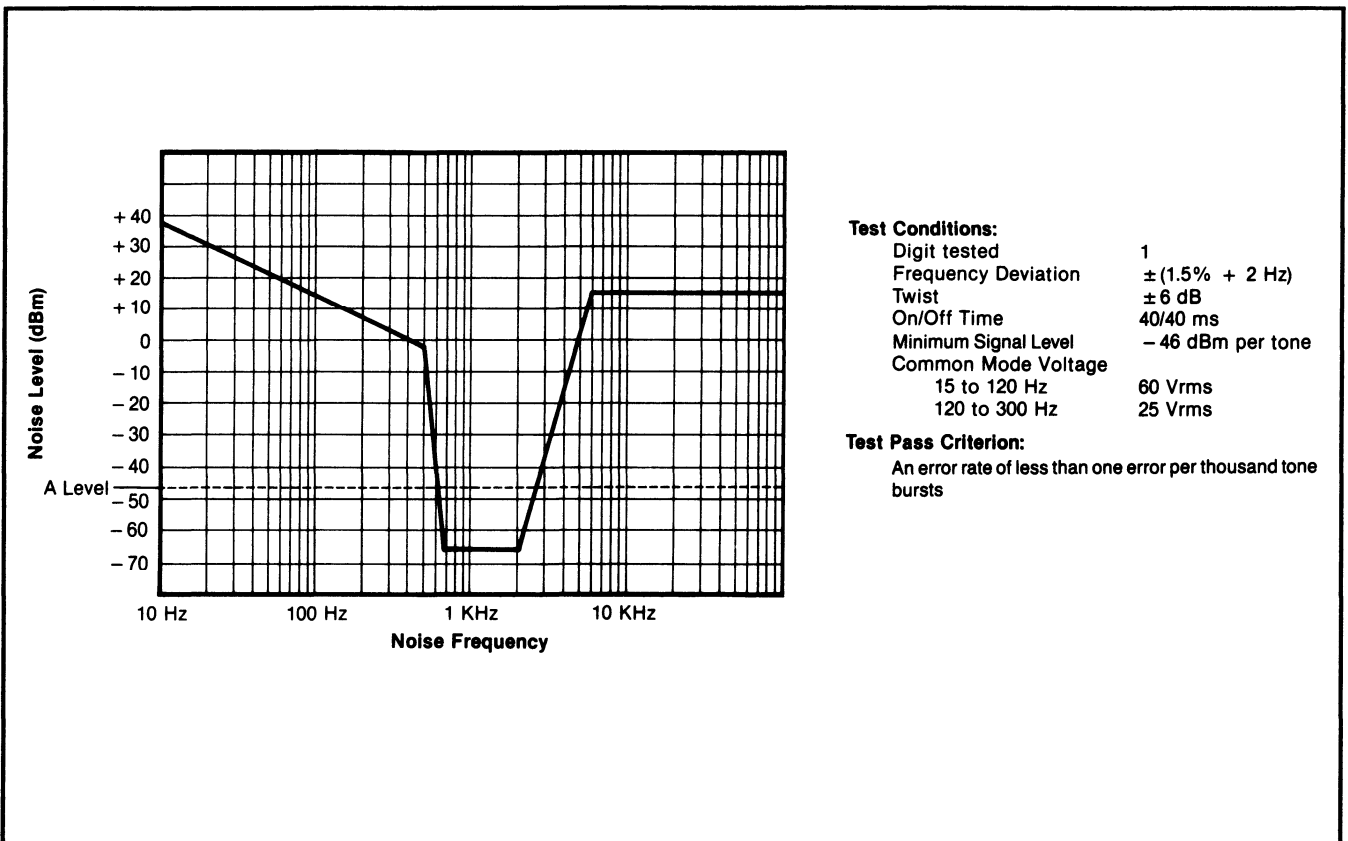
Figure 5 Typical Single-Frequency Noise Tolerance

Test Conditions:

Digit tested	1
Frequency Deviation	± (1.5% + 2 Hz)
Twist	± 6 dB
On/Off Time	40/40 ms
Minimum Signal Level	− 46 dBm per tone
Common Mode Voltage	
15 to 120 Hz	60 Vrms
120 to 300 Hz	25 Vrms

Test Pass Criterion:

An error rate of less than one error per thousand tone bursts

Table 3 DC Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units	Notes
Power	Supply Voltage	V^+ referenced to V^-	11		13.5	V	1
	Supply Current			60		mA	
	Supply Current	$(V^+) - (V^-) = 13.5V$, $T_A = 0° C$			95	mA	
Logic Inputs	Logic 0 Level				$(V^-) + 5.8$	V	
	Logic 1 Level		$(V^+) - 2.5$			V	
	Capacitance				20	pF	
	Input Current				±50	µA	2
DATA Outputs	Logic 0 Current Sink	Output at $(V^-) + 7$ V			1	mA	
	Logic 1 Current Source	Output at $(V^+) - 2$ V			100	µA	
Non-DATA Outputs	Logic 0 Current Sink	Output at $(V^-) + 2$ V			100	µA	
	Logic 1 Current Source	Output at $(V^+) - 2$ V			100	µA	

Notes:
1. V^+ more positive than V^-. V^- may be at ground.
2. The input current must be sourced or sunk to drive an input to its opposite state.

Table 4 AC (Dynamic) Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units	Notes
Input Impedance	f = 1 kHz	300			kohm	
Common Mode Noise Tolerance	f = 15 to 120 Hz	60	100		Vrms	
Common Mode Noise Tolerance	f = 120 to 300 Hz	25	30		Vrms	
Single-Frequency Dial Tone Tolerance	f ≤ 480 Hz	−5	0		dBm	1
Precise Dial Tone Tolerance		−12			dBm	1,2
Max Accept Level	SEN ADJ open	+ 10	+ 20		dBm	1,3,9
Max Accept Level	SEN ADJ shorted	− 1	+ 5		dBm	1,3,9
Max Accept Level	SEN ADJ with resistive shunt	A + 45	A + 50	10	dBm	1,3,4,9
Min Accept Level	SEN ADJ open	− 28	− 22	− 20	dBm	1,3,9
Min Accept Level	SEN ADJ shorted	− 54	− 48	− 46	dBm	1,3,9
Signal-to-Noise Ratio Requirement for Signal Detection			10	15	dB	5
Signal-to-Noise Ratio Requirement for Signal Detection			20	22	dB	6
Twist Tolerance	nominal frequency, 45 ms on/45 ms off	10	15		dB	8
Signal Recognition Time		30	37	40	ms	
Interdigital Pause Accept Time		20	25	40	ms	
Pulse Width Required to Reset with CLEAR Input				25	µs	
Off-Hook Recognition	$\overline{LC}$ at logic 0	95	100	105	ms	
On-Hook Recognition	$\overline{LC}$ at logic 1	290	300	310	ms	
Off-Hook Blanking	$\overline{LC}$ at logic 0	285	300	315	ms	7
Break Recognition	$\overline{LC}$ at logic 1	24.5		29.5	ms	
Make Recognition	$\overline{LC}$ at logic 0	7	9	11	ms	
End of Digit Recognition	$\overline{LC}$ at logic 0	95	100	105	ms	
Rotary Interdigital Blanking		190	200	210	ms	

Notes:
1. dBm = decibels above or below a reference power of one milliwatt into a 600-ohm load.
2. Per tone. Precise Dial Tone is 350 Hz with 440 Hz, ± 0.5 percent.
3. 40 ms on/40 ms off, with no more than ± (1.5% + 2 Hz) frequency deviation and no more than ± 6 dB twist
4. A = Min Accept Level
5. With the signal level at A + 5 dBm per tone, the signal 50 ms on and 50 ms off, no twist or frequency deviation, all 16 digits signalled randomly, 0 through 3 kHz flat Gaussian noise, and an error rate of less than one in 10,000. This is essentially the test method of EIA, USITA, and AT&T.
6. Single frequency in the band 600 Hz to 2000 Hz, 40 ms on/40 ms off.
7. Off-Hook Blanking is the delay between $\overline{LC}$ going to logic 0 (after having been at logic 1 longer than 300 ms) and enabling the digit detection circuits.
8. For signal levels between the A level and A + 35 dBm.
9. Measurement made with a 12 ± 0.1 V power supply. Accept levels may change ± 1 dBm over the supply range of 11 to 13.5 V.

DTMF DIGIT TIMING

ROTARY DIGIT TIMING

TIMES SHOWN ARE TYPICAL

Figure 6 Timing Diagram

Figure 7 Unit Dimensions
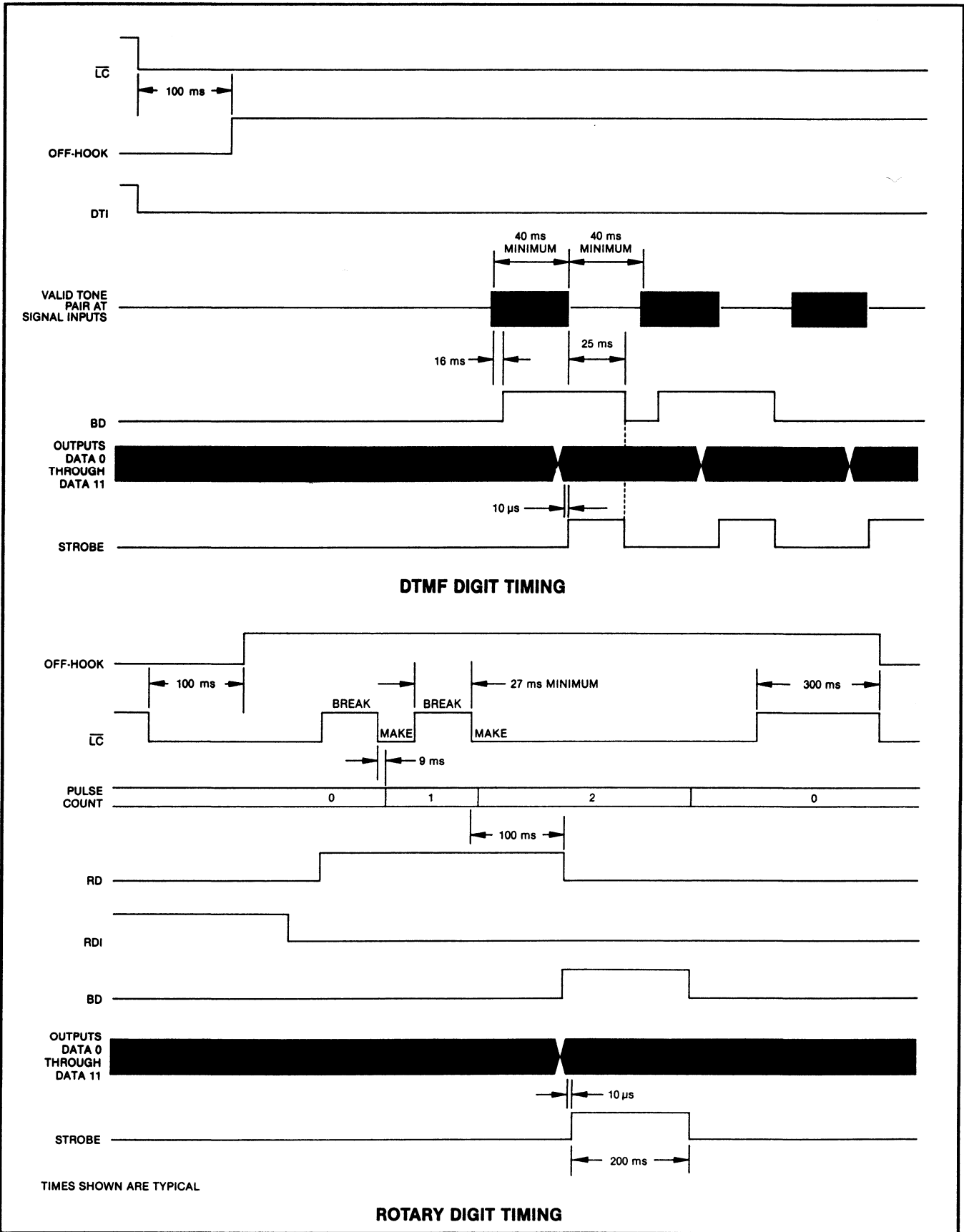
M-947 DTMF RECEIVER

The Teltone® M-947 combines switched-capacitor and digital techniques to decode Dual-Tone Multifrequency (DTMF) signals to four-bit binary data. No prefiltering of the DTMF signal is required. The M-947 is contained in a 22-pin DIP, operates from a single 12-volt supply, and uses an inexpensive 3.579-MHz television crystal for frequency reference.

The SIGNAL IN input to the M-947 is typically connected to a Touch-Tone® telephone, radio receiver, tape player, or other DTMF signal source. The M-947 filters out dial tone and noise, splits the signal into its high- and low-frequency components, and analyzes these components to determine the validity of the composite pair. Valid signals are decoded and stored at the DATA outputs; invalid signals are ignored. The CLEAR input resets all M-947 functions, while the BD and DV outputs provide, respectively, an early indication of signal presence and a DATA strobe.

All M-947 outputs interface with CMOS, standard voltage translation ICs, and transistor drivers. For applications incorporating multiple M-947s, the output from one oscillator can be cascaded through them all.

The M-947 is manufactured under U.S. Patent 4,145,576.

Features
* Decodes all 16 DTMF signals
* Capacitor-coupled SIGNAL IN input
* Latching four-bit binary output
* Built-in dial tone and noise filtering
* Superior immunity to speech and noise
* Early signal presence and valid data strobe outputs
* Single 12-VDC supply
* 22-pin DIP for high-density packaging

Telephone Switching Applications
* Central office products
* PBX and key system products
* Radio telephone products

Access and Control Applications
* Answering and recording devices
* Monitoring and alarm devices
* Equipment control devices

Data Entry Applications
* Computer systems
* Telephone banking, credit, bill-paying, and shopping systems
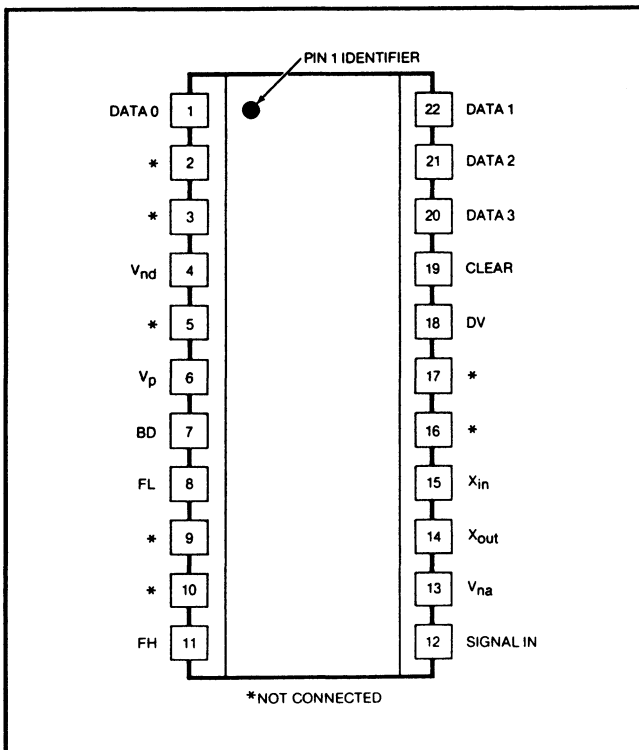
Figure 1 Pin Diagram
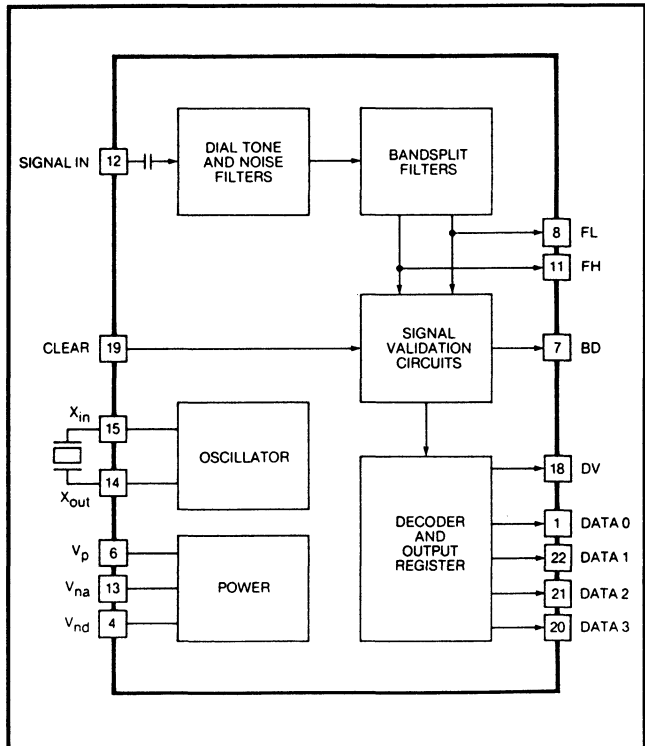
Figure 2 Block Diagram

Table 1 DTMF to Binary Decoding

SIGNAL	LOW-FREQUENCY COMPONENT	HIGH FREQUENCY COMPONENT	DATA OUTPUTS 3 2 1 0	OUTPUT EQUIVALENT HEX	OUTPUT EQUIVALENT OCTAL
1	697 Hz	1209 Hz	0 0 0 1	1	1
2	697 Hz	1336 Hz	0 0 1 0	2	2
3	697 Hz	1477 Hz	0 0 1 1	3	3
4	770 Hz	1209 Hz	0 1 0 0	4	4
5	770 Hz	1336 Hz	0 1 0 1	5	5
6	770 Hz	1477 Hz	0 1 1 0	6	6
7	852 Hz	1209 Hz	0 1 1 1	7	7
8	852 Hz	1336 Hz	1 0 0 0	8	10
9	852 Hz	1477 Hz	1 0 0 1	9	11
0	941 Hz	1336 Hz	1 0 1 0	A	12
*	941 Hz	1209 Hz	1 0 1 1	B	13
#	941 Hz	1477 Hz	1 1 0 0	C	14
A	697 Hz	1633 Hz	1 1 0 1	D	15
B	770 Hz	1633 Hz	1 1 1 0	E	16
C	852 Hz	1633 Hz	1 1 1 1	F	17
D	941 Hz	1633 Hz	0 0 0 0	0	0

Table 2 Pin Functions

Pin	Function
V_p	Postive power supply connection.
V_{na}, V_{nd}	Negative power supply connections. V_{na} and V_{nd} should be at equal potential.
CLEAR	Clear. As shown in Figure 3, logic 1 applied to CLEAR resets the Signal Validation Circuits (see Figure 2) and forces the DATA outputs to the "D" row (all zeros) of Table 1. Logic 0 applied to CLEAR enables the Signal Validation Circuits.
SIGNAL IN	DTMF input, internally AC-coupled. See Table 1 for the frequency pairs associated with each DTMF signal.
DATA 0-3	Data. As shown in Figure 3, the DATA outputs change when a signal is validated and are maintained until a new signal is validated or logic 1 is applied to CLEAR. See Table 1 for the outputs associated with each DTMF signal.
BD	Button Down. As shown in Figure 3, BD goes to logic 1 after a signal is detected but before it has been validated as one of the frequency pairs listed in Table 2. If the signal is determined to be invalid, BD returns to logic 0 immediately. If the signal is determined to be valid, BD returns to logic 0 after the signal ends.
DV	Data Valid. As shown in Figure 3, DV goes to logic 1 after the DATA outputs change and returns to logic 0 after the signal ends. To read DATA during signal presence, use the leading edge of DV. To read DATA after signal presence, use the trailing edge of DV.
FL, FH	Normally not used.
X_{in}, X_{out}	Input and output connections for a 3.579-MHz television color burst crystal.
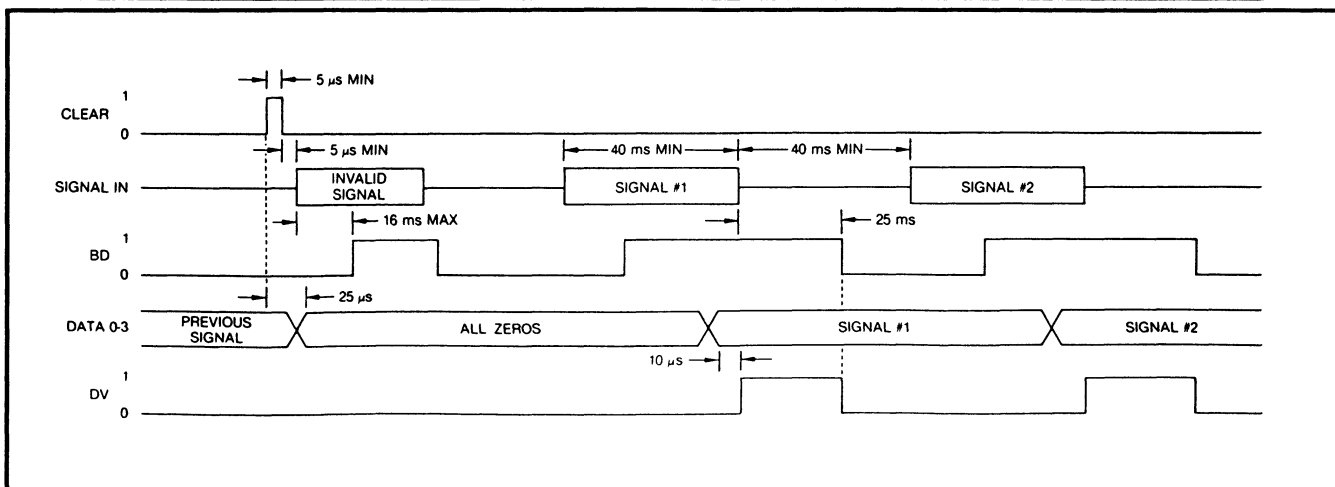
Figure 3 Timing Diagram
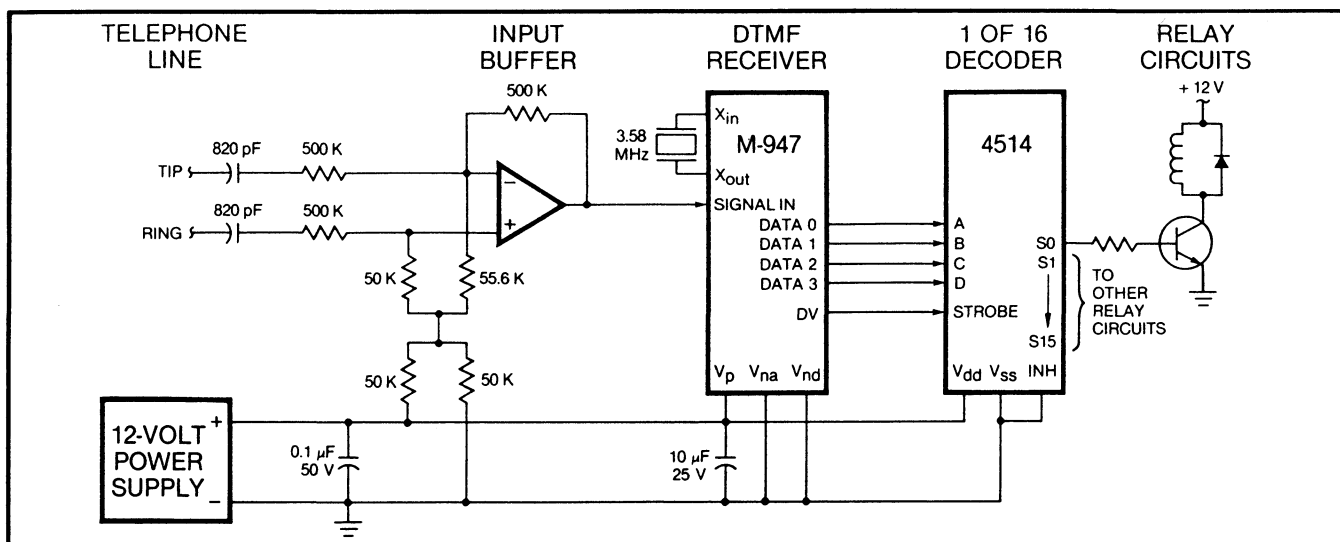
Figure 4 Controlling Relays over a Telephone Line
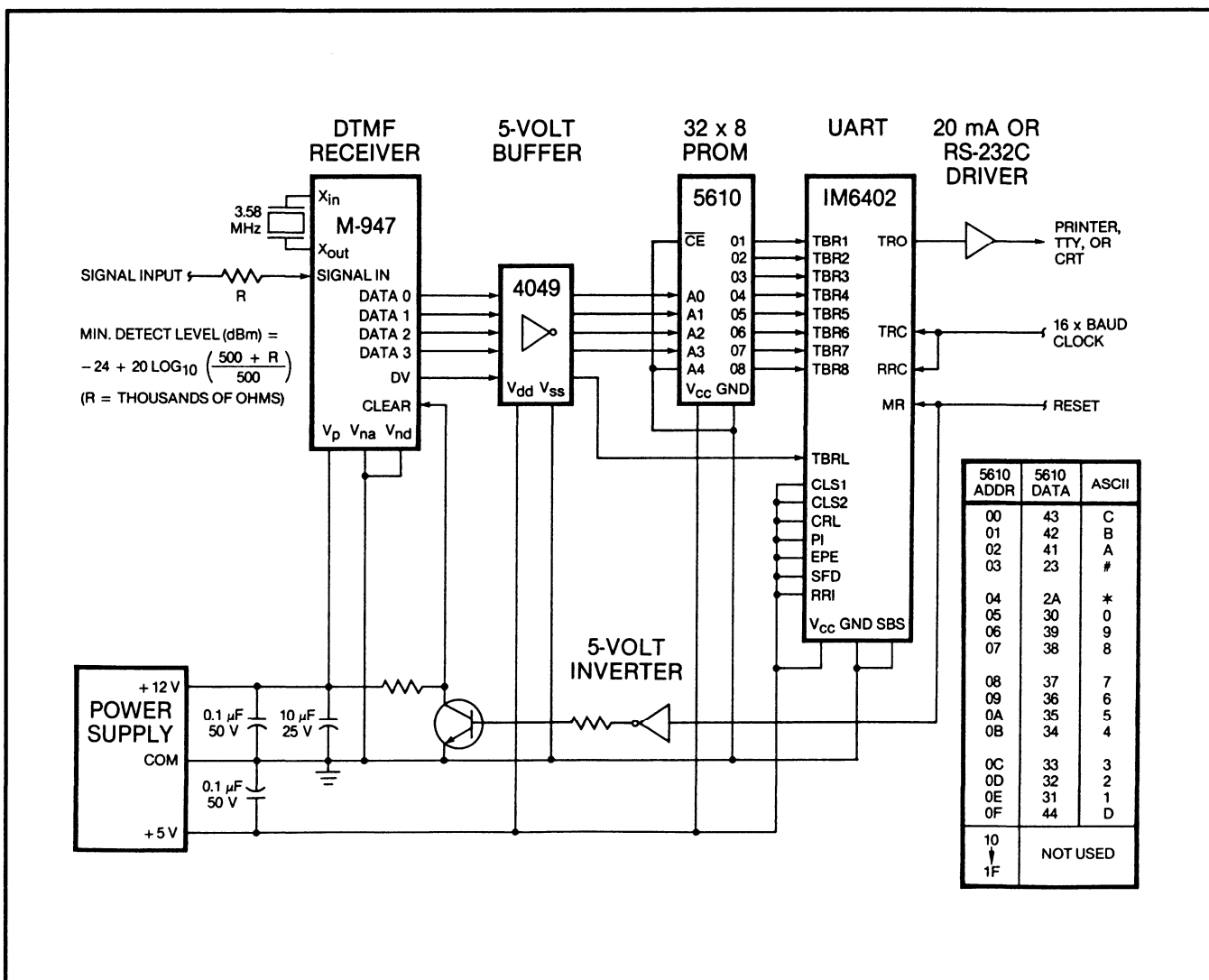
Figure 5 DTMF to Asynchronous Serial ASCII with Adjustable Minimum Detect Level
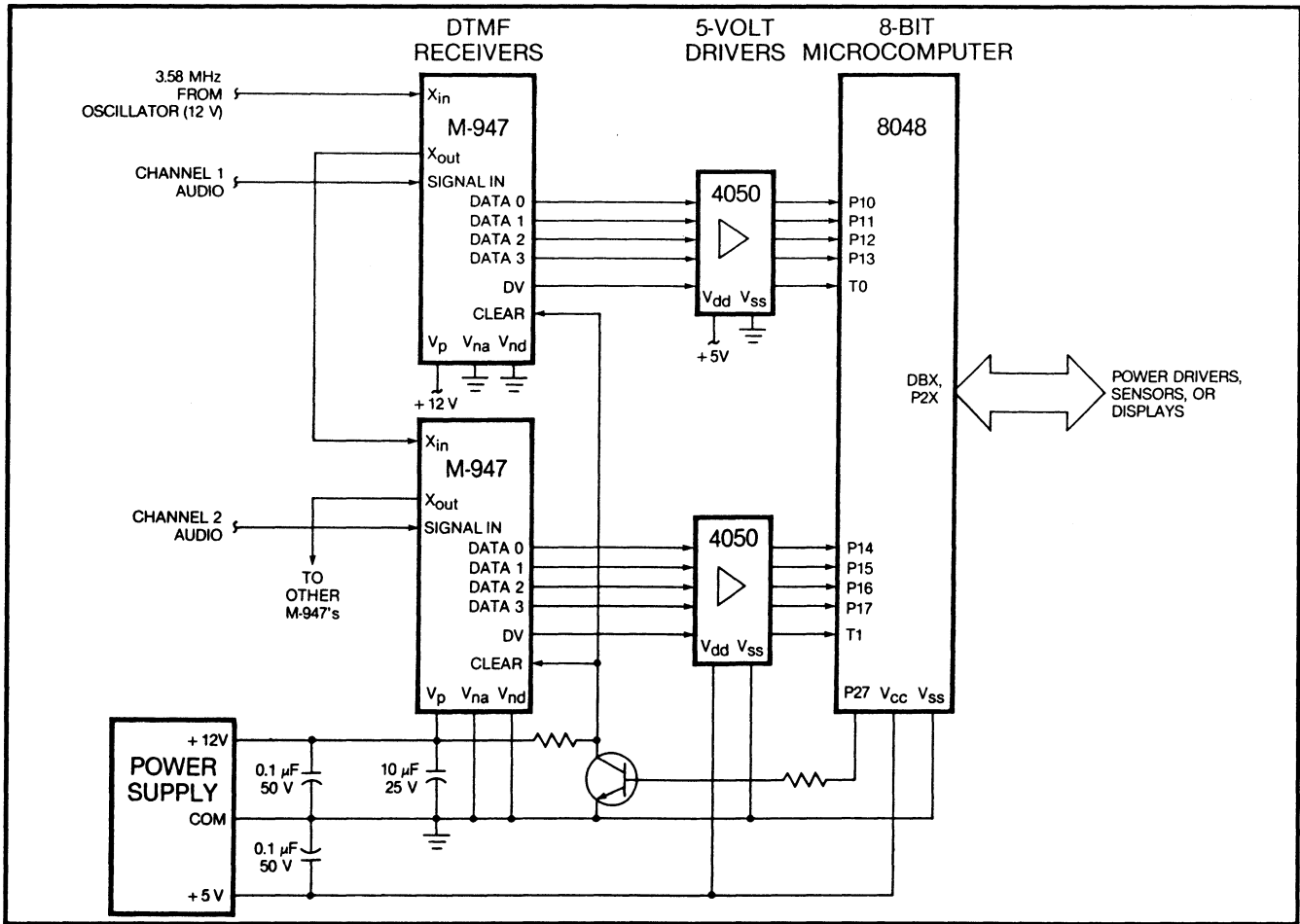
Figure 6 Intelligent Two-Channel DTMF Receiver Using an External Clock Source
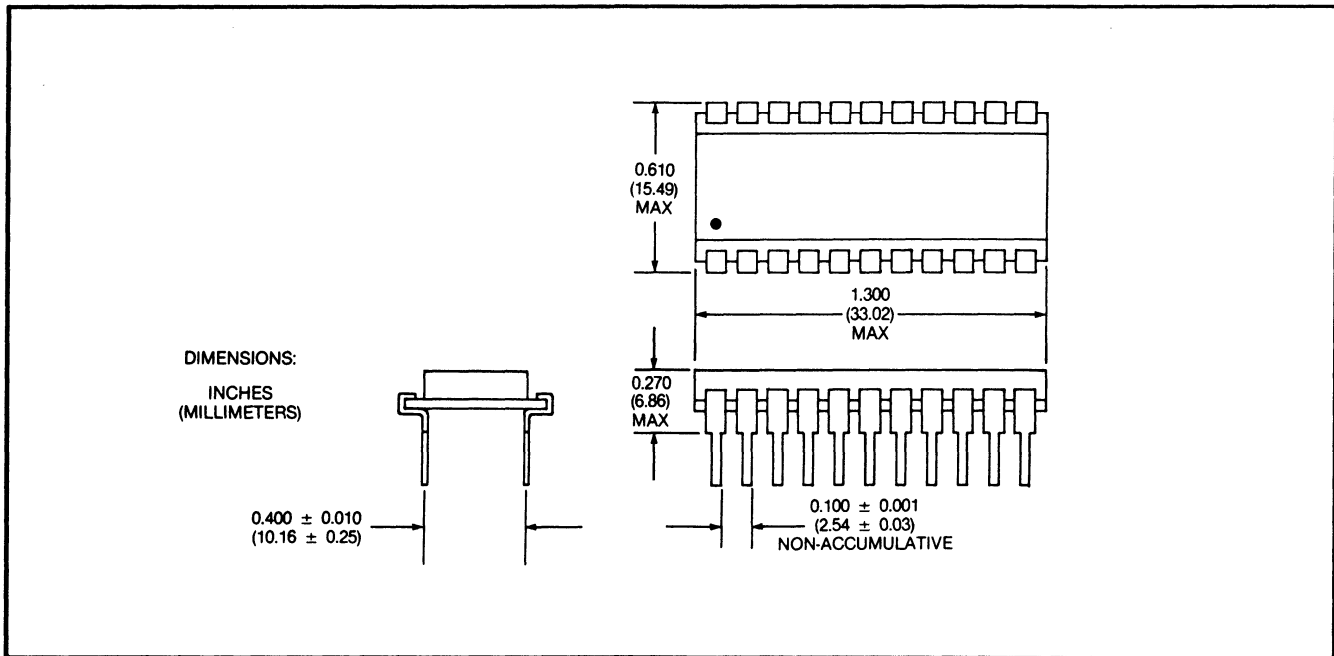
Figure 7 Package Dimensions

Table 3 Absolute Maximum Ratings (Note 1)

DC Supply Voltage (Note 2) .... 14.5 V
Voltage on SIGNAL IN .... $(V_p + 25\ V)$ to $(V_{na} - 25\ V)$
Voltage on Any Pin Except SIGNAL IN .... $(V_p + 0.3\ V)$ to $(V_{na} - 0.3\ V)$
Storage Temperature Range .... $-40°$ to $85°$ C
Operating Temperature Range .... $0°$ to $70°$ C
Lead Soldering Temperature .... $260°$ C for 5 seconds at 0.035 inches (0.89 mm) from package

Notes:
1. Exceeding these ratings may permanently damage the M-947.
2. V_p referenced to V_{na}. V_{na} should be at equal potential to V_{nd}. V_{na} may be at ground.

Table 4 Specifications

	Parameter	Min	Max	Units	Notes
Power Requirements	Supply Voltage	11.0	13.5	Vdc	1
	Supply Voltage Ripple	—	30	mVpp	2
	Supply Current	—	85	mA	
CLEAR Input	Logic 0 Voltage	−0.3	2.0	V	3
Requirements	Logic 1 Voltage	10.0	12.3	V	3
	Input Current	−50	50	μA	
SIGNAL IN Input	Signal Level	−24	+6	dBm	4, 5, 6
Requirements	Signal Duration	40	—	ms	
	Interval Between Signals	40	—	ms	
	Signal Cycle Time	85	—	ms	
	Signal Present Without Detection	—	20	ms	
	Interruption of Signal Without Redetection	—	20	ms	
	Signal Frequency Deviation	−(1.5% + 2)	+(1.5% +2)	Hz	
	Twist	−10	+10	dB	7
	Signal-to-Noise Ratio	18	—	dB	6, 8
	Noise Level	—	−37	dBm	5, 6
	Dial Tone Level (f≤500 Hz)	—	−5	dBm	4, 5
	Precise Dial Tone Level	—	0	dBm	4, 5, 9
DATA, BD, and	Logic 0 Voltage	—	2	V	3
DV Output	Logic 1 Voltage	10	—	V	3
Characteristics	Output Current	−0.1	0.1	mA	
Miscellaneous	Power Dissipation	—	1.3	W	
Characteristics	CLEAR Input Capacitance	—	15	pF	
	SIGNAL IN Input Impedance (1 kHz)	450k	—	ohms	

Notes:

1. V_p referenced to V_{na}. V_{na} may be at ground.

2. A bypass capacitor may be necessary.

3. Logic levels are shown for a supply voltage $(V_p - V_{na})$ of 12 V, and are referenced to V_{na}.

4. Per tone.

5. The unit "dBm" refers to decibels above or below a reference power of one milliwatt into a 600-ohm load. (For example, −24 dBm equals 49 mV.)

6. Measurement made with a 12 ±0.1 V power supply. Levels may change ±1 dB over the supply range of 11 to 13.5 V.

7. Twist is defined as the ratio of the level of the high-frequency DTMF component to the level of the low-frequency DTMF component.

8. With the signal level −19 dBm per component, the signal 50 ms on and 50 ms off, no twist or frequency deviation, all 16 signals received randomly, 0 through 3 kHz flat Gaussian noise, and an error rate of less than one in 10,000. This is essentially the test method of EIA, AT&T, and USITA.

9. Precise Dial Tone is 350 Hz and 440 Hz.

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Teltone Limited / 3375-14th Avenue, Markham, Ontario, Canada L3R 2L6   Phone: 416-475-0837   Fax: 416-474-9151   Envoy User Name: TTL.HQ

7-48

M-956 DTMF RECEIVER

The Teltone® M-956 (see Figure 1) combines switched-capacitor and digital frequency measuring techniques to decode Dual-Tone Multifrequency (DTMF) signals to four-bit binary data. Fabricated as a monolithic integrated circuit using low-power CMOS processing, the M-956 is packaged in a 22-pin DIP and operates from a single 5-volt DC supply. An inexpensive 3.58-MHz television crystal and resistor are the only external components required. High system density may be achieved by using the clock output of one crystal-connected receiver to drive the time bases of additional receivers.

The SIGNAL IN input to the M-956 (see Figure 2) interfaces readily to telephone lines, radio receivers, tape players, and other DTMF signal sources. The input stages of the M-956 filter out noise, split the signal into its high- and low-frequency components, and hard-limit each component to provide automatic gain control. Four discriminators in each group then detect the individual tones. Postprocessing stages of the M-956 time the tone durations and store binary data for outputting as determined by the HEX input. The STROBE output is activated by the presence of valid data in the output register and cleared by the detection of a valid end-of-signal pause or by the CLEAR input. An early signal presence indicator, BD, facilitates applications requiring tone blocking. The data outputs operate with simple logic circuits or

microprocessors, and are three-state enabled to facilitate bus-oriented architectures.

The M-956 is manufactured under U.S. Patent 4,145,576.

Features
* Complete DTMF receiver in 22-pin DIP (plastic or CerDIP)
* Decodes all 16 DTMF digits
* Excellent speech immunity
* Meets telephone impulse noise immunity standards
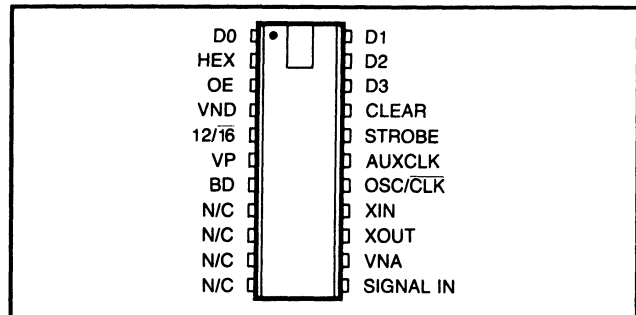
Figure 1 Pin Diagram
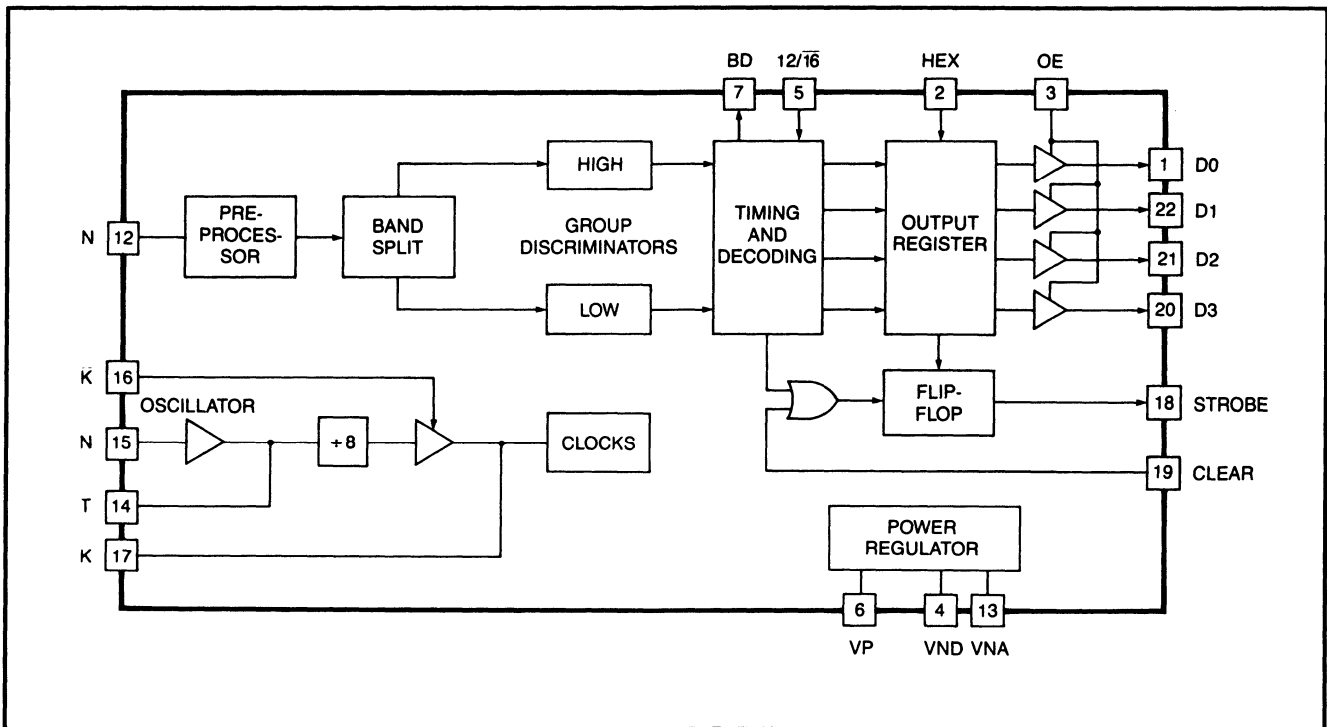
Figure 2   Block Diagram

- Selectable 4-bit hexadecimal or binary coded 2 of 8 output
- Fabricated using low-power CMOS technology
- Operates on single DC supply
- Uses inexpensive 3.58-MHz crystal
- Three-state outputs

Applications

- Central office products
- PBX and key systems
- Radio telephones
- Remote control and monitoring devices
- Computer data entry systems

Table 1 Pin Functions

Pin	Function
SIGNAL IN	DTMF input. Timings are shown in Figure 3. Internally biased so that the input signal may be AC coupled, SIGNAL IN also permits DC coupling as long as the input voltage does not exceed the positive supply. Proper coupling is shown in Figure 6. See Table 2 for the frequency pairs associated with each DTMF signal.
12/$\overline{16}$	DTMF signal detection control. When 12/$\overline{16}$ is at logic "1", the M-956 detects the 12 most commonly used DTMF signals (1 through #). When 12/$\overline{16}$ is at logic "0", the M-956 detects all 16 DTMF signals (1 through D).
D3, D2, D1, D0	Data outputs. When enabled by the OE input, the data outputs provide the code corresponding to the detected digit in the format programmed by the HEX pin. See Table 2. The data outputs become valid after a tone pair has been detected and are cleared when a valid pause is timed. Timings are shown in Figure 3.
OE	Output enable. When OE is at logic "1", the data outputs are in the CMOS push/pull state and represent the contents of the output register (see Figure 2). When OE is driven to logic "0", the data outputs are forced to the high-impedance or "third" state. Timings are shown in Figure 3.
HEX	Binary output format control. When HEX is at logic "1", the output of the M-956 is full, 4-bit binary. When HEX is at logic "0", the output is binary coded 2-of-8. Table 2 shows the output codes.
STROBE	Valid data indication. STROBE goes to logic "1" after a valid tone pair is sensed and decoded at the data outputs. STROBE remains at logic "1" until a valid pause occurs or the CLEAR input is driven to logic "1", whichever is earlier. Timings are shown in Figure 3.
CLEAR	STROBE control. Driving CLEAR to logic "1" forces the STROBE output to logic "0". When CLEAR is at logic "0", STROBE is forced to logic "0" only when a valid pause is detected.
BD	Early signal presence output. BD indicates that a possible signal has been detected and is being validated. As shown in Figure 3, BD precedes STROBE and the data outputs.
XIN, XOUT	Crystal connections. When an auxiliary clock is used, XIN should be tied to logic "1". See Figure 6.
OSC/$\overline{CLK}$	Time base control. When OSC/$\overline{CLK}$ is at logic "1", the output of the M-957's internal oscillator is selected as the time base. When OSC/$\overline{CLK}$ is at logic "0" and XIN is at logic "1", the AUXCLK input is selected as the time base.
AUXCLK	Auxiliary clock input. When OSC/$\overline{CLK}$ and XIN are at logic "0", the AUXCLK input is selected as the M-956's time base. The auxiliary input must be 3.58 MHz divided by 8 for the M-956 to operate to specifications. If unused, AUXCLK should be left open.
VNA, VND	Negative analog and digital power supply connections. Separated on the chip for greater system flexibility, VNA and VND should be at equal potential.
VP	Positive power supply connection.
N/C	Not connected. These pins have no internal connection and may be left floating.

Table 2 DTMF to Binary Decoding

SIGNAL	LOW-FREQUENCY COMPONENT (Hz)	HIGH-FREQUENCY COMPONENT (Hz)	HEX OUTPUT FORMAT 3 2 1 0	2-OF-8 OUTPUT FORMAT 3 2 1 0
1	697	1209	0 0 0 1	0 0 0 0
2	697	1336	0 0 1 0	0 0 0 1
3	697	1477	0 0 1 1	0 0 1 0
4	770	1209	0 1 0 0	0 1 0 0
5	770	1336	0 1 0 1	0 1 0 1
6	770	1477	0 1 1 0	0 1 1 0
7	852	1209	0 1 1 1	1 0 0 0
8	852	1336	1 0 0 0	1 0 0 1
9	852	1477	1 0 0 1	1 0 1 0
0	941	1336	1 0 1 0	1 1 0 1
*	941	1209	1 0 1 1	1 1 0 0
#	941	1477	1 1 0 0	1 1 1 0
A	697	1633	1 1 0 1	0 0 1 1
B	770	1633	1 1 1 0	0 1 1 1
C	852	1633	1 1 1 1	1 0 1 1
D	941	1633	0 0 0 0	1 1 1 1

Note: The M-956 detects signals A through D only when the 12/16 input is at logic "1".
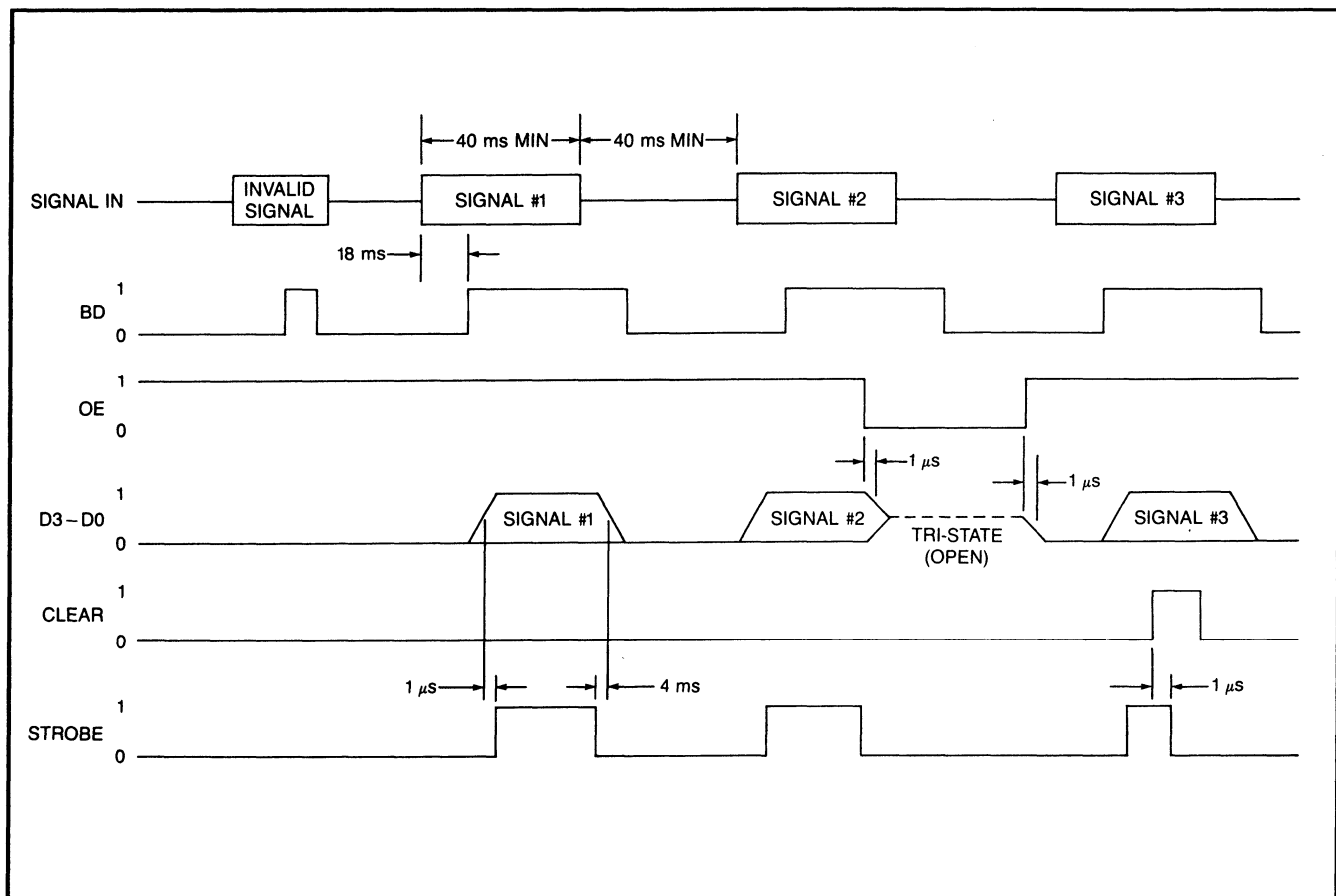
Figure 3 Timing Diagram
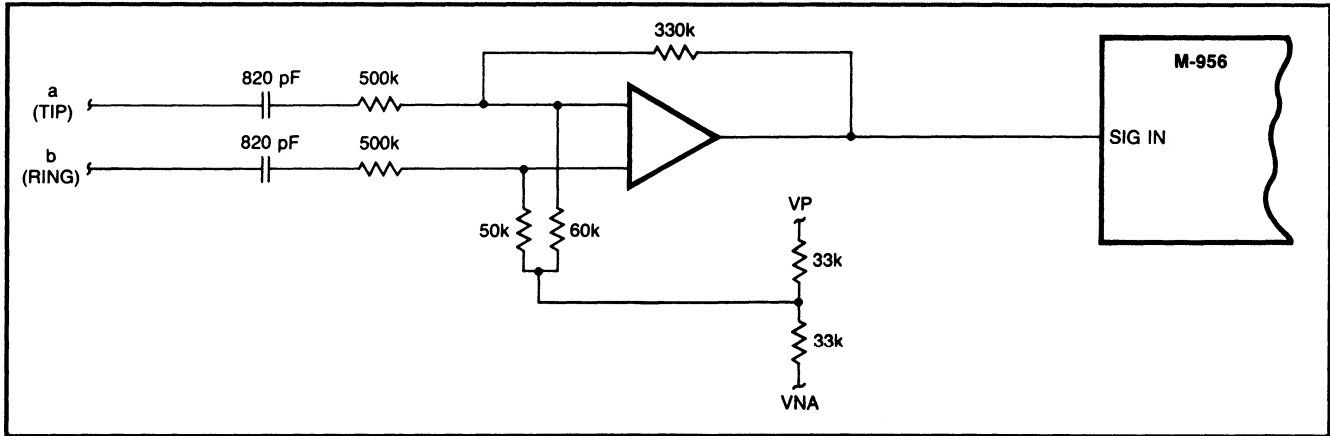
Figure 4 Telephone Line Differential Input Interface
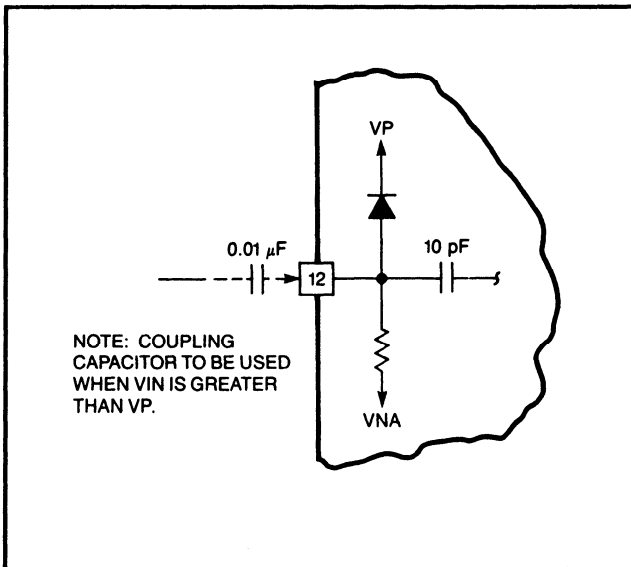
Figure 5 Input Signal Configuration
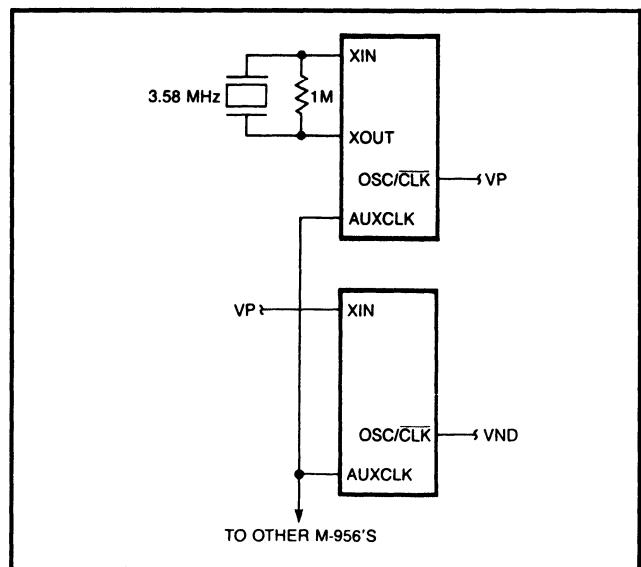
Figure 6 Use of a Common Clock

Table 3 Absolute Maximum Ratings (Note 1)

DC Supply Voltage (Note 2).	7.0 V
Voltage on SIGNAL IN.	(VP + 0.5 V) to (VND − 22 V)
Voltage on Any Pin Except SIGNAL IN.	(VP + 0.5 V) to (VND − 0.5 V)
Storage Temperature Range.	−40° to 85° C
Operating Temperature Range.	0° to 70° C
Lead Soldering Temperature.	260° C for 5 seconds

Notes:

1. Exceeding these ratings may permanently damage the M-956.

2. VP referenced to VND. VND should be at equal potential to VNA. VND/VNA may be at ground.
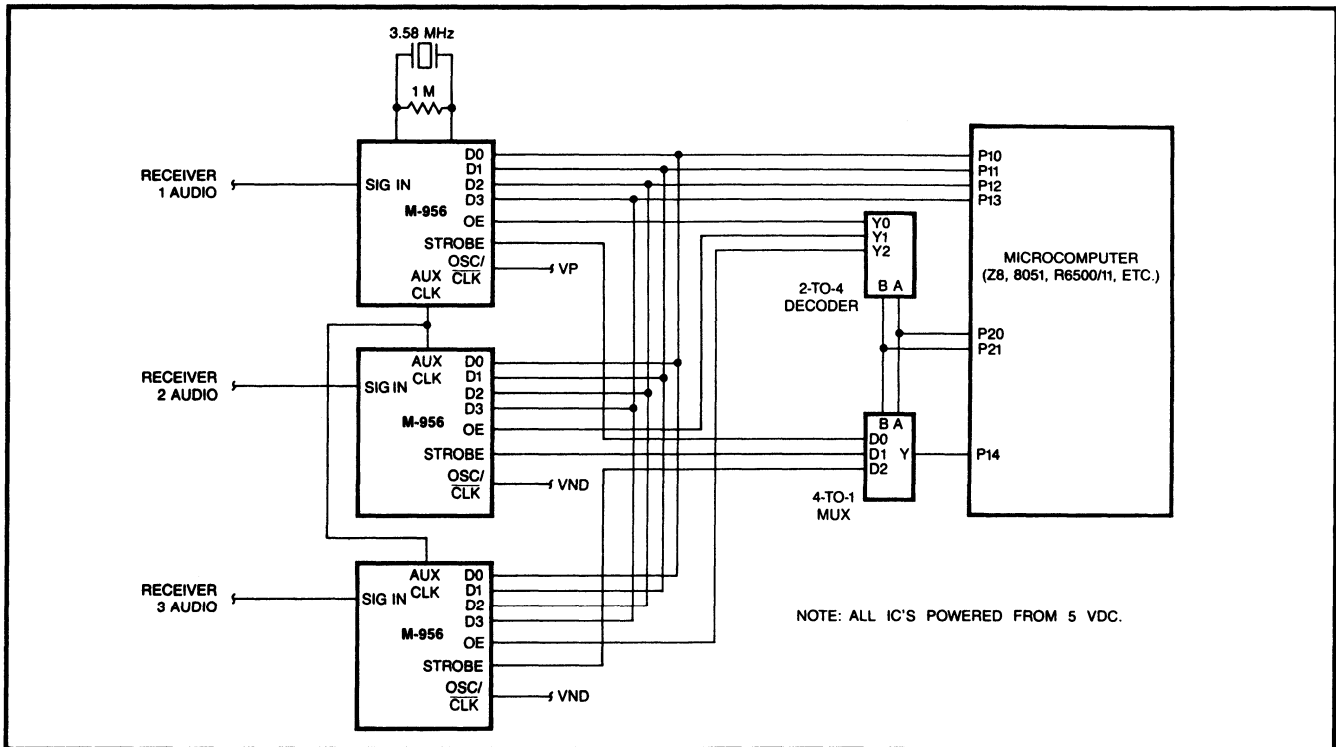
Figure 7 Multiple Receiver/Microprocessor Interface
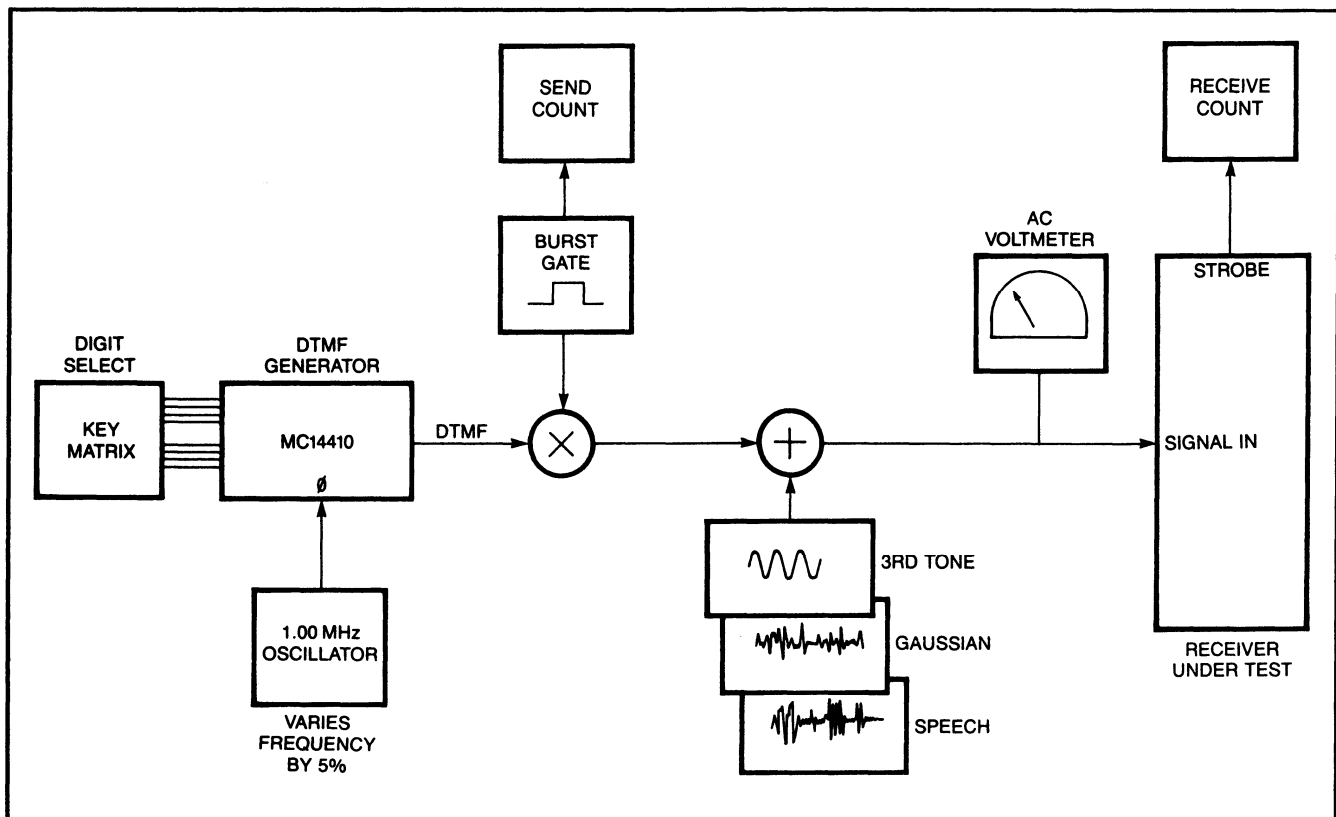
Figure 8 Test Circuit

Table 4 Specifications

	Parameter	Conditions	Min	Typ	Max	Units	Notes
SIGNAL IN Input Requirements	Signal Level (per tone)	—	−27	—	0	dBm	1
	Signal Duration	—	40	30	—	ms	
	Interval Between Signals	—	40	35	—	ms	
	Signal Present Without Detection	—	—	—	20	ms	
	Interruption of Signal Without Redetection	—	—	—	20	ms	
	Signal Frequency Deviation With Detection	—	—	$\pm 2.5\%$	$\pm(1.5\% + 2)$	Hz	
	Signal Frequency Deviation Without Detection	—	$\pm 3.5\%$	$\pm 3.0\%$	—	Hz	
	Twist	—	—	—	± 10	dB	2
	Gaussian Noise	—	—	12	A−7	dB	3
	Dial Tone Level (per tone, F ≤ 480 Hz)	—	—	—	A+0	dB	4
Digital Input Requirements	Logic 0 Voltage	—	0	—	1.5	V	5
	Logic 1 Voltage	—	3.5	—	5.0	V	5
Digital Output Characteristics	Logic 0 Voltage	$I_O = 1$ mA	0	—	0.5	V	5
	Logic 1 Voltage	$I_O = -1$ mA	4.5	—	5.0	V	5
Miscellaneous Characteristics	Power Dissipation	—	—	0.04	1.0	W	6
	SIGNAL IN Input Impedance	F = 1 kHz, paralleled with 15 pF	100k	—	—	ohms	
Power Requirements	Supply Current	VP − VND = 5 V ± 10% VP − VNA = 5 V ± 10%	—	8	18	mA	
	Power Supply Wide Band Noise (A = 0, B = 0)	VP − VND = 5 V VP − VNA = 5 V	—	—	10	mVpp	

Notes:

1. With a 5-volt power supply, an ambient temperature of 25° C, the signal duration and signal interval at minimum, and the signal frequency deviation and twist at maximum. The unit "dBm" refers to decibels above or below a reference power of one milliwatt into a 600-ohm load. (For example, −24 dBm equals 49 mVrms.)

2. Twist is defined as the ratio of the level of the high-frequency DTMF component to the level of the low-frequency DTMF component.

3. With a 5-volt power supply, an ambient temperature of 25° C, the signal level at A + 5, the signal frequency deviation and twist at 0, and the signal applied 50 ms off and 50 ms on. The A level is the minimum detect level selected.

4. With the signal duration and signal interval at minimum, and the signal frequency deviation and twist at maximum. The A level is the minimum detect level selected.

5. Logic levels are shown for a supply voltage (VP − VND) of 5 V, and are referenced to VND.

6. For a 5-volt power supply and an ambient temperature of 25° C.
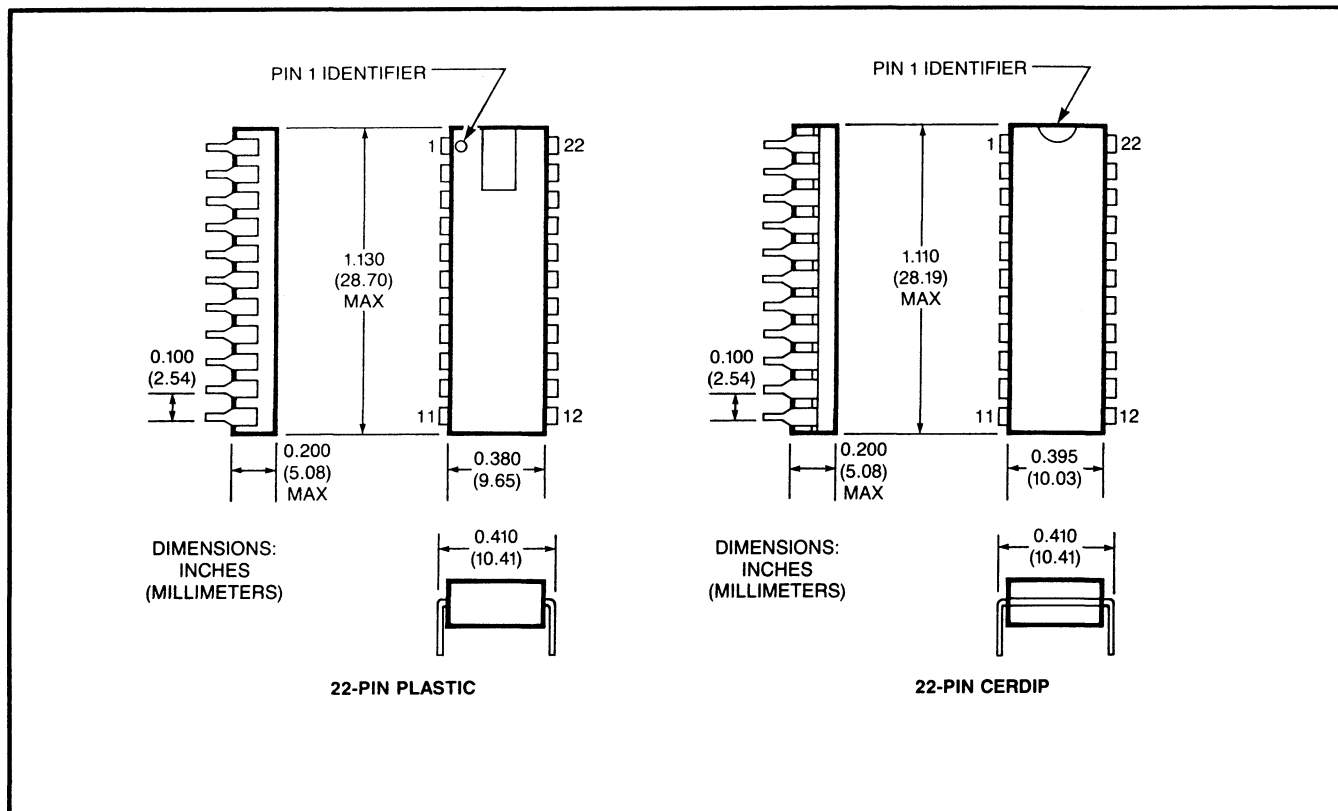
Figure 9 Package Dimensions

M-967 DTMF RECEIVER

The Teltone® M-967 tone and rotary dial decoder IC is an LSI implementation of the circuitry needed to form the heart of a DTMF or rotary dial receiver circuit. When combined with filters for separation of the dual tones, the M-967 will provide high-quality detection of DTMF signals.

The crystal-controlled time base in the M-967 accurately measures the frequencies of the tone signals, provides precise supervision of telephone hook status, and validates dial pulse digits with digital repeatability. When the decoder has validated a signal, the information is presented along with a strobe in binary. The outputs can be blanked, and separate pins are provided for * and # detection.

To operate, the M-967 requires a single 12-volt DC supply and an 895-kHz crystal or clock input (895 kHz = 3.58 MHz/4).

Features
- Decodes all 16 DTMF signals
- Contains timing and counting circuitry for loop hook status and 10 pps dial pulse decoding
- Tone-only, or mixed mode operation
- Selectable output formats

- Two inputs with hysteresis for accepting the output of a DTMF bandsplit filter
- Meets or exceeds common foreign and domestic telephone central office requirements for DTMF recognition and speech immunity
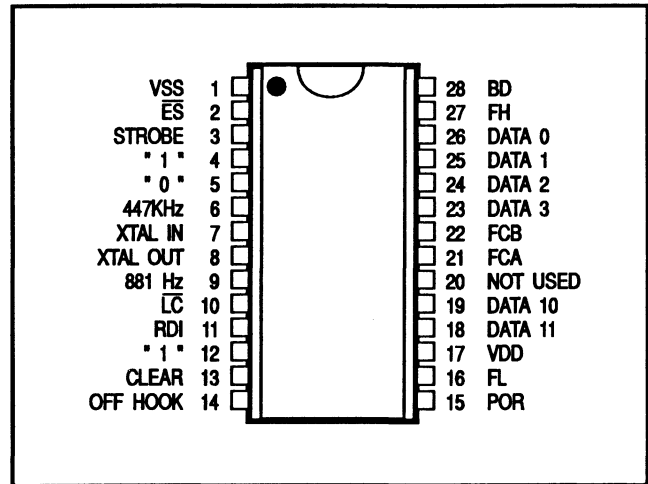
Figure 1 Pin Diagram
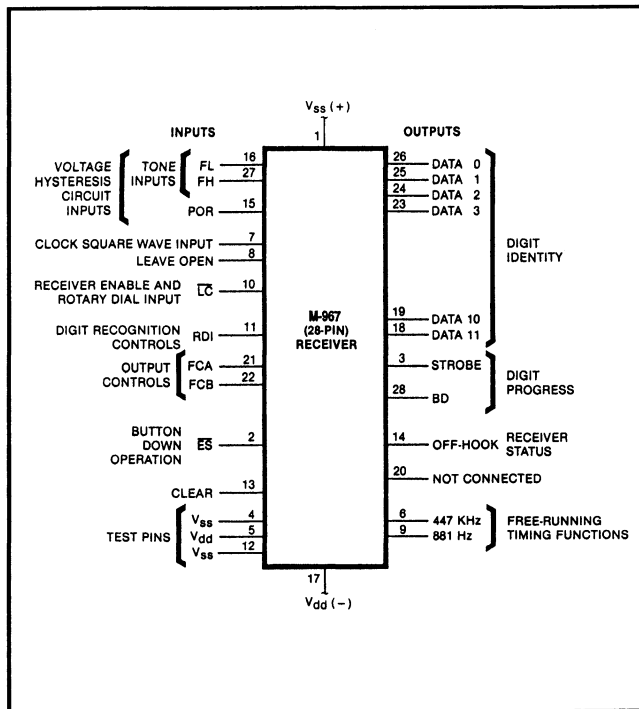
Figure 2 Receiver Configuration
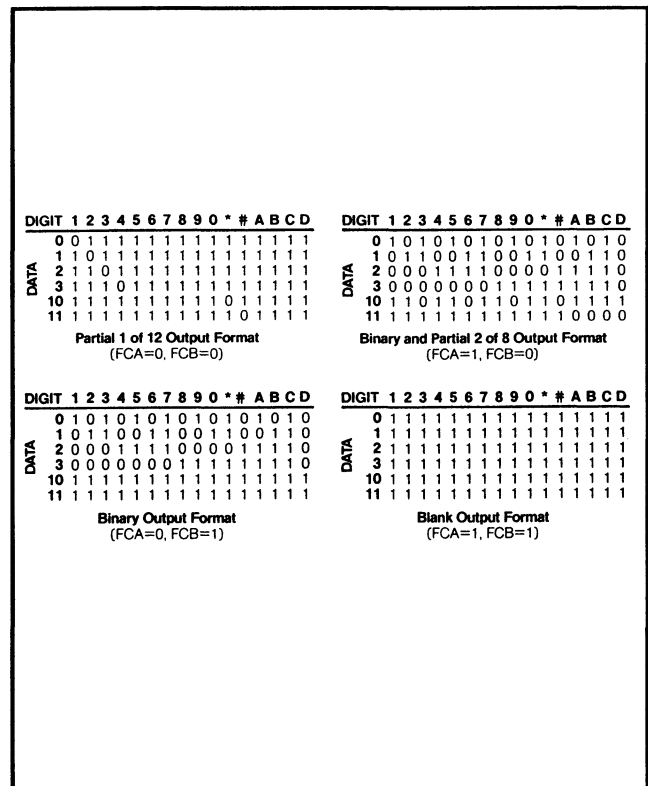
Figure 3 Output Formats
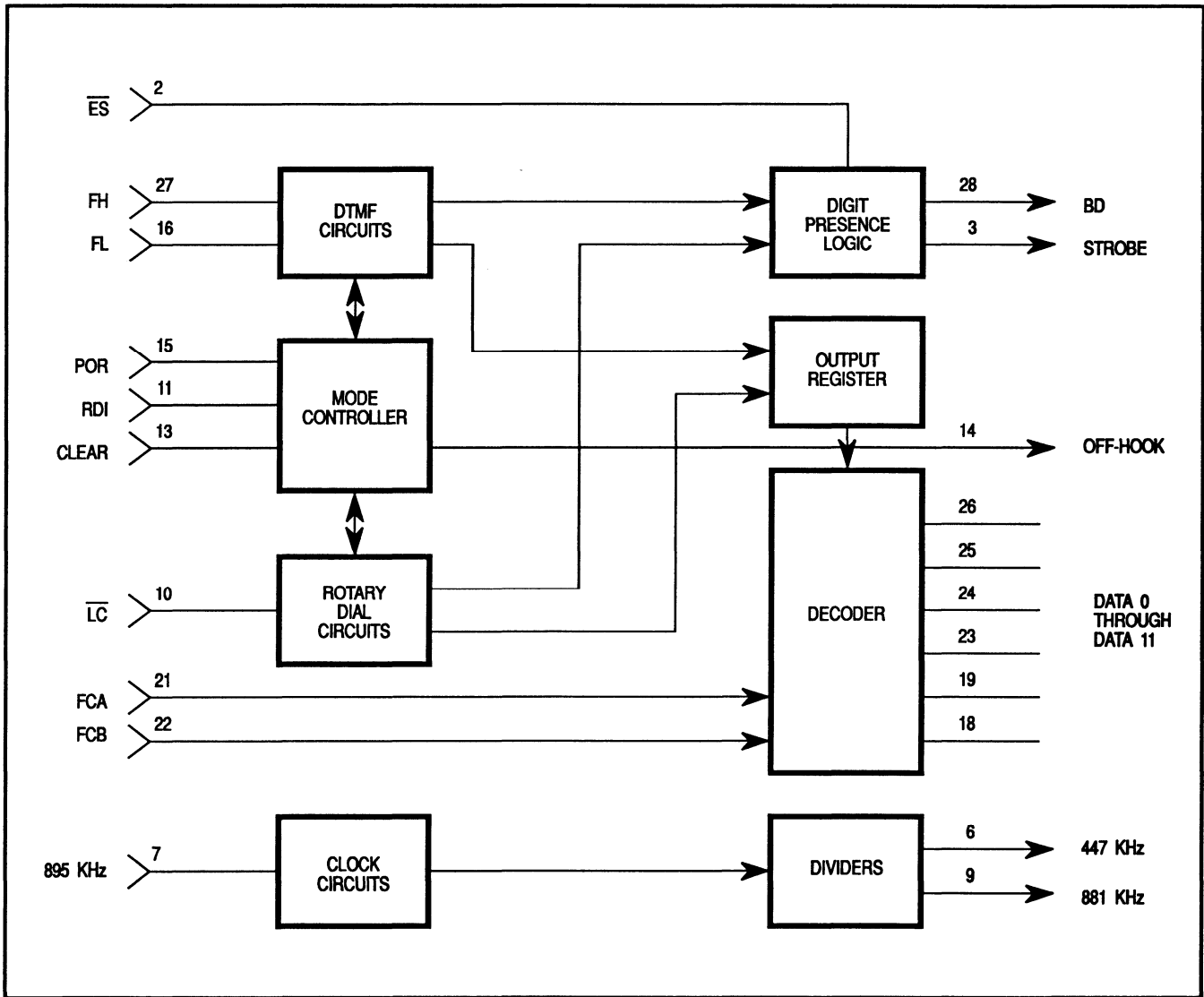
Figure 4 Block Diagram

Table 1 Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2) . . . . .14.5 V
Power Dissipation . . . . .600 mW
Voltage on Any Pin . . . . $(V_2 + 0.3\text{ V})$ to $(V_1 - 0.3\text{ V})$
Storage Temperature . . . . $-40°$ to $150°$ C
Operating Temperature . . . . $0°$ to $70°$ C ambient air
Lead Soldering Temperature . . . . $260°$ C for 5 seconds at 0.035 inches from package

Notes:
1. Exceeding these ratings may cause permanent damage.
2. V_2 (positive supply) referenced to V_1 (negative supply). V_2 may be at ground.

Table 2 Pin Functions		
Pin Number	Function	Description
1	V$_{SS}$	Positive power supply (V$_2$)
2	$\overline{ES}$	Early split not input. When pulled to logic 0 (V$_1$), $\overline{ES}$ enables the early tone presence (BD) output.
3	STROBE	Valid data output. When DTMF digits are being detected, STROBE goes to the logic 1 state 10 microseconds after the DATA outputs change and returns to the logic 0 state 25 milliseconds (ms) after the end of DTMF detection. When rotary dial digits are being detected, STROBE goes to logic 1 for 200 ms after the interdigital pause is recognized. To read DATA during DTMF signal presence, use the leading edge of STROBE (button-down operation). To read DATA after DTMF signal presence, use the trailing edge of STROBE (button-up operation).
4		Test input. Connect to logic 1.
5		Test input. Connect to logic 0.
6	447 kHz	50 percent duty cycle. PMOS logic level signal for external use. Actual frequency is the clock frequency divided by 2.
7	CLOCK IN	895-kHz input from the filter.
8	XTAL OUT	Not used. Leave open.
9	881 Hz	50 percent duty cycle. PMOS logic level signal for external use. Actual frequency is the clock frequency divided by 1016.
10	$\overline{LC}$	Loop current not input. $\overline{LC}$ is both a receiver enable/disable input and the rotary dial pulse input. The M-967 interprets a logic 0 as an off-hook condition, interdigital pause, or a make period. The M-967 interprets a logic 1 as an on-hook condition or break period. For DTMF operation only, LC can be connected to V$_1$; then, with POR connected as described below, the receiver is enabled as long as CLEAR is at logic 0.
11	RDI	Rotary dial inhibit input. For mixed DTMF and rotary dial operation, connect RDI to logic 0. For DTMF operation only, connect RDI to logic 1.
12		Test input. Connect to logic 1.
13	CLEAR	Receiver enable/disable input. A logic 1 applied to the CLEAR input instantaneously resets all detection circuits and forces the DATA outputs to the D column of the currently enabled output format (see Figure 3).
14	OFF-HOOK	Output OFF-HOOK goes to the logic 1 state 100 ms after $\overline{LC}$ is pulled to logic 0. OFF-HOOK goes to the logic 0 state 300 ms after LC is pulled to logic 1.
15	POR	Power-on reset, receiver enable/disable input. A 0.01 μf capacitor connected to V$_2$ and POR causes POROUT to go to logic 1 (V$_2$) for approximately 10 ms after power is applied. This pulse resets all detection circuits and forces the DATA outputs to the D column of the currently enabled output format (see Figure 3).
16	FL	FLSQ input from the filter.
17	V$_{dd}$	Negative power supply (V$_1$).
18	DATA 11	Data outputs. See Figure 3 for the outputs associated with each output format. A DTMF digit is output when it has persisted for 35 ms. A rotary dial digit is output when an interdigital pause is recognized.
19	DATA 10	
20		Not used.
21 and 22	FCA and FCB	Format control A and B inputs. As shown in Figure 3, FCA and FCB determine the DATA output format. FCA and FCB can also be used as a data strobe. By holding both inputs at logic 1, all data outputs will remain at logic 1 until FCA and/or FCB are poulled to logic 0.
23	DATA 3	See description to DATA 10 and 11.
24	DATA 2	
25	DATA 1	
26	DATA 0	
27	FH	FHSQ input from the filter.
28	BD	Button down output. When enabled by $\overline{ES}$ being at logic 0, BD goes to the logic 1 state within 16 ms after a tone pair is detected. BD then returns to the logic 0 state 25 ms after the tone pair ends.

1. TO TTL OR CMOS AT A LOWER SUPPLY VOLTAGE

2. TO LOW POWER SCHOTTKY TTL

3. TO RELAYS OR DISPLAYS (NEGATIVE SUPPLY)

4. TO TRANSISTOR DRIVERS

5. (NOT SHOWN) TO CMOS AT THE SAME SUPPLY VOLTAGE—INTERFACE DIRECTLY (ALL OUTPUTS)

Figure 5 Output Interface Techniques

Table 3 DC Electrical Characteristics

	Parameter	Min	Typ	Max	Units	Conditions
Supply Requirements	Supply Voltage	+11	+12	+14.5	V	V_2 referenced to V_1 (Note 1)
	Ripple Voltage			250	mV	Measured peak-to-peak at 120 Hz
	Supply Current		25	35	mA	14.5 V at 0°C
Logic Inputs	Logic 0 Level			$V_1 + 3.2$	V	
	Logic 1 Level	$V_2 - 2.5$			V	
	Capacitance			15	pF	
	Input Current (Note 2)			50	μA	
Analog Inputs	Logic 0 Threshold	0.57 (ΔV)	0.65 (ΔV)	0.73 (ΔV)	V	$\Delta V = V_2 - V_1$
	Logic 1 Threshold	0.43 (ΔV)	0.35 (ΔV)	0.27 (ΔV)	V	$\Delta V = V_2 - V_1$
	Capacitance			15	pF	
	Input Current (Note 2)			±50	μA	
Data Outputs	Logic 0 Current Sink			1	mA	Output at $V_1 + 7$ V
	Logic 1 Current Source			100	μA	Output at $V_2 - 2$ V
Non-Data Outputs	Logic 0 Current Sink			100	μA	Output at $V_1 + 2$ V
	Logic 1 Current Source			100	μA	Output at $V_2 - 2$ V

Notes:
1. V_2 more positive than V_1. V_2 may be at ground.
2. The load current must be sourced or sunk to drive an input to its opposite state.

Table 4 AC (Dynamic) Electrical Characteristics

	Parameter	Min	Typ	Max	Units	Conditions
FL and FH Inputs	Signal Detect Time	27		30	ms	
	Interdigital Pause Detect Time (Note 1)	26		34	ms	
	Interdigital Pause Reject Time (Note 1)	26			ms	
	Signal Detect Bandwidth	−1.5% −2 Hz		+1.5% +2 Hz	Hz	Of each nominal DTMF frequency
	Signal Reject Bandwidth	−3.5%		+3.5%	Hz	Of each nominal DTMF frequency
Inputs Other Than FL and FH	Pulse Width Required to Reset with CLEAR or POR Inputs			25	μs	
	Off-Hook Recognition	95	100	105	ms	$\overline{LC}$ at Logic 0
	Off-Hook Blanking (Note 2)	285	300	315	ms	$\overline{LC}$ at Logic 0
	Break Recognition	24.5		29.5	ms	$\overline{LC}$ at Logic 1
	Make Recognition	7	9	11	ms	$\overline{LC}$ at Logic 0
	End of Digit Recognition	95	100	105	ms	$\overline{LC}$ at Logic 0
	Rotary Interdigital Blanking	190	200	210	ms	
	On-Hook Recognition	290	300	310	ms	$\overline{LC}$ at Logic 1
Available Frequencies	447.433 kHz Pulse Width	2.232	2.234	2.237	μs	
	881 Hz Pulse Width	0.567	0.568	0.569	ms	
	20 Hz Pulse Width (Note 3)	24.95	24.98	25	ms	

Notes:
1. The Interdigital Pause Detect Time is that interval of loss of tones after which the return of the valid tone pair is considered a new digit. The Interdigital Pause Reject Time is the interval a valid tone pair can be interrupted without being treated as a new digit when it returns.
2. Off-Hook Blanking is the delay between $\overline{LC}$ going to logic 0, from being at logic 1 longer than 300 ms, and enabling the digit detection circuits.
3. 40-pin receivers only.

Figure 6 Timing Diagram

TIMES SHOWN ARE TYPICAL
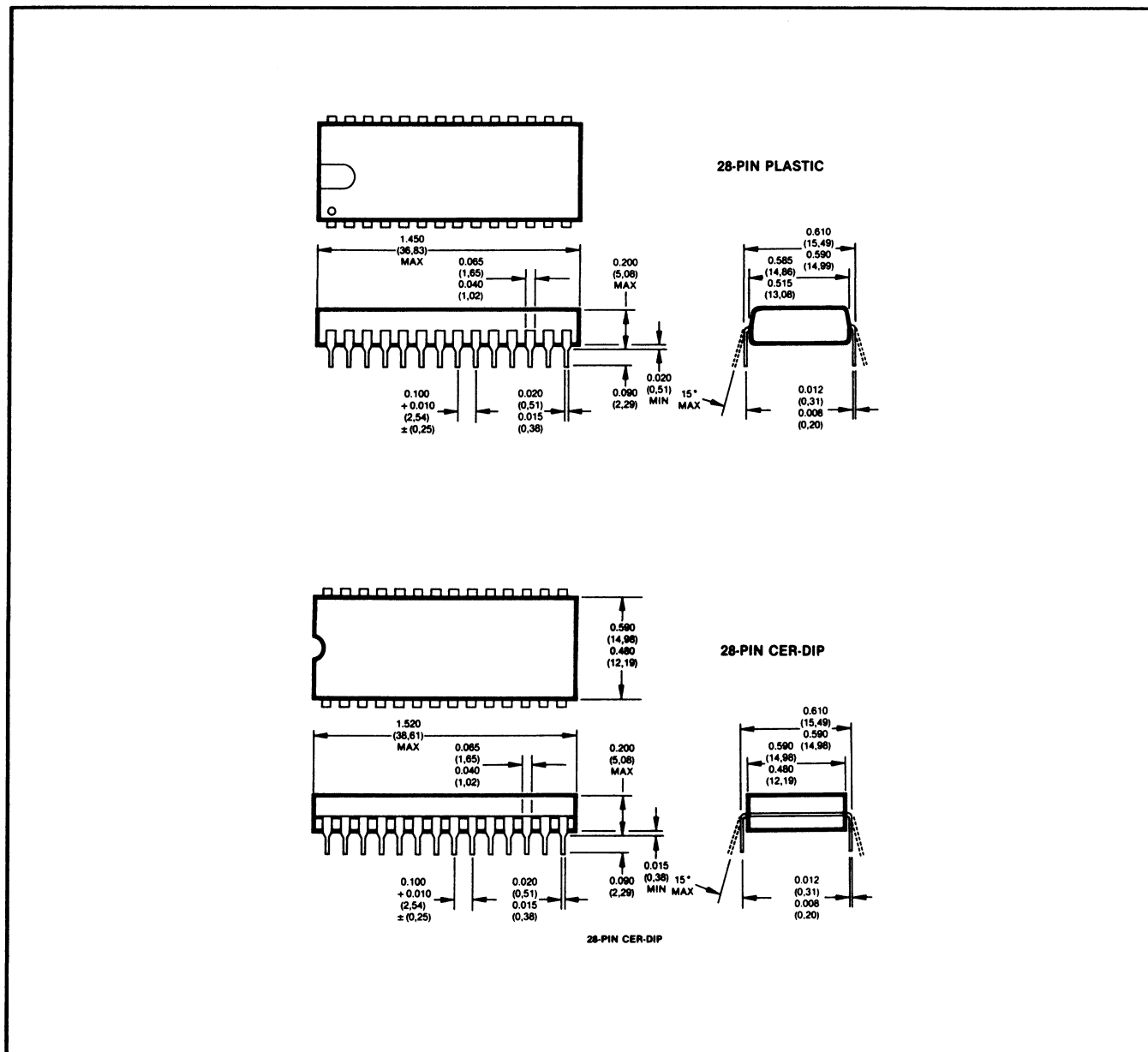
Figure 7 Package Dimensions

M-985 R1 MULTIFREQUENCY RECEIVER

The Teltone® M-985 MF Receiver is a single circuit board designed to provide high-performance detection of multitone trunk address signaling in accordance with U.S. and international standards. The M-985 is easily mounted using plastic standoffs and mates with 0.25-inch-square pins on the mother board. Overall height above the mother board is kept to 0.75 inches.

Features

- Detects multifrequency tone signals containing frequencies 700, 900, 1100, 1300, 1500, and 1700 Hz
- Compatible with North Americn MF standards and with CCITT R1 MF recommendations
- High-impedance balanced differential input (AC coupled)
- Single 12-VDC supply

Figure 1 Pin Diagram

Table 1 Pin Functions

Figure 2 Block Diagram
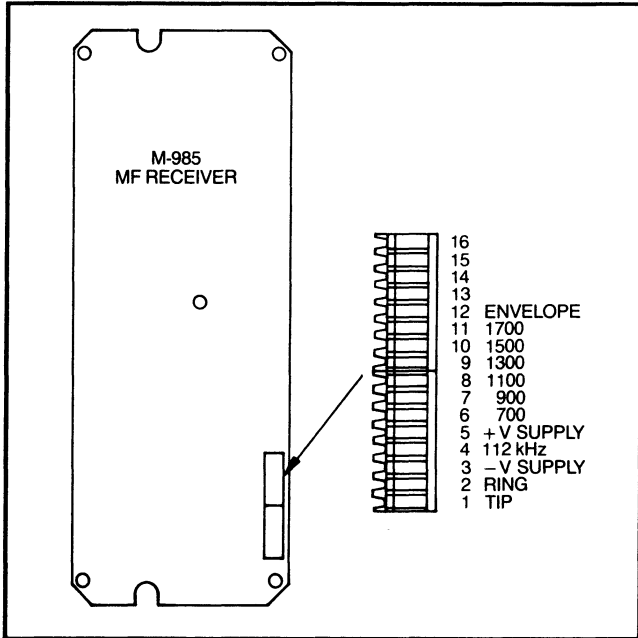
Pin	Function
112 kHz	Input (3.58 MHz/32)
TIP	MF signal input balanced to Ring
RING	MF signal input balanced to Tip
+V	Positive supply voltage input
−V	Negative supply voltage (ground) input
700	Active low detect output for 700 Hz
900	Active low detect output for 900 Hz
1100	Active low detect output for 1100 Hz
1300	Active low detect output for 1300 Hz
1500	Active low detect output for 1500 Hz
1700	Active low detect output for 1700 Hz
ENVELOPE	Active low output when input signal is present

Figure 3 Timing Diagram

Five mounting holes (0.156 inch diameter)
Sixteen electrical connectors (require 0.025 inch diameter pin)

PIN 1

2.000
(50.80)

0.025
(0.63)

3.000
(76.20)

3.300
(83.82)

1.200
(30.48)

0.400
(10.16)

0.100
(2.54)

3.775
(95.89)

0.350
(8.89)

8.000
(203.20)

0.150
(3.81)

DIMENSIONS:
INCHES
(MILLIMETERS)

0.500
(12.70)
MAX

8.700
(220.98)

M-985 RECEPTACLE

PLASTIC SPACER
MOTHER BOARD

0.750
(19.05)
MAX
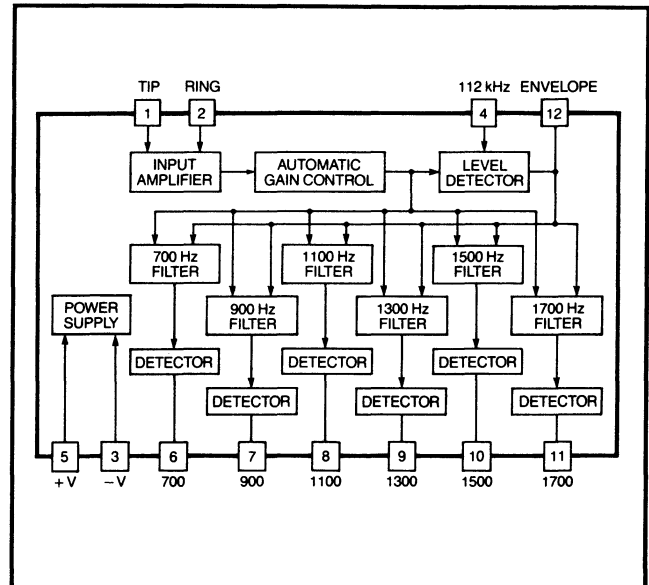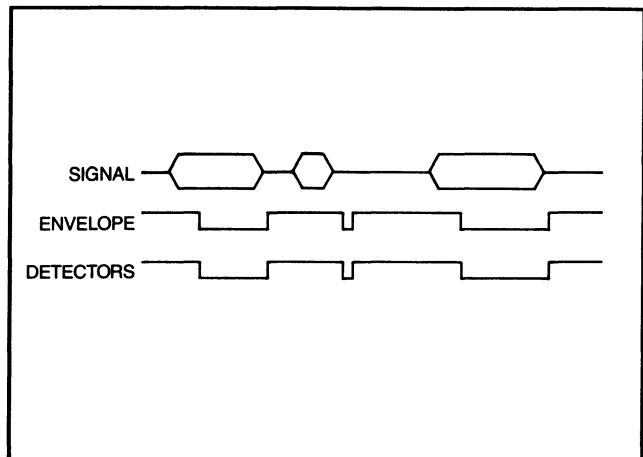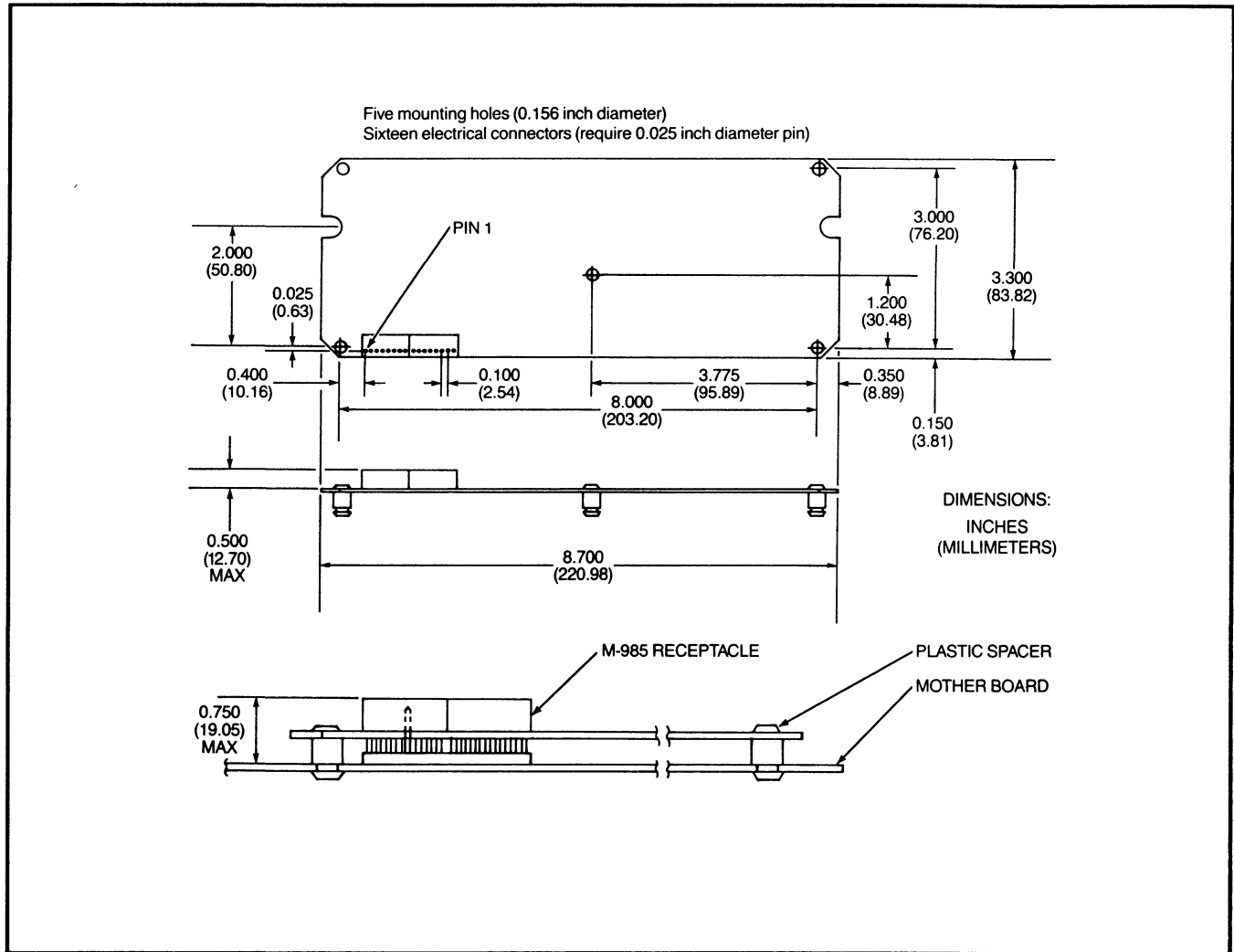
Figure 4 Package Dimensions

Table 3 Specifications

| Parameter	Min	Max	Units	Remark
Signal Level	−25	0	dBm	600 ohms
Signal Duration	27		ms	
Signal Interval Duration	20		ms	
Signal Frequency Offset		1.5	%	
Twist (Level Skew)		6	dB	
Input Impedance	75		kohm	
Tone Present Output	1.0	3.0	volt	$R_L \geq 10$ kilohms
Tone Absent Output	9.0	11.0	volt	$R_L \geq 10$ kilohms
Supply Current		100	mA	
Supply Voltage	10.8	13.2	volts	

M-987 R2B MULTIFREQUENCY RECEIVER

The Teltone® M-987 MF Receiver is a single circuit board designed to provide high-performance detection of multitone trunk address signaling in accordance with international standards. The M-987 is easily mounted using plastic standoffs and mates with 0.25-inch-square pins on the mother board. Overall height above the mother board is kept to 0.75 inches.

Features

- Detects multifrequency tone signals containing frequencies 1380, 1500, 1620, 1740, 1860, and 1980 Hz
- Compatible with CCITT R2 MF recommendations
- High-impedance balanced differential input (AC coupled)
- Single 12-VDC supply

Figure 1 Pin Diagram

Table 1 Pin Functions

Figure 2 Block Diagram
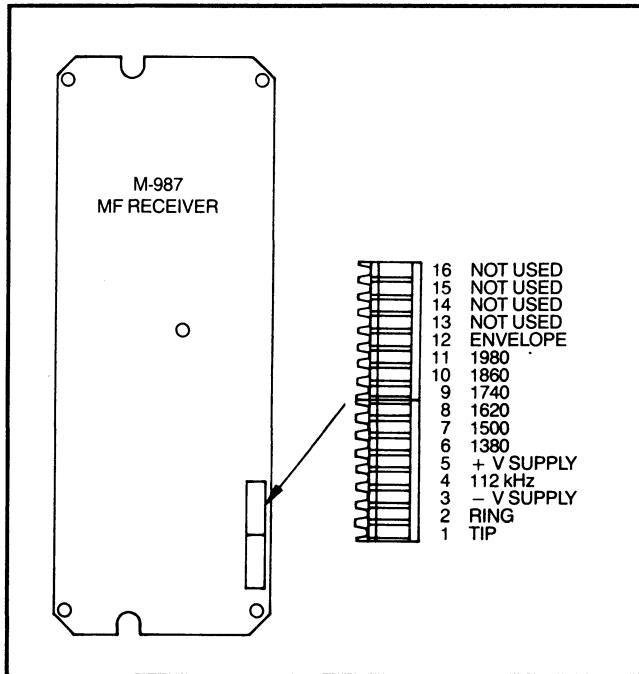
Pin	Function
112 kHz	Input (3.58 MHz/32)
TIP	MF signal input balanced to Ring
RING	MF signal input balanced to Tip
+ V	Positive supply voltage input
− V	Negative supply voltage (ground) input
1980	Active low detect output for 1980 Hz
1860	Active low detect output for 1860 Hz
1740	Active low detect output for 1740 Hz
1620	Active low detect output for 1620 Hz
1500	Active low detect output for 1500 Hz
1380	Active low detect output for 1380 Hz
ENVELOPE	Active low output when input signal is present

Figure 3 Timing Diagram

Five mounting holes (0.156 inch diameter)
Sixteen electrical connectors (require 0.025 inch diameter pin)

PIN 1

2.000
(50.80)

0.025
(0.63)

0.400
(10.16)

0.100
(2.54)

8.000
(203.20)

3.775
(95.89)

3.000
(76.20)

3.300
(83.82)

1.200
(30.48)

0.350
(8.89)

0.150
(3.81)

DIMENSIONS:
INCHES
(MILLIMETERS)

0.500
(12.70)
MAX

8.700
(220.98)

M-987 RECEPTACLE

PLASTIC SPACER
MOTHER BOARD

0.750
(19.05)
MAX
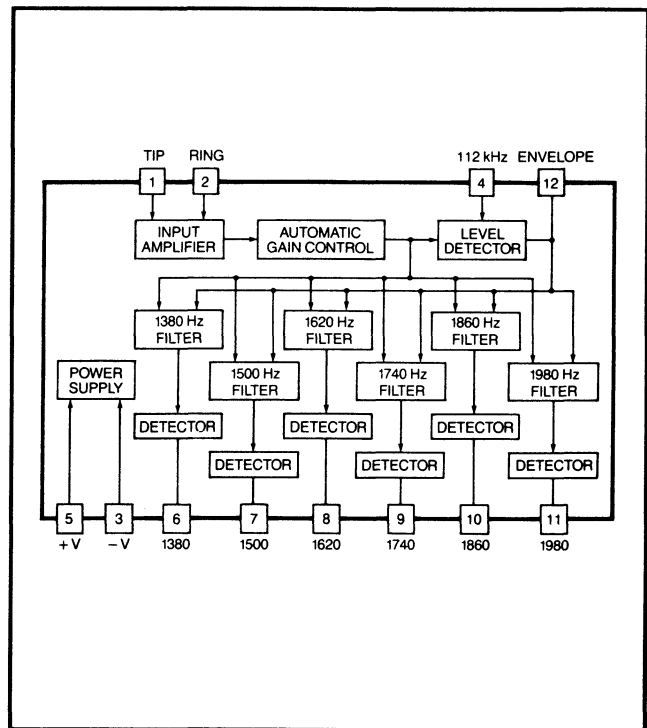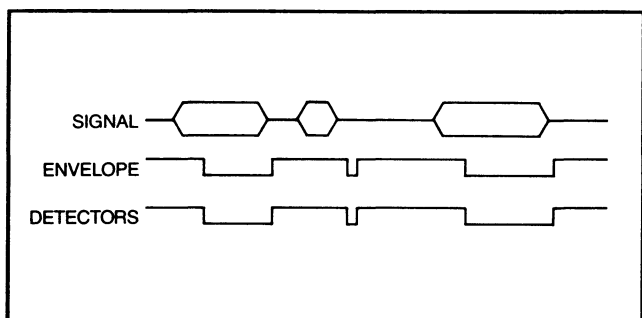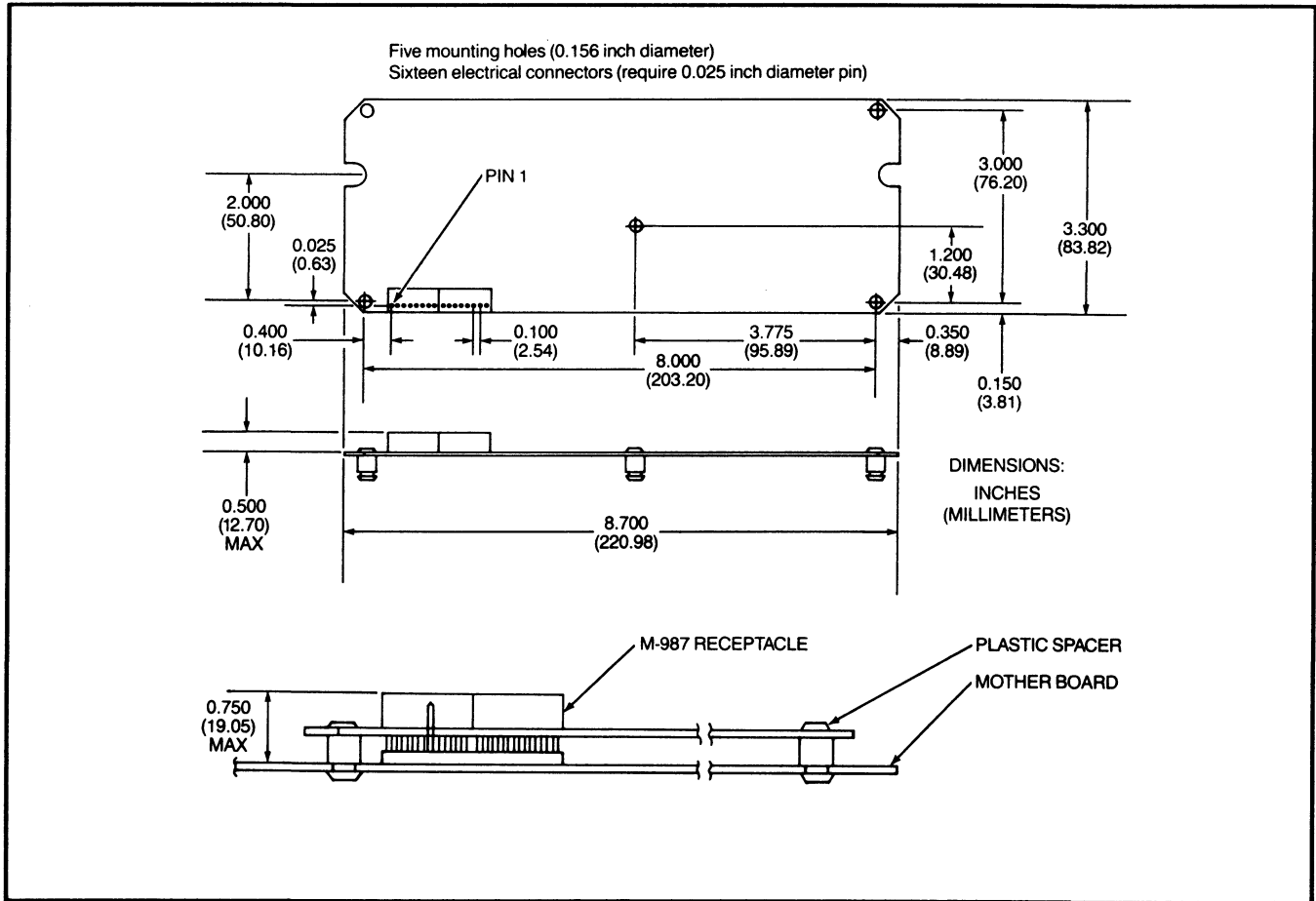
Figure 4 Package Dimensions

Table 2 Specifications

Parameter	Min	Max	Units	Remark
Signal Level	−35	−5	dBm/freq.	600 ohms
Operation Time plus Release Time		80	ms	
112 kHz Duty Cycle	45	55	%	
112 kHz Low Voltage	0	2	volts	V supply = 12.0
112 kHz High Voltage	10	12	volts	V supply = 12.0
Signal Frequency Offset	−10	+10	Hz	
Twist (Level Skew)		7	dB	non-adjacent freq.
		5	dB	adjacent freq.
Input Impedance	75		kohm	
Tone Present Output	0.0	3.0	volts	V supply = 12.0
Tone Absent Output	9.0	12.0	volts	V supply = 12.0
Supply Current		100	mA	
Supply Voltage	10.8	13.2	volts	

M-988 MULTIFREQUENCY RECEIVER

The Teltone® M-988 Multifrequency Receiver is a high-quality circuit module intended for use in detection of trunk signals as outlined in AT&T and Bellcore MF Standards, and in CCITT recommendations for System R1 and Signaling System Number 5.

Using advanced circuit integration techniques, the M-988 provides the high performance demanded of such devices—in a compact form. The power consumption of the M-988 is less than half that of similar devices.

Features
- Meets Bellcore, AT&T, and CCITT standards
- 2-of-6 outputs
- ±5 volt supply, low power
- Tone error indicator
- Gain adjustment with external resistor
- Compact package

Figure 1 Pin Diagram

Pin assignments:
- -5V 1, 50
- 2, 49
- 3, 48
- 4, 47
- 5, 46
- GND 6, 45
- 7, 44
- D6 1700 Hz 8, 43
- D5 1500 Hz 9, 42
- D4 1300 Hz 10, 41
- DE 11, 40
- DV 12, 39 NO CONNECTIONS THIS SIDE
- D3 1100 Hz 13, 38
- D2 900 Hz 14, 37
- D1 700 Hz 15, 36
- 16, 35
- 17, 34
- 18, 33
- GI 19, 32
- GII 20, 31
- GIII 21, 30
- INH 22, 29
- INL 23, 28
- 24, 27
- +5V 25, 26

" - " MEANS NO CONNECTION
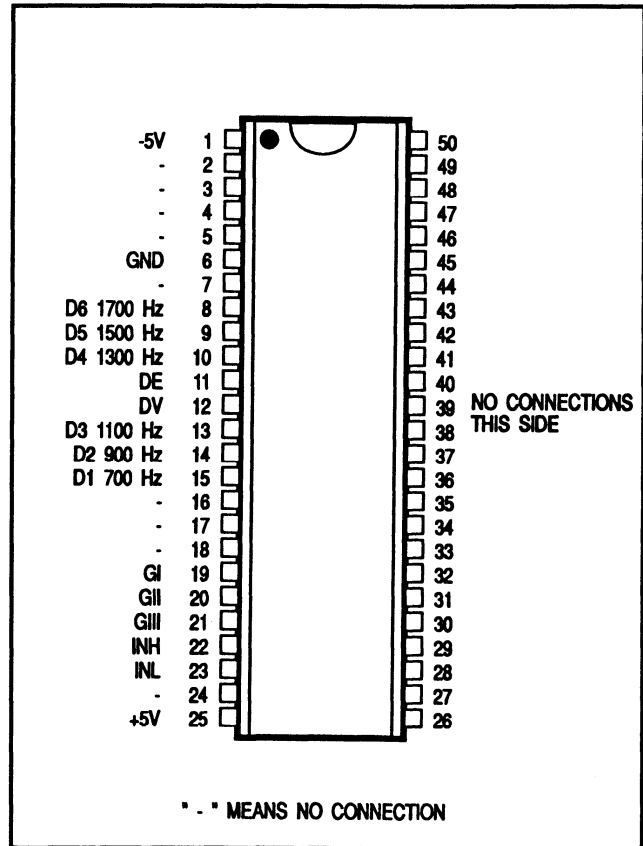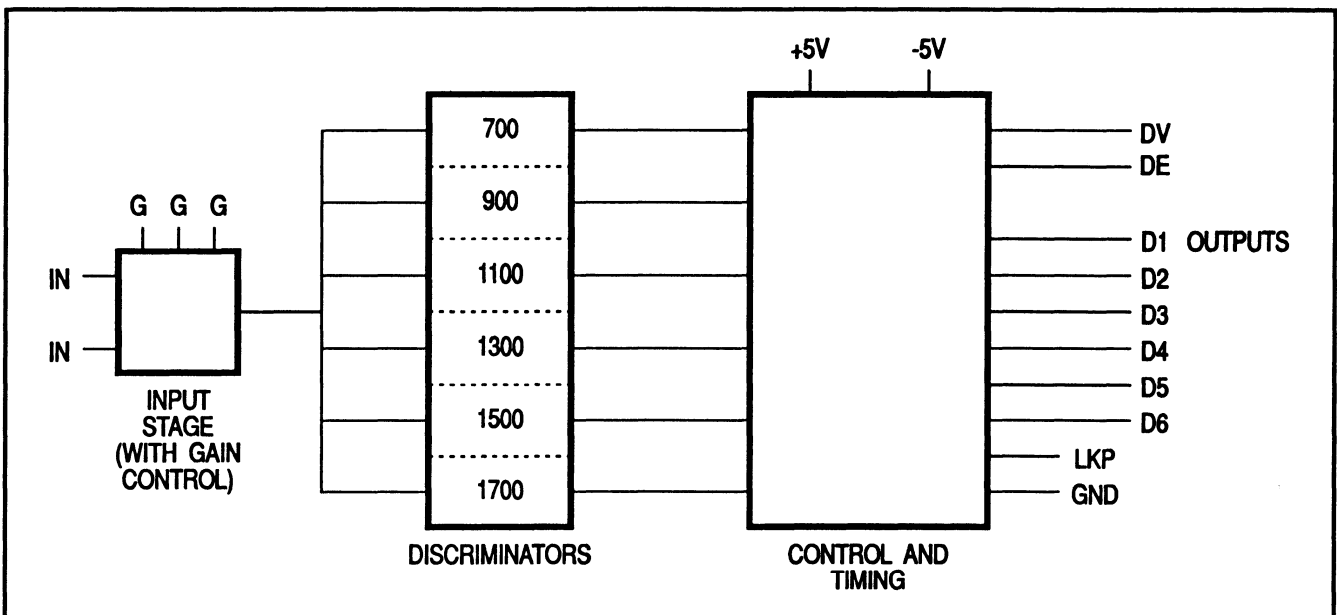
Figure 2 Block Diagram

Table 1 Specifications

Parameter	Min	Max	Units	Notes
Receive frequency tolerance	±(1.5% + 5 Hz)			
Detect level	-34	-5	dBm	600 ohm
Not-detect level		-43	dBm	
Detect time (all sigs)	30		ms	Pin 27 open or at ground
Detect time (KP only)	55		ms	Pin 27 at +5 V
Tone burst mask timing		10	ms	
Interval detect timing	20		ms	
Interval mask timing		10	ms	
C-message S/N ratio	20		dB	
Power consumption		25	mA	Nominal V
Operating temeperature	0	+70	°C	Ambient
Output drive	1		mA	0.5 V off either rail
Dimensions: 2.25 x 2.65 x 0.5 inches maximum (57 x 67 x 12.7 mm)				

Table 2 Timing Specifications

Parameter		Symbol	Min.	Max.	Units
Tone time, KP (LKP = V_{DD})	detect	T_{on}	55	—	ms
	reject	T_{on}		30	ms
Tone time, KP (LKP = D_{GND})	detect	T_{on}	30	—	ms
	reject	T_{on}		10	ms
Tone time, all others	detect	T_{on}	30	—	ms
	reject	T_{on}	—	10	ms
Pause time	detect	T_{pse}	20	—	ms
	reject	T_{br}	—	10	ms
Data setup time		T_{su}	6	—	µs
Data hold time		T_H	7	—	µs
Tone skew tolerance		Tskew	—	4	ms
Strobe pulse width		—	20	—	ms
Strobe separation		—	20	—	ms
Rise time DV, DE, D0-D5, 10-90%	CL = 20 pF	T_r	—	100	ns
Fall time DV, DE, D0-D5, 10-90%	CL = 20 pF	T_f	—	100	ns
Data enable time	CL = 20 pF	T_{en}	—	100	ns
Data disable time		T_{dis}	—	100	ns
Strobe reset time	CL = 20 pF	T_{rst}	—	100	ns

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7-70
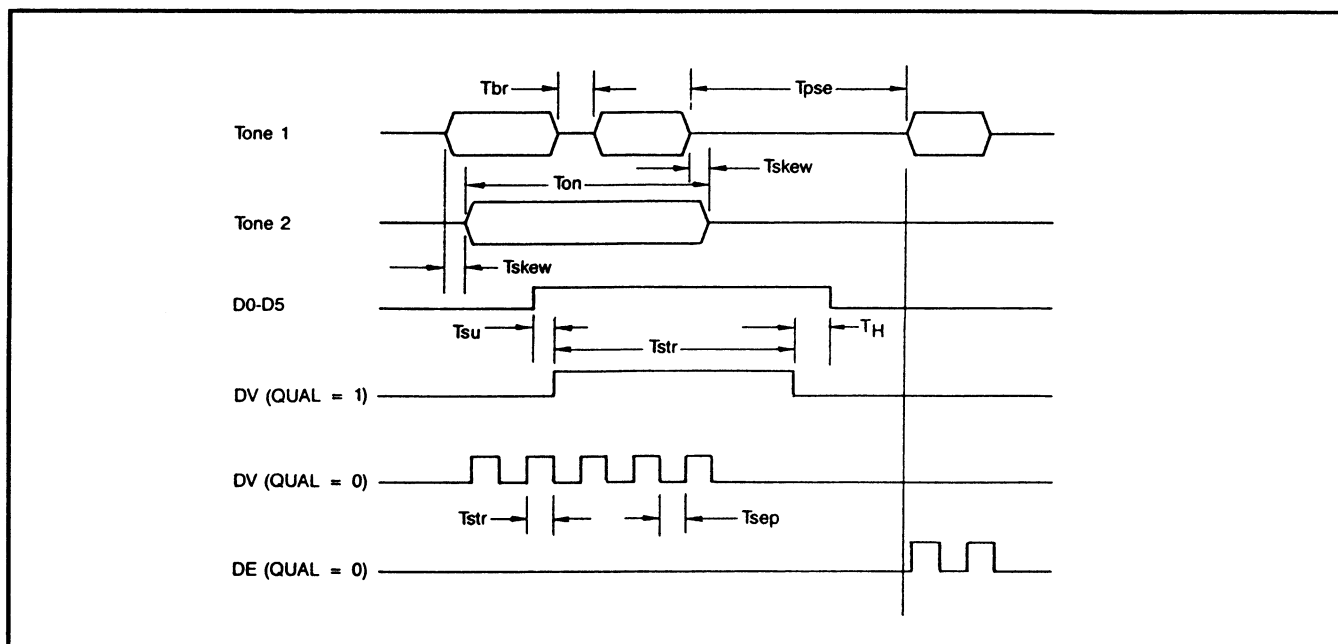
Figure 3 Timing Diagram

Table 3 M-988 Sensitivity Data			
GI to GII	**+dB**	**GII to GIII**	**-dB**
51K	1.5	51K	-1.5
36K	2.1	36K	-2.1
27K	2.7	27K	-2.7
20K	3.5	20K	-3.5
15K	4.4	15K	-4.4
10K	6	10K	-6

Notes:

1. Power requirement: Total 25 mA max, -5 Volt 7 mA max.

2. Tip and Ring: Tip to INH, Ring to INL, differential amplifier inputs are capacitivity coupled.

3. Strobe pins DV and DE: Valid data is indicated on the DV strobe pin, and data errors are indicated on the DE strobe pin. Whenever a valid 2 of 6 code has been detected, the DV strobe rises and remains high until the code stops. When an invalid code is detected, e.g., 1 of 6, 3 of 6, etc., the DE strobe remains high until all errors stop or a valid tone pair is detected. The DV and DE strobes will never be high simultaneously.
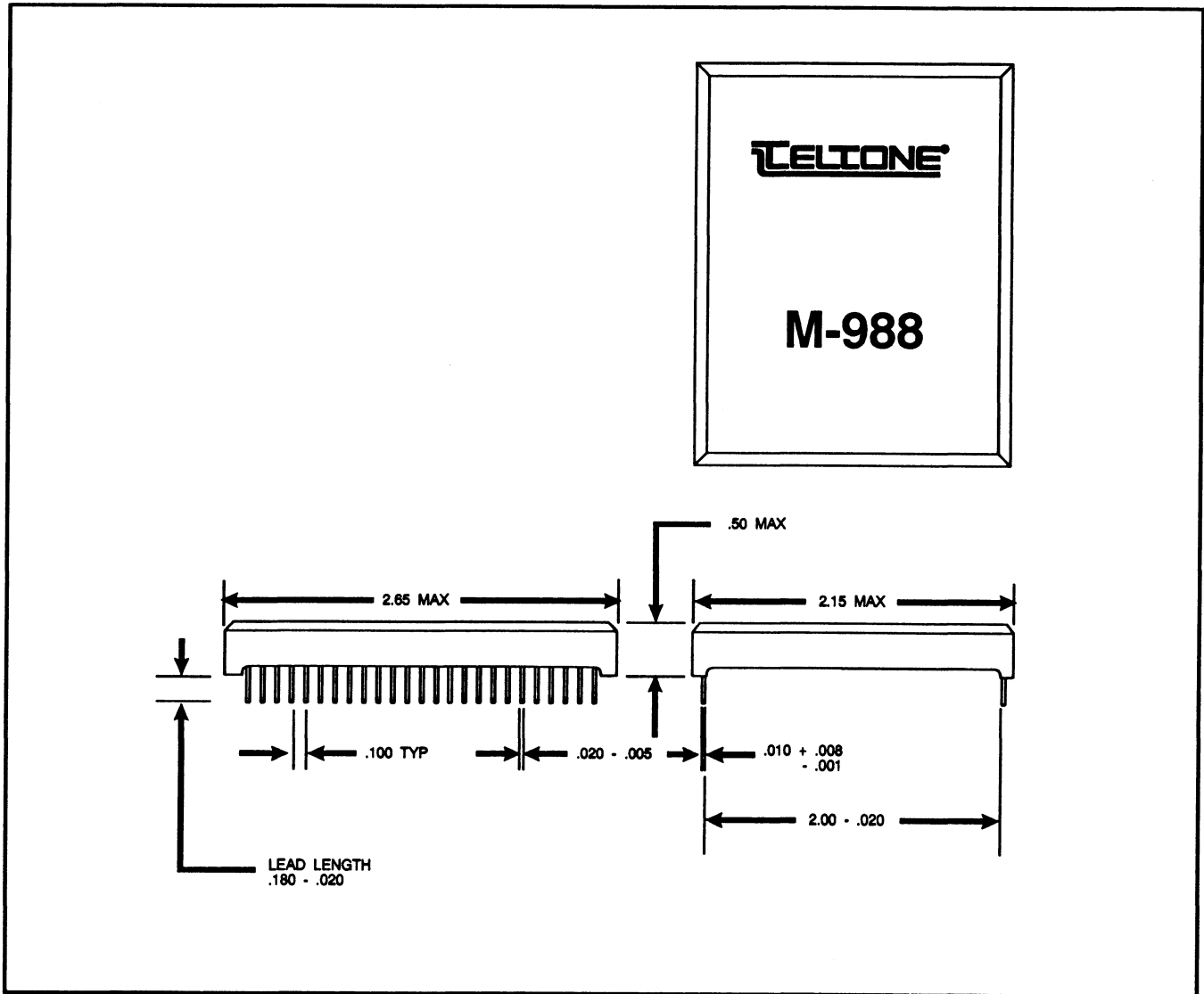
Figure 4 Package Dimensions

M-989 R2F MULTIFREQUENCY RECEIVER

The Teltone® M-989 MF Receiver is a single circuit board designed to provide high-performance detection of multitone trunk address signaling in accordance with international standards. The M-989 is easily mounted using plastic standoffs and mates with 0.25-inch-square pins on the mother board. Overall height above the mother board is kept to 0.75 inches.

Features

- Detects multifrequency tone signals containing frequencies 540, 660, 780, 900, 1020, and 1140 Hz
- Compatible with CCITT R2 MF recommendations
- High-impedance balanced differential input (AC coupled)
- Single 12 V supply
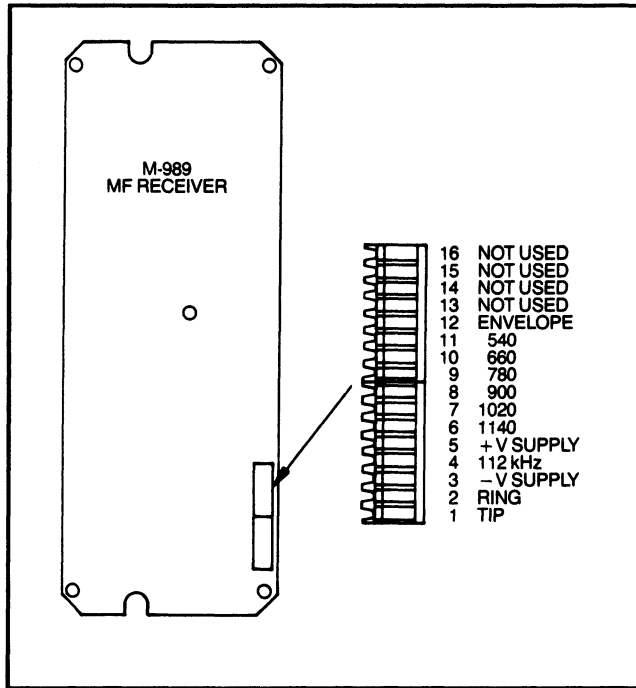
Figure 1 Pin Diagram
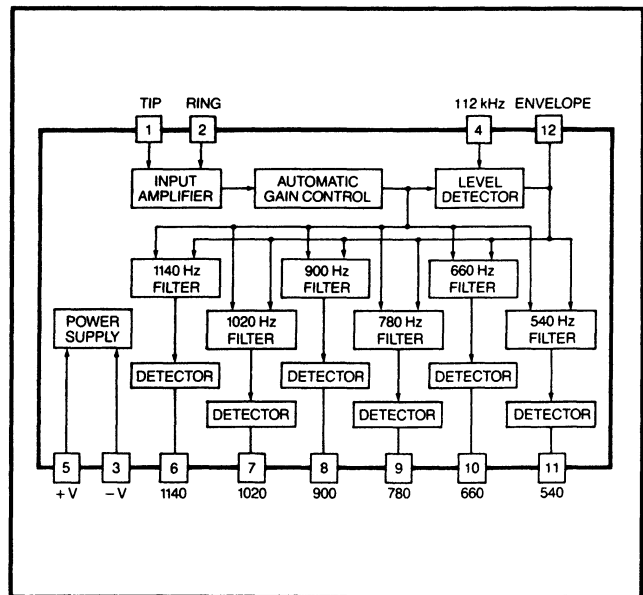
Figure 2 Block Diagram

Table 1 Pin Functions

Pin	Function
112 kHz	Input (3.58 MHz/32)
TIP	MF signal input balanced to Ring
RING	MF signal input balanced to Tip
+V	Positive supply voltage input
−V	Negative supply voltage (ground) input
540	Active low detect output for 540 Hz
660	Active low detect output for 660 Hz
780	Active low detect output for 780 Hz
900	Active low detect output for 900 Hz
1020	Active low detect output for 1020 Hz
1140	Active low detect output for 1140 Hz
ENVELOPE	Active low output when input signal is present

Table 2 Specifications

Parameter	Min	Max	Units	Remark
Signal Level	−35	−5	dBm/freq	600 ohms
Operation Time plus Release Time		80	ms	
112 kHz Duty Cycle	45	55	%	
112 kHz Low Voltage	0	2	volts	V supply = 12.0
112 kHz High Voltage	10	12	volts	V supply = 12.0
Signal Frequency Offset	−10	+10	Hz	
Twist (Level Skew)		7	dB	non-adjacent freq.
		5	dB	adjacent freq.
Input Impedance	75		kohm	
Tone Present Output	0.0	3.0	volt	V supply = 12.0
Tone Absent Output	9.0	12.0	volt	V supply = 12.0
Supply Current		100	mA	
Supply Voltage	10.8	13.2	volts	

Five mounting holes (0.156 inch diameter)
Sixteen electrical connectors (require 0.025 inch diameter pin)

PIN 1

2.000
(50.80)

0.025
(0.63)

0.400
(10.16)

0.100
(2.54)

8.000
(203.20)

3.775
(95.89)

3.000
(76.20)

1.200
(30.48)

3.300
(83.82)

0.350
(8.89)

0.150
(3.81)

0.500
(12.70)
MAX

8.700
(220.98)

DIMENSIONS:

INCHES

(MILLIMETERS)

M-989 RECEPTACLE

PLASTIC SPACER

MOTHER BOARD

0.750
(19.05)
MAX

Figure 3 Package Dimensions

SIGNAL

ENVELOPE
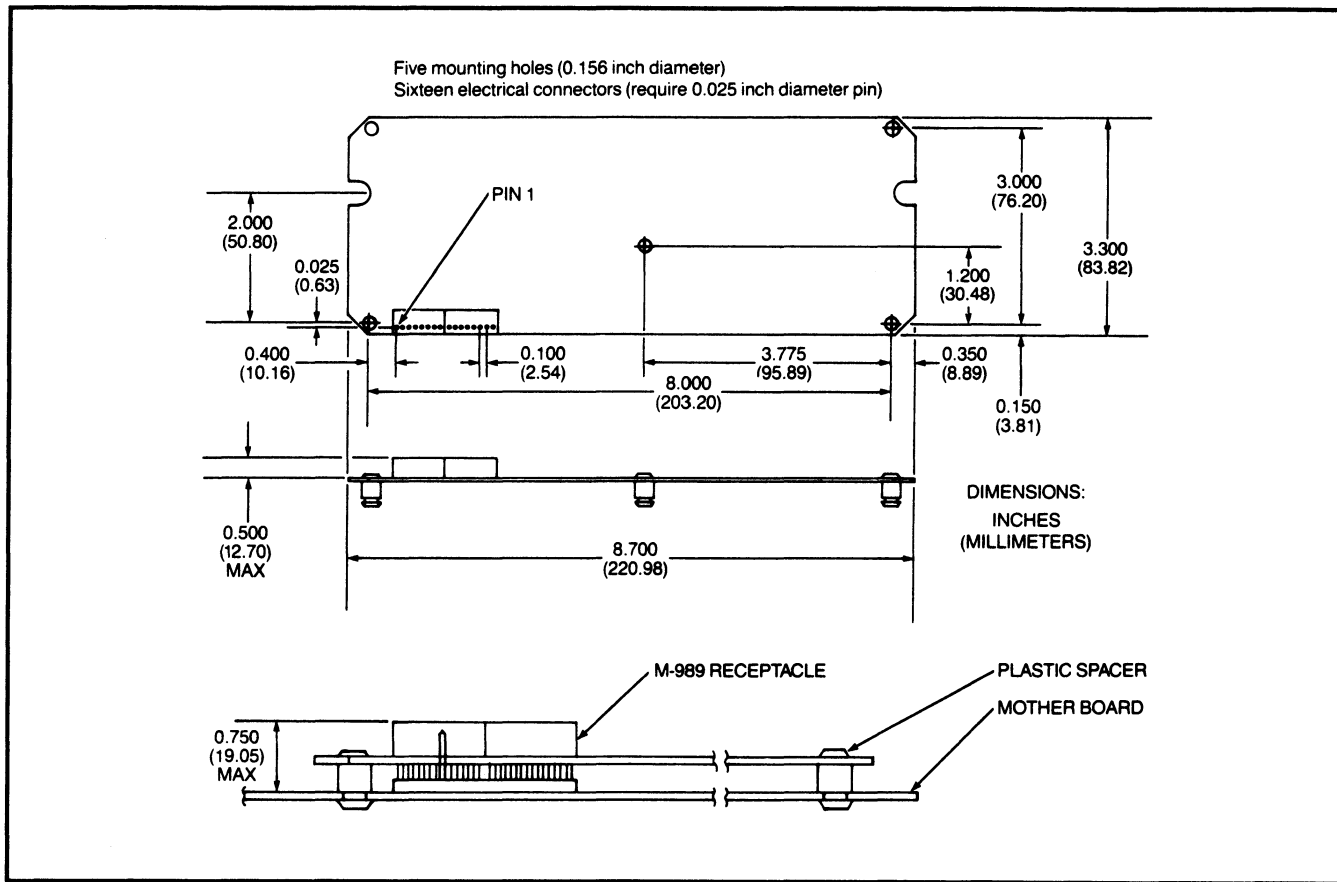
DETECTORS
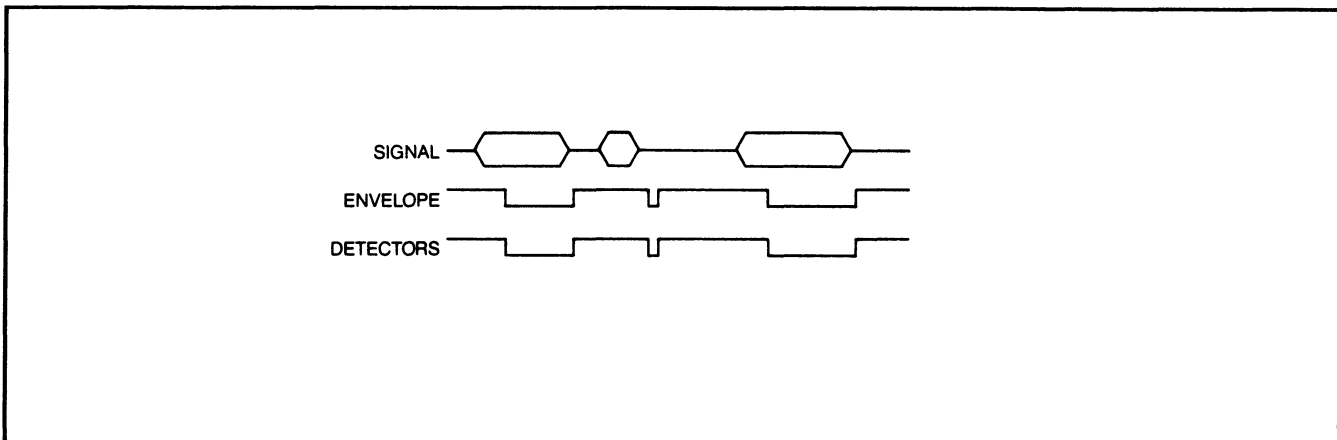
Figure 3 Timing Diagram

Telecom Solutions

ADD INTEROFFICE CALLING TO 1A/10A SERIES KEY TELEPHONE SYSTEMS

Service life of existing 1A/10A key telephone systems can be extended easily and inexpensively with Teltone® single-link intercoms and expansion modules. All units are FCC Part 68 registered.

Basic units add interoffice calling, providing a common circuit with battery feed, lamp supervision, and selective signaling of up to 10 or 19 telephones. Choose from five interchangeable modules:

* R-10 selectively signals up to 10 stations in response to rotary dialing.
* R-19 provides the same service as the R-10, and it can signal up to 19 stations.
* T-10 is similar to the R-10, but is for Touch-Tone® phones only.
* T-19 is similar to the R-19, but is for Touch-Tone only.
* C-19 is a combined Touch-Tone and rotary dial intercom. Similar to the R-19 and T-19, it includes the following additional features:
  * Provision for users at tone phones to set up conference calls (maximum of 5) without hanging up to redial each number.
  * Ringback tone to the caller during signaling.

These modules are designed to work with any 1A1/1A2 and 10A1/10A2 type key telephone systems manufactured by Western Electric Company, GTE Automatic Electric, ITT, and Stromberg-Carlson which offer selector-controlled intercom signaling service. They operate on the key system's 24-VDC power supply.

EX-18A Expansion Module adds another 18 stations to an intercom circuit. Up to five EX-18As can be added to one basic unit, providing an intercom system of up to 100 stations. The EX-18A is compatible with all Teltone single-link intercoms and may be substituted for expansion modules by other manufacturers.
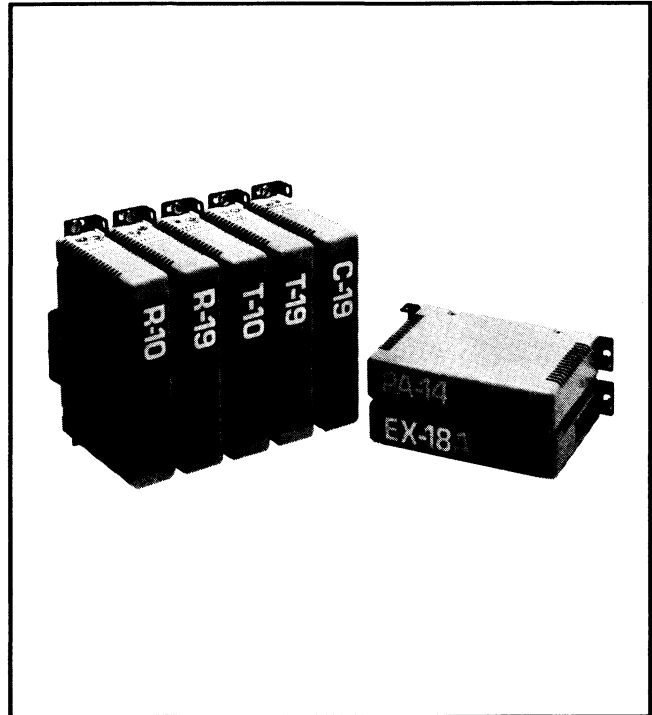
PA-14 Paging Access Unit provides dial access to a paging system. Background music can be routed through the unit for disabling when the PA-14 is dialed up. The PA-14 is compatible with all basic intercom units and with the EX-18A.

Easy Installation

All units can be mounted either on a wall or in a 7- or 9-inch key telephone cabinet (an optional adapter is required for installation in a 9-inch cabinet).

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8-1

Teltone Corporation / 10801-120th Avenue NE, Kirkland, WA 98033   Phone: 1-800-426-3926 or 206-827-9626   Fax: 206-827-6050   TWX: 910-449-2862
Teltone Limited / 3375-14th Avenue, Markham, Ontario, Canada L3R 2L6   Phone: 416-475-0837   Fax: 416-474-9151   Envoy User Name: TTL.HQ

8-2

ACCESS TO OFFICE TELEPHONE SERVICES, AWAY FROM THE OFFICE

The Teltone® M-106 Remote Service Accesss Unit provides direct inward system access (DISA) to office PBX or CO Centrex services from telephones outside the system, without attendant assistance. Off-premises callers can place local or toll calls through the system, access WATS, FX, and tie lines, or use specialized services such as dictation or paging systems and computer services. Users can access these services from home, hotel, mobile, or pay phones by dialing a number dedicated to the M-106.

Wall-mountable, single-card M-106 versions are suitable for PBX installations. Rack-mountable versions are available for large quantity, high-density applications such as installation in the CO.

Benefits
- Increased availability and usefulness of PBX and Centrex services. Unattended access means 24-hour availability.
- Control of toll calling expenses. Off-premises callers can use less expensive WATS or dedicated lines of the office telephone system.
- Improved accounting of business calling. Long-distance charges for business calls made off-premises are included in each month's office telephone bills.
- Increased convenience and time savings for callers.
- Facilitates WATS line resale.

Features
- Controlled access using a 3-digit security code that can be changed as desired (option).
- Redialing after a dialing error, busy signal, or answer tone, without reaccessing the M-106 (standard).
- Compatibility with loop or ground start systems (standard).
- Amplification of voice signals in both directions (option).
- Operation using -48 or -24 VDC power supply (option).
- Conversion of DTMF signals to rotary dial pulses (option).
- Call transfer or conferencing using a simulated switchhook flash (option).
- Restriction of call duration to 5, 10, 15, or 20 minutes (option).
- Ability to use remote power on/off switch (option).
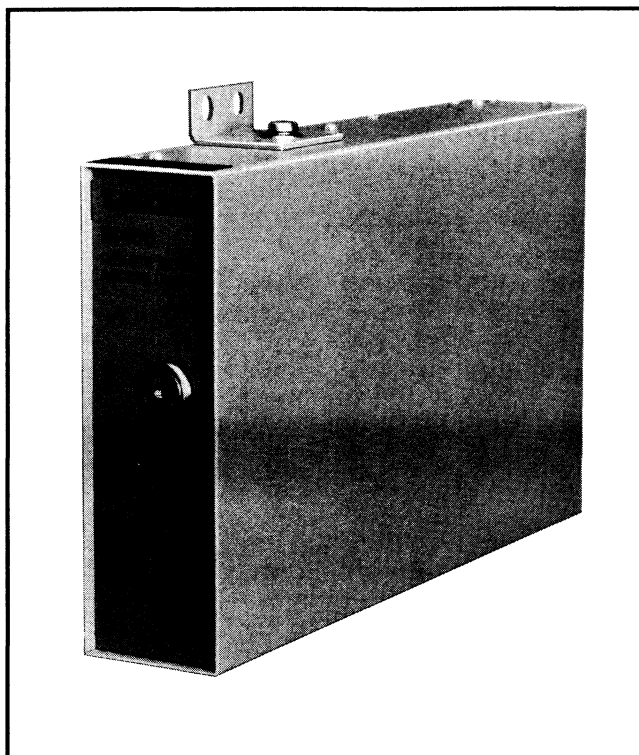
Specifications

DTMF INPUT SIGNAL REQUIREMENTS

Signal level (per tone)	-22 +4 dBm (0.06 to 1.2 VRMS)
Signal duration	≥ 40 ms
DTMF interdigital time	≥ 45 ms
Twist	-8 to +6 dB
Tone frequency tolerance	
Must accept	± (1.5% + 2 Hz)
Must reject	± (3.5% + 2 Hz)
Dial tone tolerance	≤ -12 dBm pr tone (0.2 VRMS)
Signal-to-noise ratio	22 dB

DC OUTPUT SIGNALING CHARACTERISTICS

Early line split	≤ 16 ms after reception of tone
Outpulse rate	10 ± 0.5 pps
Outpulse ratio	60 ± 2% break
Outpulse interdigital time	735 ± 25 ms
Talk path restoral time	40 ms following last break of last digit outpulsed
Memory capacity	20 digits (recirculating)

OPERATIONAL CHARACTERISTICS

Ringing voltage requirements

Voltage	40 to 150 VRMS
Frequency	16 to 66 Hz
Ring trip	280 to 518 ms after detection of ringing voltage

SPEECH PATH CHARACTERISTICS

Insertion loss

1500-3500 Hz	≤ 1 dB
350-1500 Hz	≤ 2 dB

POWER REQUIREMENTS

Input voltage

-48 VDC unit	-44 to -56 VDC
-24 VDC unit	-20 to -28 VDC

Supply current, single-card versions

Idle	160 mA
In use	200 mA

Supply current, rack-mount versions

Idle	120 mA
In use	200 mA
Suggested fusing, single-card versions	500 mA
Suggested fusing, rack-mount versions	One 1-1/3 amp fuse per six cards (each card can be fused independently if needed)

ENVIRONMENTAL REQUIREMENTS

Temperature	0 to 55 degrees C
Relative humidity	Up to 85%, noncondensing

FCC REGISTRATION

Federal Communications Commission (FCC) approved for direct connection to telephone company lines per part 68 FCC Rules and Regulations. Registration Number: AHH9WA-67638-OT-E.

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Teltone Limited / 3375-14th Avenue, Markham, Ontario, Canada L3R 2L6   Phone: 416-475-0837   Fax: 416-474-9151   Envoy User Name: TTL.HQ

8-4

TWO-WAY TOUCH-TONE®/ASCII COMMUNICATIONS

Until now, there has been a language gap between the ASCII world of computers and the Touch-Tone world of telephones that has prevented telephone-to-computer communication. Now, the Teltone T-310 Telephone Access Unit bridges this gap with two-way Touch-Tone/ASCII conversion. Using the set of T-310 commands, you can readily configure your computer to provide precise and complete call progress information (useful for enabling system security), to answer and originate calls unattended, and to collect data signaled from a Touch-Tone phone. You can also combine these commands into system-building software. Create systems for energy management and financial transactions, or (when used with the audio port) for inquiry response and telemarketing, just to name a few.

At all times, your computer can monitor the T-310's activity status, allowing its alternation with an (optional) auxiliary phone. Once a call is established, the T-310's Touch-Tone/ASCII translator gives the option of one- or two-way communication. When you are away, you can use a Touch-Tone phone to signal your programmable security access code to your T-310 and send data or instructions (to perform programmed functions) via Touch-Tone. So you can control or input to your system from almost anywhere.

Features

- *Autoanswer/originate* accepts or places calls automatically.

- *Audio Port* lets you induce voice and other signals, via auxiliary equipment, onto the telephone network.

- *Inactivity Timeout* can be implemented to reduce phone bills by automatically disconnecting when there is no activity for a selected period of time.

- *Programmable Selection of Touch-Tone or Pulse Dialing* is compatible with any phone system.

- *RS-232-C (V.24)* is the most common method of communicating with data devices.

- *Software Control and System Status* let you choose from a broad array of options and quickly review your selections via your computer terminal. No need to remember what you set up.

- *Terse Mode* provides only a numerical status code; verbose mode adds a verbal equivalent of the code for user convenience.

- *Touch-Tone/ASCII Conversion* allows you and those you authorize to input data to your computer using just a Touch-Tone phone.

- *Primary and Secondary/Dial Tone Detection* enables you to access and identify two-level-entry dialing equipment, such as PBXs.

- *Automatic Tracking of Line Status* informs you of hook status, seize failures, etc. The continual monitoring of hook status permits you to use an auxiliary phone without unwanted interruptions from auto-originate functions.

- *Automatic Tracking of Call Status* recognizes dial, busy, ringback tones and answer (voice detection) to handle calls automatically. You can, if you wish, monitor the status of calls or log call records on your computer.

- *Programmable Security Checking* disconnects callers who fail to enter the correct security code in the allotted
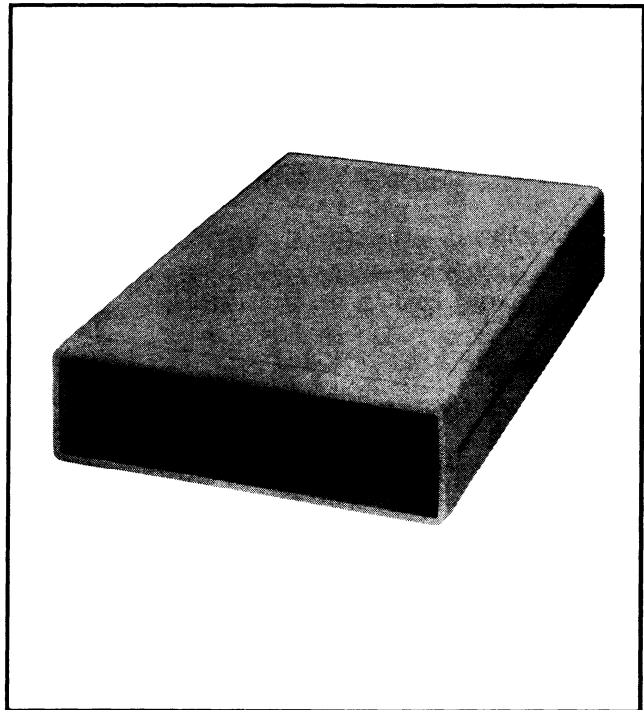
time. In addition, you can develop a simple program for dialback security that validates callers by disconnecting and calling them back. Thus you provide double protection for your data base, while allowing system access to authorized users.

- *Switchless Setup* means there are no option switches to set: progrmaming is via ASCII instructions from your program or keyboard. The T-310 will automatically select the most common options if not otherwise instructed. Program option changes are easily made.

- *Switchhook Flash Capability* enhances the T-310's use in telephone switching systems, like PBXs, for call transferring, holding, and conferencing.

Specifications

DATA PORT

Electrical	EIA RS-232-C (CCITT V.24)
Connector	DB-25S type (female)
Interchange rate	300 baud
Communication protocol	Asynchronous ASCII, with 1 start bit, 7 data bits, 1 parity bit, and 1 stop bit
Parity supported	Space, Mark, Even, Odd
Flow control	Bidirectional in-channel XON/XOFF
Circuit indicator LEDs	OH —Off-Hook CD—Call display, DTMF (Touch-Tone®) transmsission

PHONE LINE

Dial signaling	7 digits per second, DTMF mode (-9 dBm maximum); 10 pulses per second, pulse mode

AUDIBLE PROMPTS

Connection tone	One second burst of non-DTMF tone
Acknowledgment tone	70 ms burst of DTMF "A"
Error tone	Triple burst of DTMD "D" , 70 ms on and 70 ms off

TONE DETECTION

DTMF detection	All 16 digits. Receive level + 6 dBm to -30 dBm, 40 ms signal detection and 40 ms interval detection'
Dial tone detection	
Busy tone detection	60 IPM (interruptions per minute)
Reorder tone detection	120 IPM
Audible ringing ("Ringback tone") detection	
"High" tone detection	Tone > 540 Hz, 3 seconds on
"Low" tone detection	Tone > 320 Hz and < 540 Hz, 3 seconds on

AUDIO INPUT

Electrical	± 20 volts maximum. Input impedance 10 kilohms minimum. Signal level internally limited to -9 dBm maximum, per FCC specifications
Connector	3/32-inch subminiature audio jack

POWER TRANSFORMER REQUIREMENTS

Input voltage	120 VAC nominal at 60 Hz
Output voltage	16 VAC at 375 mA nominal

PACKAGE

Dimensions	5.5" wide x 1.5" high x 9.0" deep (139.7 x 38.1 x 228.6 mm)
Connector plug	
Inside diameter	0.082"
Outside diameter	0.218"
Length	0.413"

TELEPHONE LINE CONNECTION CABLE REQUIREMENTS

Positions	6 (four inner contacts)
Plugs	Both emds

FCC REGISTRATION

Registered under FCC Part 68 (AHH9WA-15188-MD-T)

DEMO OR TEST FAX MACHINES, PHONES, AND MODEMS

The Teltone® TLS-3 Telephone Line Simulator is an ideal tool for demonstrating telephones, fax machines, or modems during seminars and showcase events or in retail stores.

A "portable CO", the TLS-3 also provides a means for an installer to check a telephone or telephone system installation where Central Office (CO) lines are not available.

The TLS-3 provides two simulated lines, each with a separate battery feed. Modular jacks on the TLS-3 front panel enable connection of a telephone, or a telephone line, to each numbered TLS-3 line. Each connected station can ring the other and a talk path is established between stations. Precise dial tone, busy tone, and ringback tone are supplied to the calling station. Ring trip occurs upon station answer. The TLS-3 comes equipped with an AC power cord and two modular cords with alligator clips, which enable line connections via 66-type or simular terminal block.

The TLS-3 simulates both loop start and ground start trunks, enabling limited testing of PBX installations. Loop start/ground start operation is controlled by two switches, one for each TLS-3 line.
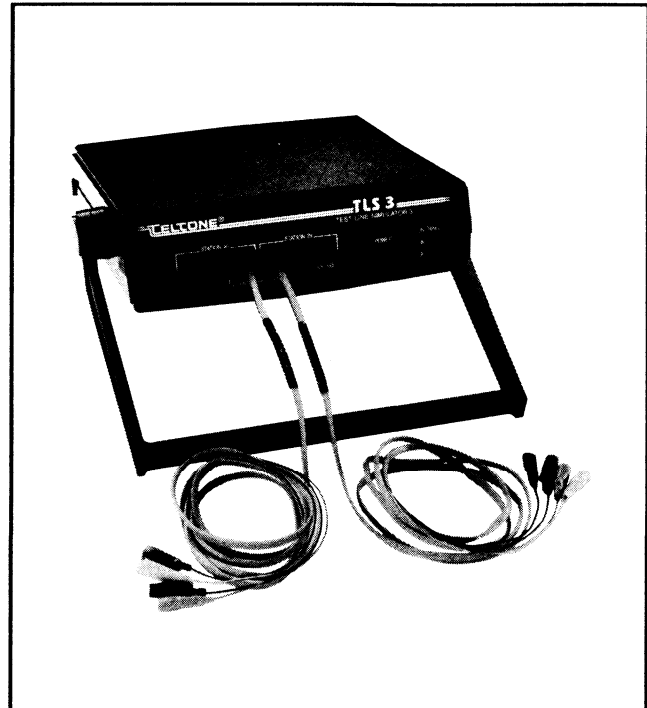
Features
* Supplies precise dial tone, busy tone, and ringback tone
* Loop start or ground start operation
* Two simulated lines with talk path
* Accepts tone and rotary input
* Interrupted or continuous ringing
* Ringing voltage source with short circuit protection
* AC powered with power switch and internal fuse (no batteries needed)
* Ground reference provided on A1 lead of modular jacks
* Polarity verification capability
* Optional carrying pouch for TLS-3 and cords

Specifications

AC POWER INPUT
Voltage   115 ± 15 VRMS
Current   0.2 A max
Fuse (internal)   1/4 A (fast blow)
Frequency   49.5 to 60.5 Hz

POWER
Dissipation (with ringing generator shorted):   20 VA max

TELEPHONE LINE CIRCUIT (Loop Start Operation)
Voltage (loop start operation):   -24 ± 3 V, ref. Ring to Tip; open circuit
Current
  Maximum (Ring and Tip shorted):   68 mA
  Minimum (at maximum loop of 250 ohms excluding telephone):   20 mA

TELEPHONE LINE CIRCUIT (Ground Start Operation) (See Note 1)
Tip ground connect   175 ± 35 ms after uninterrupted ground (1000 ohms or less) is applied to Ring
Tip ground release   375 ± 35 ms after loop opens
Forced connect   Connects Tip ground upon ringing
Forced disconnect (see Note 2)   375 ± 35 ms after Tip ground has been released from the other line
Maximum current (Ring) 135 mA (Ring grounded)
Maximum current (Tip)   3 mA (Tip ground released)

RING SOURCE

Voltage	100 ± 10 V
Current	80 mA max
Maximum load	5 ringer equivalences (Class A)
Trip	1000 ohms or less

DTMF DETECTION

Frequency	Accept ± (1.5% + 2 Hz) Reject ± 3.5%
Tone time	40 ms min
Interdigital time	40 ms min
Amplitude	+4 to -18 dBm per frequency and ≤ 6 dB difference between frequencies

ROTARY DETECTION

Rate	5 to 23 pps
Interdigital time	315 ms min
Break time	30.5 ms min
Make time	12.5 ms min
End-of-digit recognition time	95 ms min

LOOP CURRENT DETECT (see Note 3)

On-hook detect	300 ms ± 20 ms
Off-hook detect	100 ms ± 20 ms

INTERRUPTED RING TIMING

Ringing	1.6 sec ± 10%
Silent	4.8 sec ± 10%

TONE CHARACTERISTICS

Dial tone	350 Hz ± 0.5% @ -17 dB ± 1.5 dB; 440 Hz ± 0.5% @ -17 dB ± 1.5 dB
Busy tone	480 Hz ± 0.5% @ -17 dB ± 1.5 dB; 620 Hz ± 0.5% @ -17 dB ± 1.5 dB; 500 ms on, 500 ms off, repeating (60 IPM)
Ringback tone	440 Hz ± 0.5% @ -17 dB ± 1.5 dB; 480 Hz ± 0.5% @ -17 dB ± 1.5 dB; both frequencies modulated at 20 Hz ± 1%

ENVIRONMENT

Operating temperature	0 to 55 degrees C
Storage temperature	-40 to 55 degrees C
Humidity	85% noncondensing

Note 1: After Tip ground is connected, the operation and specifications are identical to loop start operation until Tip ground is released.

Note 2: The time will be the same if the other line is in loop start operation.

Note 3: In ground start operation, the reference is from the time Ring ground is applied.

SOLUTIONS FOR EXTENDING THE LIFE OF YOUR KEY OR PBX SYSTEM

Off-Premises Supervision Control Unit for 1A2 and 10A2 Key Systems
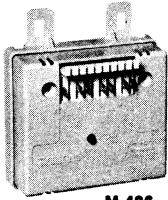
- For remote phones—garages, warehouses, outdoor locations
- Eliminates costly control pair
- Positive status indicator
- End the "Who's on Hold" question

M-486

Off-Premises Supervision Control and Line Card for 1A2 and 10A2 Key Systems

- Off-premises control without adding control pair
- Combine M-486 features with 400 series line card
- Mounts in standard line card slot
- Minimal installation time

M-487

Single Link Intercoms for 1A2 and 10A2 Key System Expansion
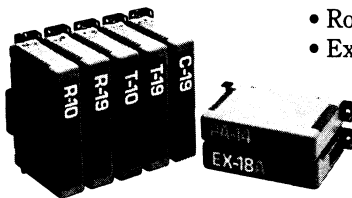
- 10- and 19-station units
- Rotary, tone, and combination
- Expand to 100 Stations
  - Easy to install—no adjustments
  - Interchangeable units
  - Paging access
  - Music on hold
  - Economical

RTC INTERCOMS

Service Evaluation for PBX Systems
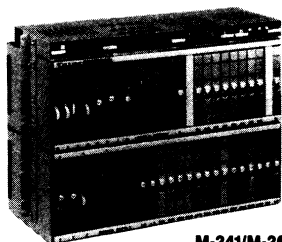
- For catalog houses, service departments, sales offices, etc.
- M-260 Automatic Call Disposition Analyzer provides automatic call sampling and analysis
- M-241 Remote Service Evaluation Unit enables operator monitoring of equipment or employee performance

M-241/M-260

Tone and Rotary 19-Station Intercom on One Card

- Pin-for-pin compatible with WECO 424/407/440/478 KTUs
- Circuit busy LED indicator
- Adjustable ring burst duration control
- Compatible with 1A2 and ComKey; 7A, 14A, and 21A systems

M-426

Remote Service Access Unit Adds DISA* Feature to PBX and Key Systems

- Use WATS, FX, TIE, and other system features—anytime—from anywhere—without an attendant
- 3-digit security code
- Optional voice amplifier
- File-mounted units available

M-106

*Direct Inward System Access

Telephone Line Simulator—A Portable Central Office in a Box

- Installation tool
- Phone and phone system demonstrations
- DTMF and rotary
- Precise dial tone
- Busy tone
- Interrupted ringing and ringback tone
- Two lines with talk path
- Loop and ground start

TLS-3

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8-10

CENTRAL OFFICE SWITCH ENHANCEMENTS AND SERVICE EVALUATION SYSTEMS

Convert-a-Unit™ File-Mounted Tone Converter for KTS,PBX, or CO Applications

M-161

- Our most versatile converter
- −24 or −48 VDC models
- 5-, 20-, and 25-unit card files
- E&M lead model
- Selectable ring detector and ground start recognition
- FCC Part 68 registered

Convert-a-Pak™ Tone Converter for KTS, PBX, or CO Applications
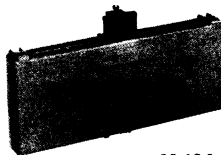
M-164

- Individually packaged converters rack or wall mount with special mounting bracket
- −24 or −48 VDC models
- Intercom and KTS dedicated line models
- ANI forwarding
- # sign release
- Timeout start at off-hook or on receipt of 1st digit (optional)

Tone Converter for SxS and Crossbar Central Offices
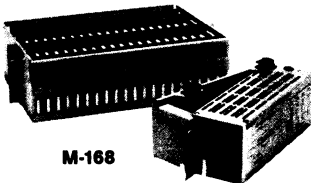
M-168

- Single-circuit or space-saving dual-circuit card versions
- Rack, switch, or wall mountable (4-, 20-, and 25-unit card files)
- −48 VDC operation only

CallPro™ Call Processor for SxS and Crossbar Central Offices

M-166

- Adds microprocessor intelligence to electromechanical switches
- Absorbs, translates, adds, or repeats dialed digits
- Scores of applications including service code routing, toll restriction
- Extends switch life
- Tone-to-pulse conversion
- Class mark control or sleeve lead monitor connection
- Software available for user programming

Coin-Free Trunk Adapters for SxS and No. 5 Crossbar Central Offices
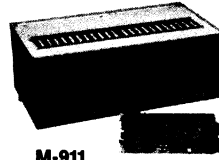
M-911

- 0, 0 +, 1 +, and 3-digit calls coin-free
- Coin-free 7-digit numbers
- Low-cost M-912 installs in less than 1 hour per No. 5 Crossbar OR
- M-911 also provides DTMF conversion in SxS offices

Precise Dial Tone Generator

M-904

- Fully redundant dial tone supply
- Provides major and minor alarms, audible and visual
- Output up to one Watt
- Allows field selection of single or dual frequency dial tones
- Provides 350 and/or 440 Hz precise tones
- Mounts in 19- or 23-inch racks

Network Analysis Systems

M-263

M-260

M-242
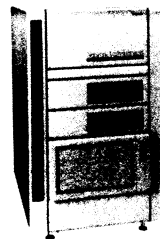
- Fully automated call sampling, polling, and reporting
- M-263 Poller Processor automatically collects and processes service evaluation data from 200 M-260-equipped offices, and generates standard or custom reports
- M-260 Automatic Call Disposition Analyzer (ACDA) monitors up to 100 analog lines or trunks, analyzes each call, and records call dispositions (battery backed). Evaluation data can be collected any time day or night
- M-241 and M-246 live evaluation units permit evaluation of equipment or employee performance
- M-242 Operator Console permits simultaneous monitoring of up to 5 remote units

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Teltone Limited / 3375-14th Avenue, Markham, Ontario, Canada L3R 2L6   Phone: 416-475-0837   Fax: 416-474-9151   Envoy User Name: TTL.HQ
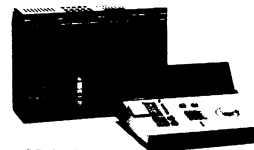
8-12

Section 9

Application
Notes

APPLICATIONS FOR DTMF AND PULSE TELEPHONE DIALING

Including Remote Access and Control

CONTENTS

Computer data entry, operations monitoring, and equipment control are just a few of the many functions that can be performed from remote locations using a standard telephone set and the Public Switched Telephone Network. Telephone dialing is a simple yet reliable form of data transmission which offers system designers the following unique advantages:

- A worldwide network already in place and economical to use

- Inexpensive and user-friendly "terminals" (telephone sets)

- Readily obtainable hardware

Teltone Corporation offers an entire family of DTMF and pulse dialing receivers to make your application simple and cost-effective. This guide provides the background information you will need to get started, together with detailed diagrams and descriptions of circuits that you can use intact or modify to suit your purposes.

PUBLIC SWITCHED TELEPHONE NETWORK (PSTN)

The principal elements of the PSTN are shown in block diagram form in Figure 1. The telephone line is a wire loop which connects each station to a local switching center called a "central office" (CO). The called and calling stations may be connected to the same CO, or they may be connected to different CO's linked by intermediate switching centers. Two types of station instruments are in common use today: pulse-dialing (rotary) telephones and tone-dialing telephones. Pulse-dialing telephones transmit digits as serial makes (connections) and breaks (disconnections) of the telephone line, while tone-dialing telephones generate pairs of tones called Dual-Tone Multifrequency (DTMF) tones. DTMF dialing is the newer system and is usually preferred, for reasons which will be explained later in this guide.
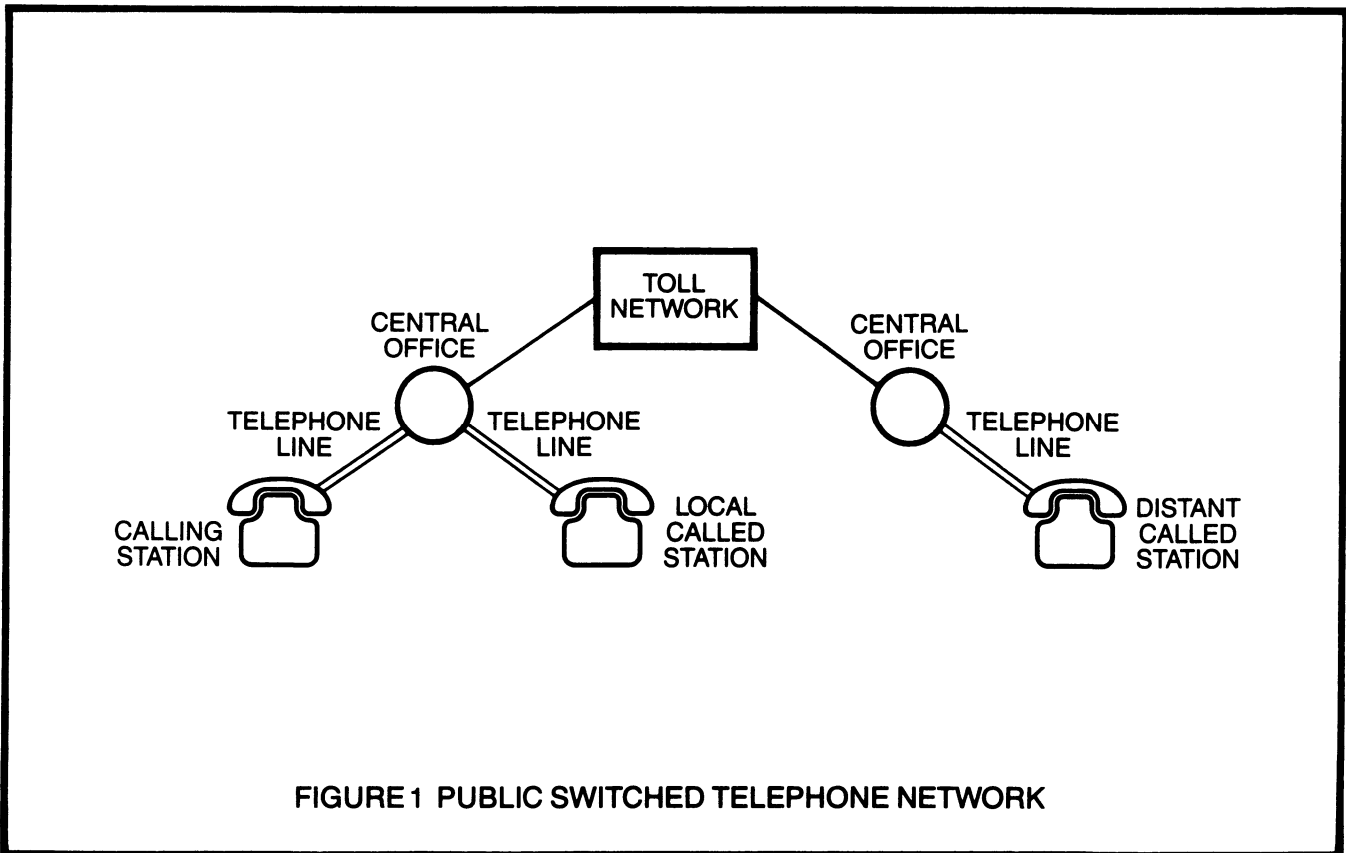
FIGURE 1 PUBLIC SWITCHED TELEPHONE NETWORK

THE TELEPHONE LINE

In Figure 2(a) the station-to-CO connection is shown in detail. Lifting the telephone handset is called going "off-hook," and its effect is to close the telephone hookswitch and allow DC current (called "loop current") to energize the CO current sense relay. The CO then couples dial tone to the line, which is the caller's signal to dial. The pulses or tones generated by the calling telephone are detected at the CO and used to route the call. Replacing the telephone handset is going "on-hook," and its effect is to open the hookswitch, interrupt the flow of loop current, and de-energize the current sense relay. After the relay has been de-energized for several hundred milliseconds, the CO drops the connection and the system returns to idle.

Figure 2(b) is a schematic of the electrical circuit formed by the elements of Figure 2(a). In North America, the off-hook telephone appears as about 600 ohms AC and 100 to 200 ohms DC. The telephone line has wire-to-wire capacitance and simple resistance resulting from the length of the wire. Long telephone lines have capacitances which can attenuate the higher frequencies and resistances which can limit the DC current. The most common CO circuit equivalent is a DC battery feeding loop current via two large, balanced inductances in parallel with a capacitively coupled 900-ohm resistance. The inductances are usually part of the current sense relay, and the battery voltage can be -36 to -60 VDC depending on the system. In North America, -50 VDC is most common.

Figure 3 shows the general line conditions that occur during an off-hook and dial sequence, as seen from the CO. DTMF and pulse dialing are included as part of the same sequence, although this is not likely to occur in a real application. Loop current is usually 20 to 100 milliamperes, while DTMF tones arriving at the CO are usually 50 to 1000 millivolts (rms) depending on line conditions. Most pulse dialing occurs at 8 to 12 pulses per second with a line make-to-break ratio of about 60 to 40. This means that a large digit such as "9" can have a duration greater than one second. In contrast, DTMF tones are usually 50 milliseconds in duration with intervals between tones of at least 40 milliseconds, for a total signal cycle time of about 100 milliseconds. The significantly greater speed of DTMF dialing—as much as a factor of 10—is one of its chief advantages over pulse dialing.
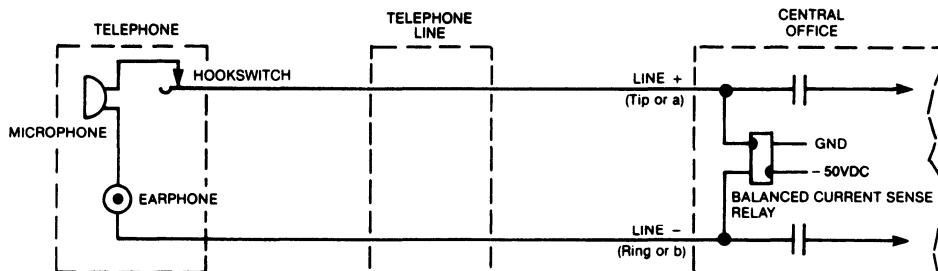
FIGURE 2(a) TELEPHONE LINE TERMINATIONS
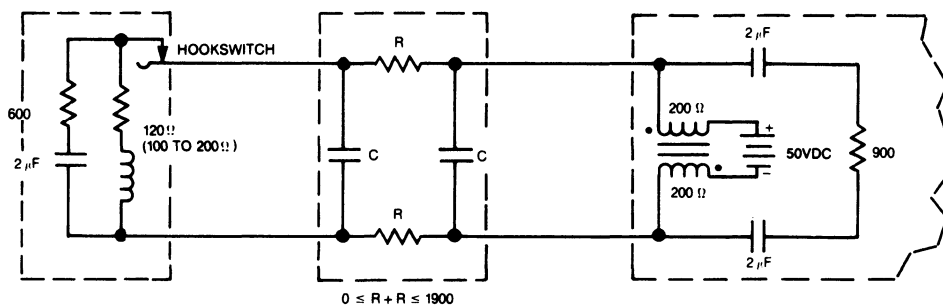
FIGURE 2(b) TELEPHONE LINE SCHEMATIC DIAGRAM
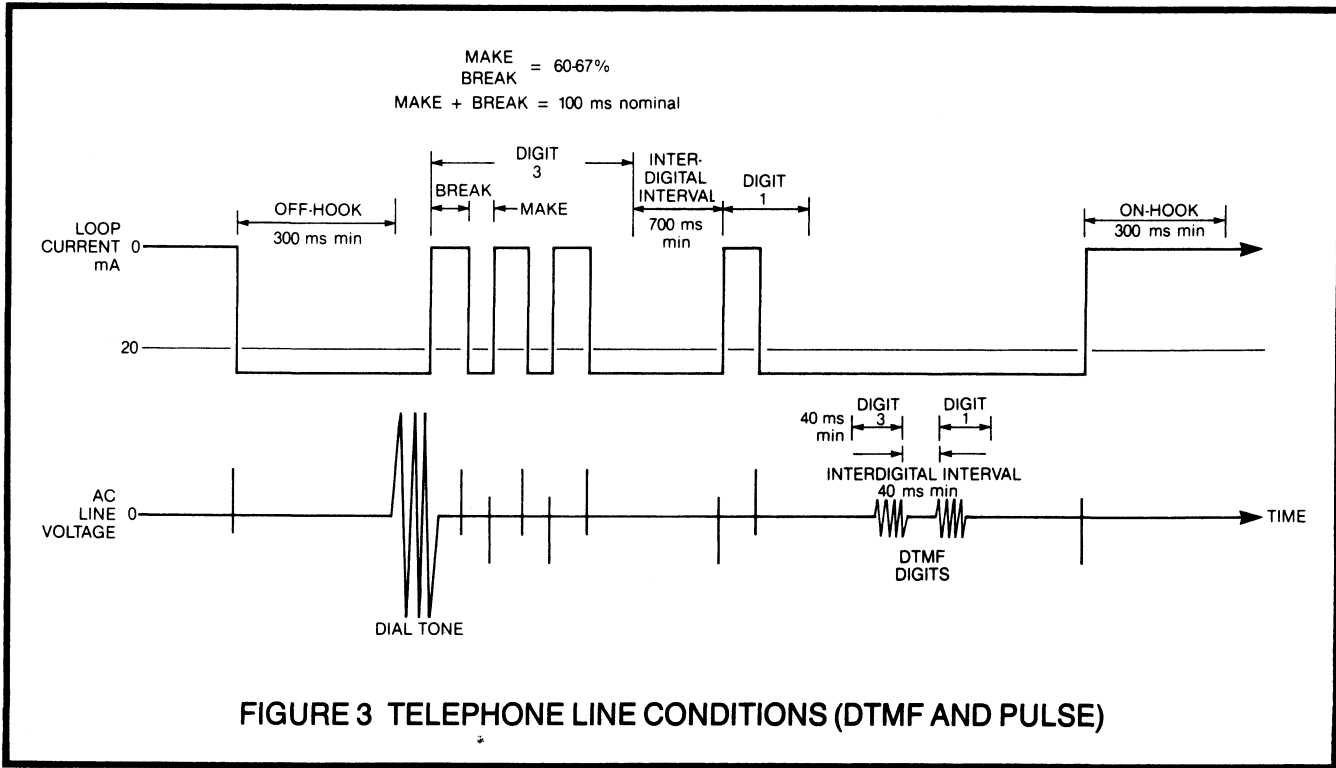
FIGURE 3 TELEPHONE LINE CONDITIONS (DTMF AND PULSE)

THE STATION-TO-STATION CONNECTION

Figure 4(a) shows a case of the station-to-station connection in which the calling station and the called station are linked via toll transmission facilities. Dialed digits are stored at the CO of the calling station, then forwarded via other switching centers to the CO of the called station. This signalling is either along the switching path as MF (a special 2-of-6 tone code) or via a separate digital channel dedicated to this purpose. When the call is answered, an indication is returned through the network from the called station's CO to toll recording equipment at the calling station's CO.

In Figure 4(b) the basic station-to-station connection is shown in electrical schematic. Note the capacitor and transformer coupling which limits DC signals to the local telephone lines and ensures that only AC signals are transmitted station to station. Originally engineered to provide a channel for speech, this AC path also accommodates newer schemes for communicating in the same frequency spectrum, extending from 300 Hz to 3300 Hz. These schemes include FSK data, facsimile, and DTMF. The capability for station-to-station

signalling, also called "end-to-end" signalling, is another advantage of DTMF dialing over pulse dialing.

Although the human ear can tolerate quite a bit of noise and still understand spoken words, the electronic detection of spectral information is complicated by impulse noise, random noise, cross-channel interference, and circuit losses. The biggest penalties are imposed by the local telephone lines where losses due to line resistance and capacitance are often as great as 8 dB. Toll transmission facilities have better control over conditions and usually do not impose more than 10 dB loss, despite their longer length. Both toll and local lines also introduce noise of many types. As shown in Figure 5, a tone transmitted at one station may be greatly attenuated at the receiving station. Moreover, there is likely to be additional difficulty for the receiver in terms of signal-to-noise ratio and individual tone level variations. For these reasons, the engineering of DTMF receivers usually involves compromises and design trade-offs between sensitivity and detection reliability.
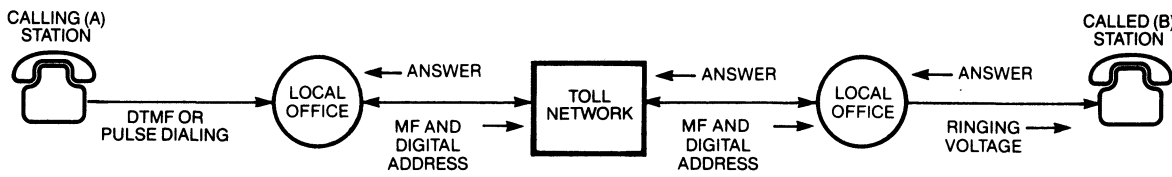
FIGURE 4(a) SIGNALLING ON A CALL TO A DISTANT STATION
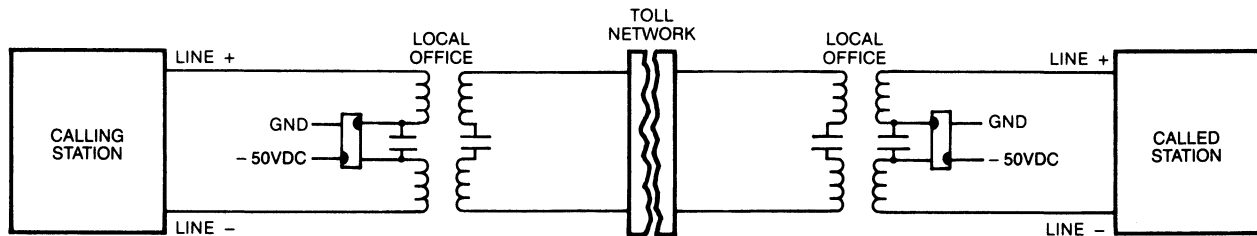
FIGURE 4(b) TYPICAL CIRCUIT FOR COMPLETED LINK WITH A DISTANT STATION
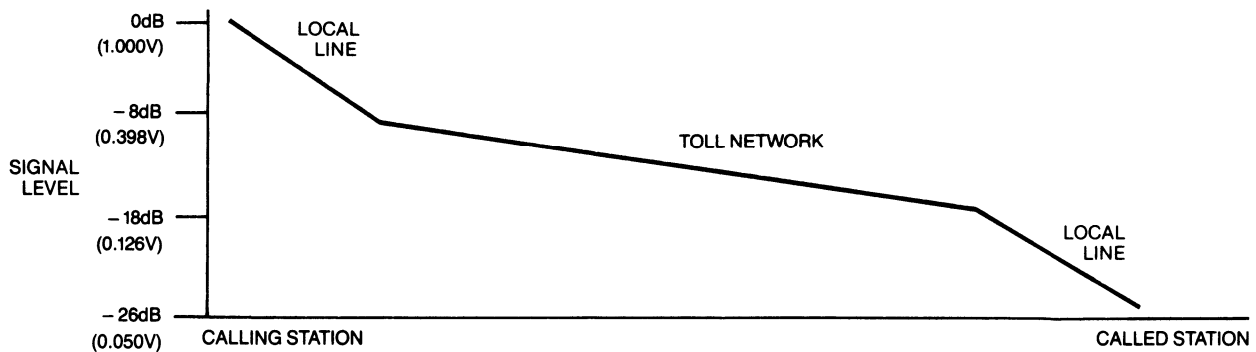

FIGURE 5 AN EXAMPLE OF LOSSES ENCOUNTERED OVER A LINK

DUAL-TONE MULTIFREQUENCY (DTMF) SIGNALLING

The DTMF dialing scheme was developed by Bell Laboratories and introduced in the United States in the mid-1960's as an alternative to pulse (rotary) dialing. Offering increased speed, improved reliability, and the convenience of end-to-end signalling, DTMF has since been adopted as standard and recommended for use by such organizations as the International Telephone and Telegraph Consultative Committee (CCITT), the Conference of European Postal Telecommunications Administrations (CEPT), Nippon Telegraph and Telephone (NTTPC), and others around the world.

Each of the 16 possible DTMF signals shown in Figure 6 is a composite of one frequency from a high-frequency (column) group, and one frequency from a low-frequency (row) group. This 2-of-8 scheme often reduces to 2-of-7, because signals in the 1633 Hz column are reserved for special non-dialing functions.

COLUMN

	1209	1336	1477	1633
697	1	2	3	A
770	4	5	6	B
852	7	8	9	C
941	*	0	#	D

ROW

(FREQUENCIES IN Hz)

FIGURE 6 DTMF FREQUENCY ASSIGNMENTS

RECEIVER PARAMETERS

Because DTMF senders and receivers are designed for a unique electrical environment, the parameters used to describe their performance may be unfamiliar. Here is a brief explanation of some of the more important terms:

Sensitivity ("A" level)—The lowest level signal that is guaranteed to be detected. The range of levels detected is known as the "dynamic range," which usually extends to about 30 dB above the A level. Absolute levels are expressed in dBm, assuming a terminating impedance of 600 ohms.

Twist—The ratio of the level of the high-frequency DTMF signal component to the level of the low-frequency signal component. Most modern receivers can handle level differences of +4 to −8 dB.

Frequency Deviation—Deviations from nominal sometimes arise because of inaccuracies in DTMF senders and frequency shifts in analog carrier systems. Receivers are expected to detect signals that are off by as much as 1.5 percent plus 2 Hz from nominal throughout their dynamic range.

Signal-to-Noise Ratio—This ratio is the minimum separation between signal and noise that will not degrade detection accuracy over long strings of data. It can be specified with the signal on nominal frequency or deviated.

Detect/Reject Times—The standard choice for both signal and pause detect times is 40 milliseconds. Reject times are called for because of common telephone network occurrences that may interrupt or generate tones briefly.

Dial Tone Tolerance—Tones indicating readiness to accept dialing must not interfere with DTMF signal detection. Truly "dial tone immune" receivers tolerate dial tones more than 22 dB stronger than the A level without degrading long strings of data.

Speech Immunity—Speech and caller background noise are often present when DTMF receivers are on line. Because the human voice contains many tone combinations similar to DTMF digits, receivers must be carefully engineered to distinguish between actual signals and simulated signals. Test tapes are available that can be used to obtain typical numbers of simulations for different receivers.

The division of frequencies into high and low groups simplifies the design of a DTMF receiver as shown in Figure 7. This particular design (Teltone circa late 1970's) embodies a standard approach. When connected to a telephone line, radio receiver, or other DTMF signal source, the receiver filters out dial tone and noise, separates the signal into its high-frequency group and low-frequency group components, and then digitally measures zero crossings over averaging periods to produce digit decoding.

As shown in Figure 8, the detection of DTMF signals can be complicated by the presence of 50/60 Hz power line noise, dial tone of various frequencies, random noise, and other sources of interference. Dealing with these problems while remaining immune to speech-simulated digits presents the greatest challenge to DTMF engineers. The tolerable interference line shown in the figure is recommended by the CEPT and is considered a design goal by Teltone and other manufacturers of quality DTMF receivers.

FIGURE 7 TYPICAL DTMF RECEIVER ARCHITECTURE

FIGURE 8 DTMF SIGNALLING ENVIRONMENT
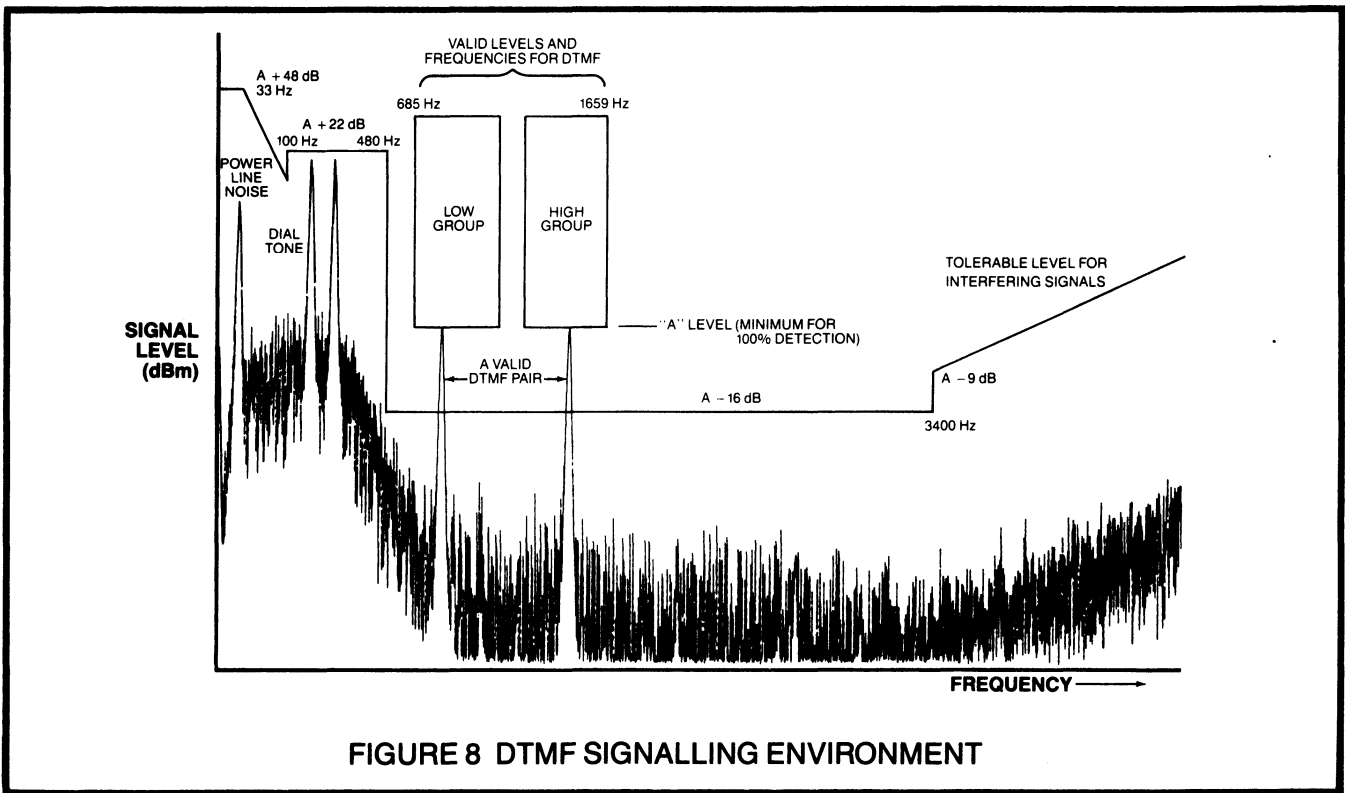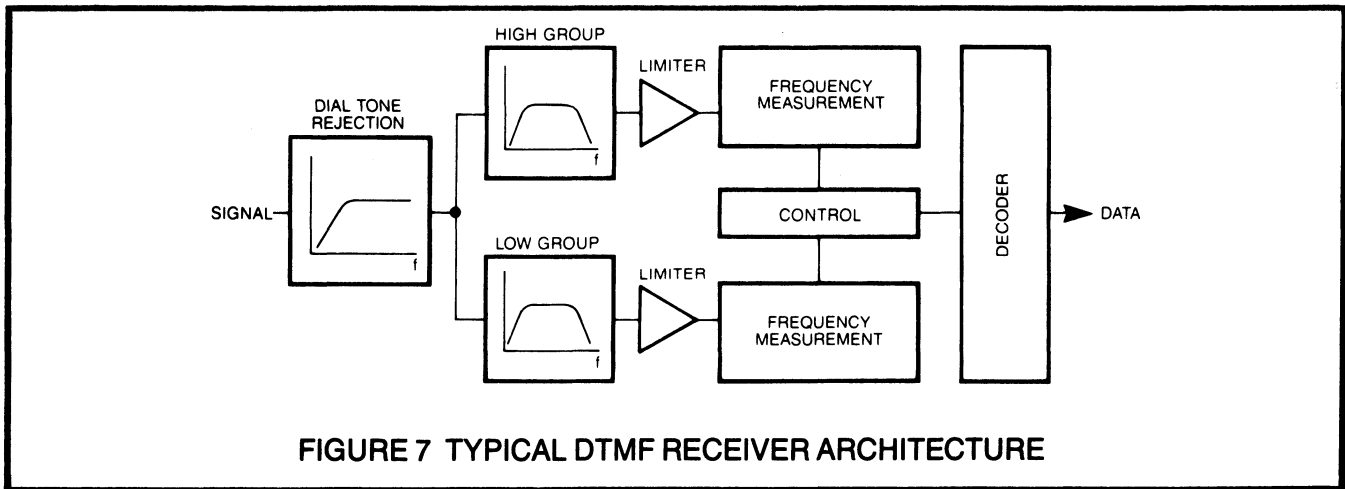
DETECTING SIGNALS
AS THE PRIMARY RECEIVER

DTMF and pulse dialing receivers were originally developed as "primary" or dialed digit receivers whose data was used to determine call destinations. Examples of their use in this capacity can be seen on this page. Figure 9 shows a typical Private Branch Exchange (PBX) or CO switching equipment application, while Figure 10 shows a simple receiver connected to a telephone set for dedicated digit entry. Both circuits are easy to apply because of the wide dynamic ranges and time-guarded $\overline{LC}$ inputs of the receivers used. Refer to the individual receiver data sheets for detailed specifications.

The critical parameters in the circuit of Figure 9 are good line balance, low insertion loss, and light line loading. These are easily achieved with the Teltone M-927 receiver and M-949 balanced line sense relay. The M-949 is energized by the flow of loop current which results when a caller goes off-hook. This drives the M-927's $\overline{LC}$ input true and enables the receiver to

detect dialed digits. Tying the STROBE output to the DTI and RDI inputs as shown causes the receiver to recognize only DTMF digits or only pulse digits, depending on the type of digit first received. When loop current is lost and the M-949 is de-energized for a prescribed duration, the receiver recognizes on-hook and returns to idle. The signal input of the M-927 is AC coupled and will tolerate AC, DC, and impulse voltages. The M-949 has a minimum of 63 dB balance and provides 1500 volts isolation from line to relay contact. In the United States, the use of these parts allows registration under Federal Communications Commission (FCC) regulations.

If the application is less demanding, the circuit of Figure 10 may be suitable. Here a standard telephone set is powered by a 12 VDC supply isolated by two resistors. Across one resistor is a transistor which turns on when the telephone is taken off-hook and turns off when the telephone is put on-hook. The transistor drives the Teltone M-917's $\overline{LC}$ input, which operates identically to the M-927's relay-driven $\overline{LC}$ input in Figure 9.
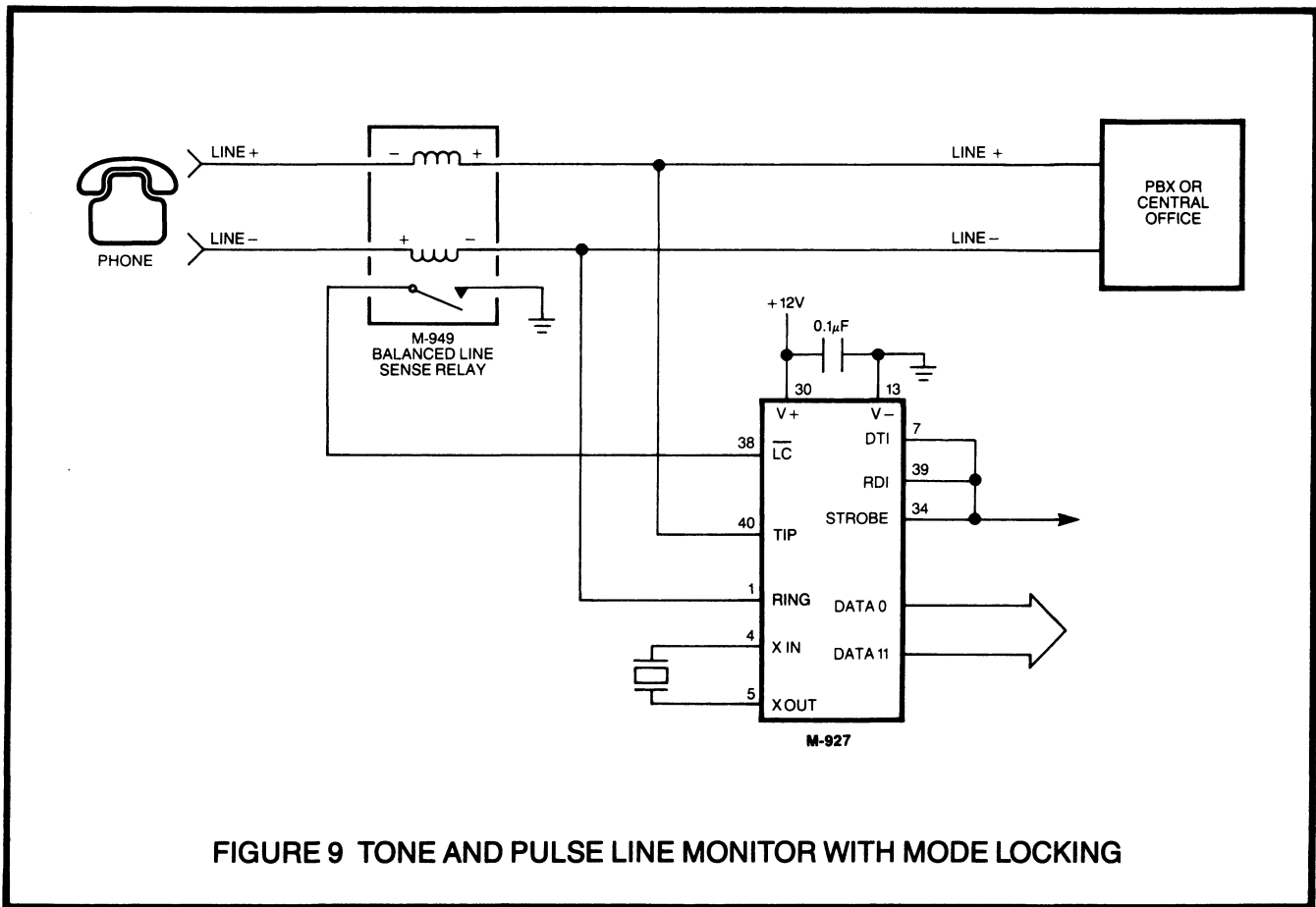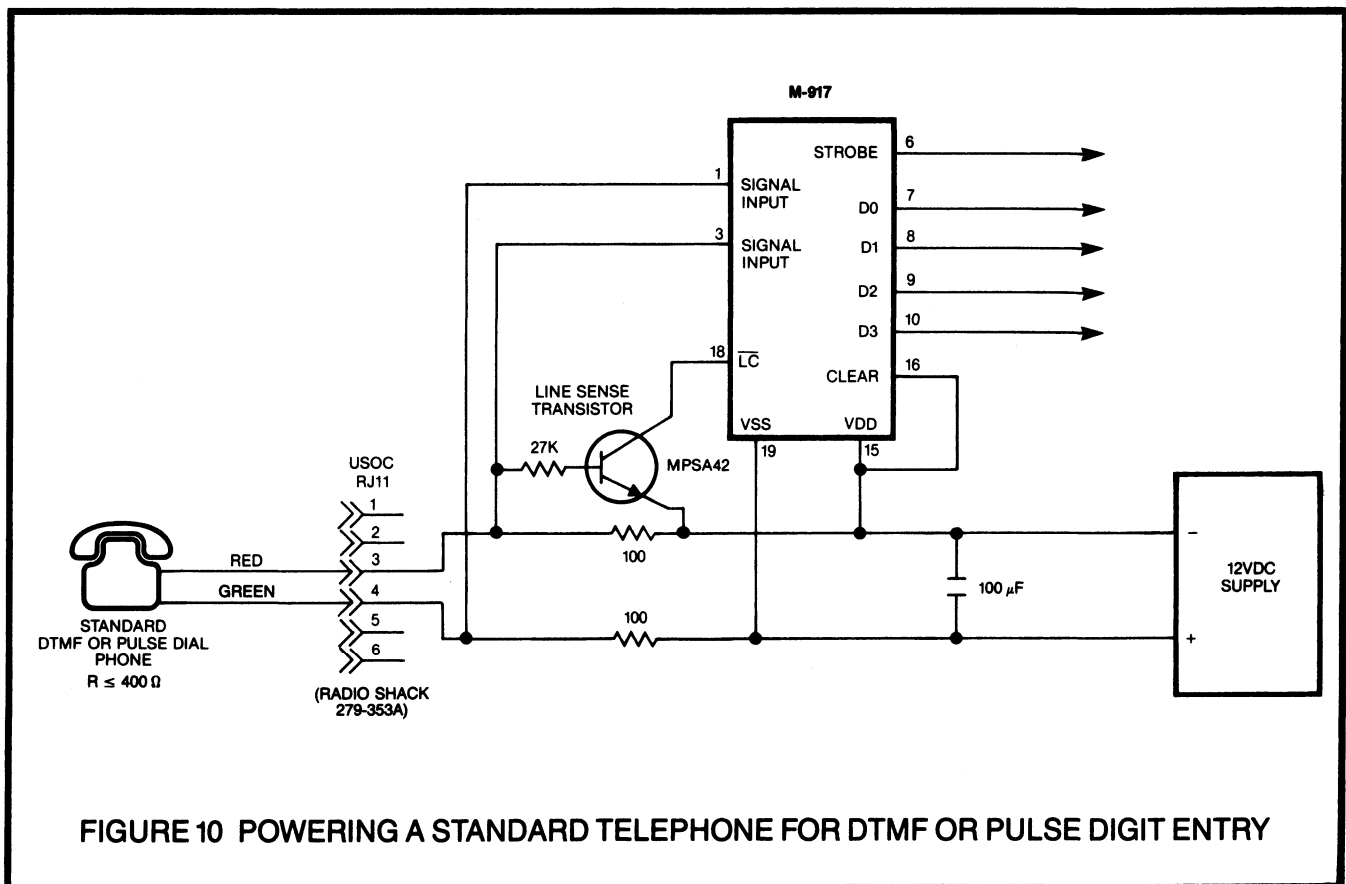

FIGURE 9 TONE AND PULSE LINE MONITOR WITH MODE LOCKING

FIGURE 10 POWERING A STANDARD TELEPHONE FOR DTMF OR PULSE DIGIT ENTRY

DETECTING SIGNALS AT THE CALLED STATION

It is often useful to be able to dial up a remote station, have the call be answered automatically, and then transmit data using either the DTMF keypad on the telephone or an acoustic DTMF generator. Figure 11 shows a typical circuit for detecting ringing voltage and answering the line, while Figure 12 shows a typical circuit for retransmitting received data.

In Figure 11, the application of ringing voltage to the telephone line causes the neon isolator to fire, driving the M-927's $\overline{LC}$ input true. This in turn drives the M-927's OFF-HOOK output false, which energizes the seize relay and permits DC current to flow, thereby answering the call. Digits dialed by the caller can then be received and decoded. The flow of DC current is maintained by the hold coil, while AC impedance is maintained by a 600-ohm resistor, in series with a capacitor, across the line. Note that the polarity of the CO voltage is important, so a diode bridge should be

used if polarity reversals can occur. While the seize relay is energized, an LED opto-isolator monitors the flow of loop current. If loop current is lost for more than 300 milliseconds, due to either the caller's going on-hook or a command on the line shown as $\overline{HANG\ UP}$, the system returns to idle until ringing voltage is applied again. The telephone line connector shown is the United States standard RJ11, but could be any type. Protection from common mode or differential line transients is provided by metal oxide varistors (MOV's).

Receivers such as the Teltone M-947 are constructed to use "single-ended" signals, which appear with reference to ground only. Such receivers are easily connected to balanced lines using either of the input circuits shown in Figure 12. The M-947's output is shown converted to a 7-bit ASCII format for asynchronous transmission on an EIA RS-232-C (CCITT V.24) line. Specific types of PROM's and UART's are indicated, but devices from other manufacturers could also be used.
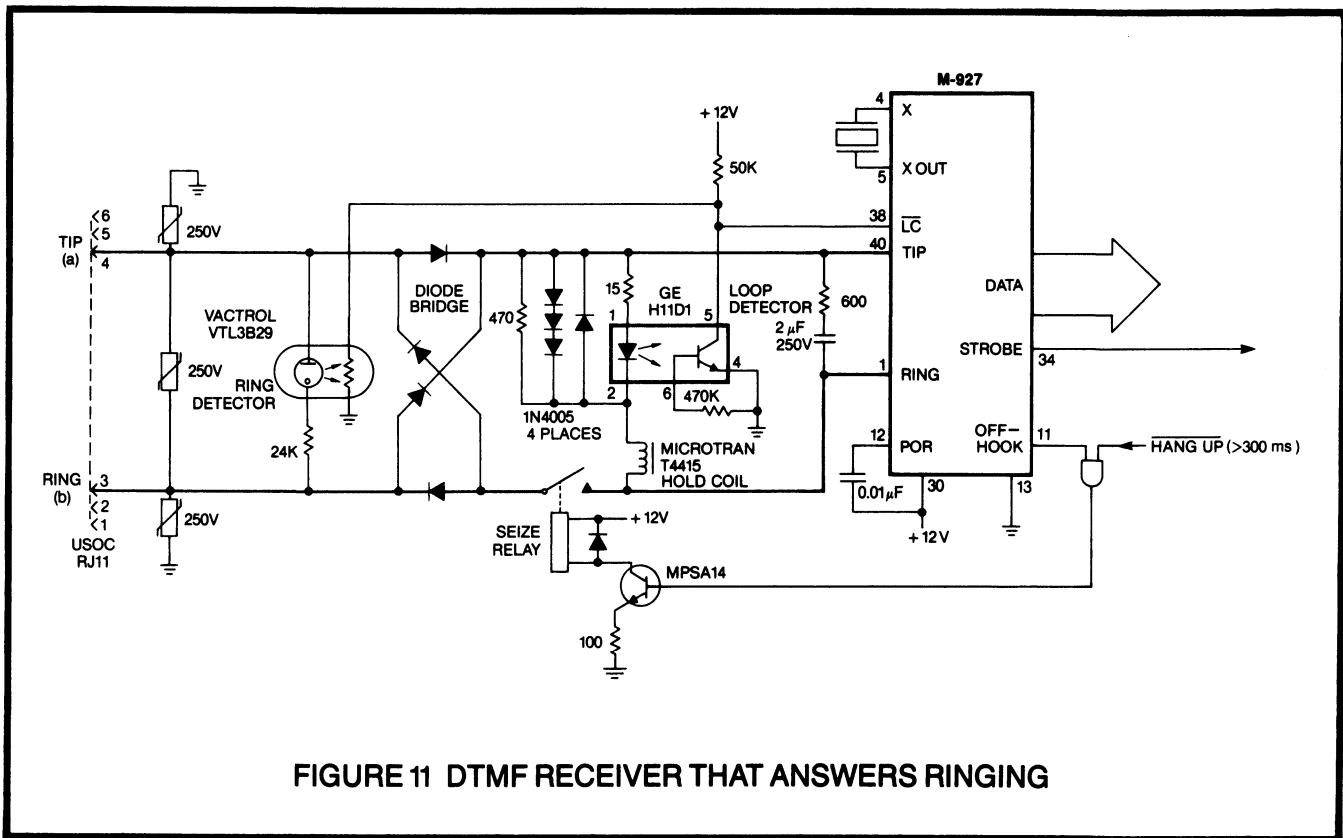
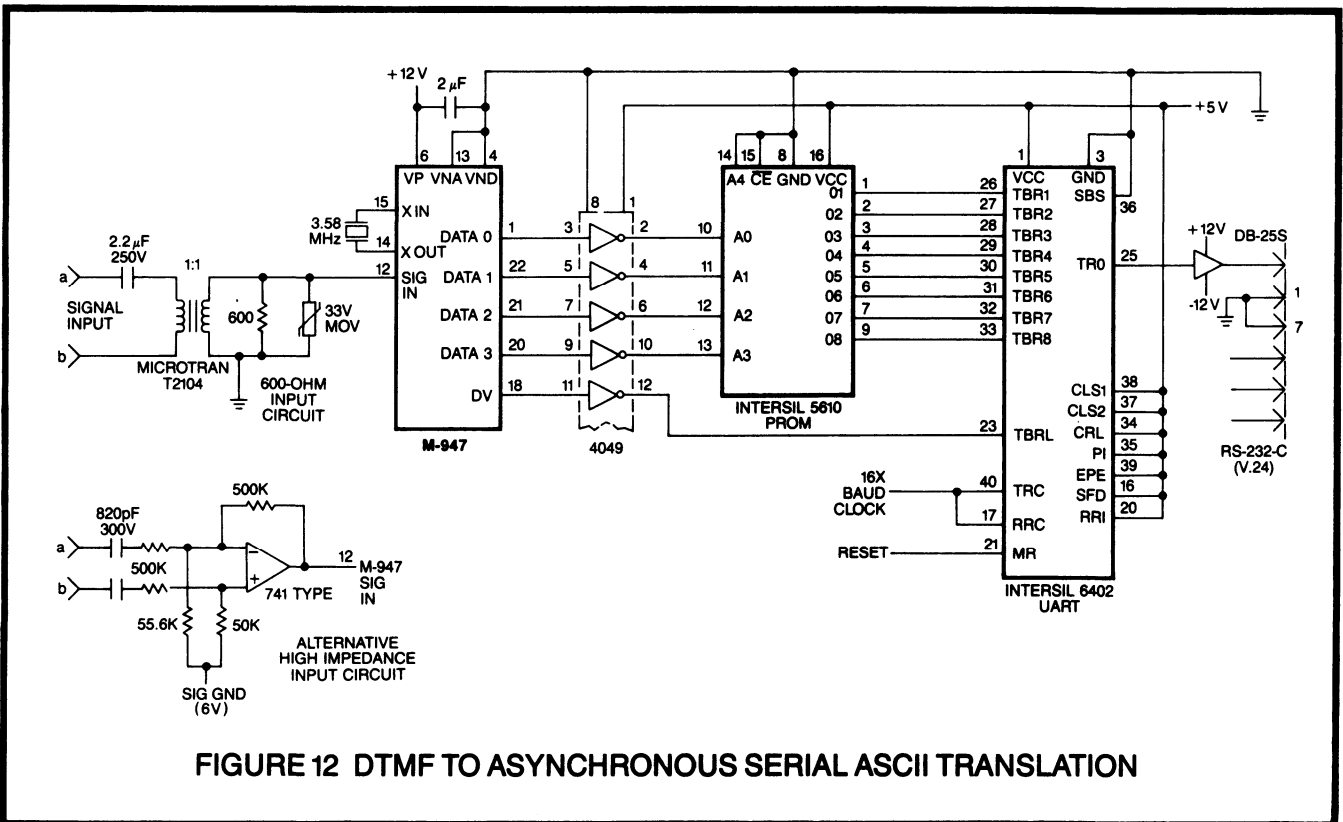FIGURE 11 DTMF RECEIVER THAT ANSWERS RINGING

FIGURE 12 DTMF TO ASYNCHRONOUS SERIAL ASCII TRANSLATION
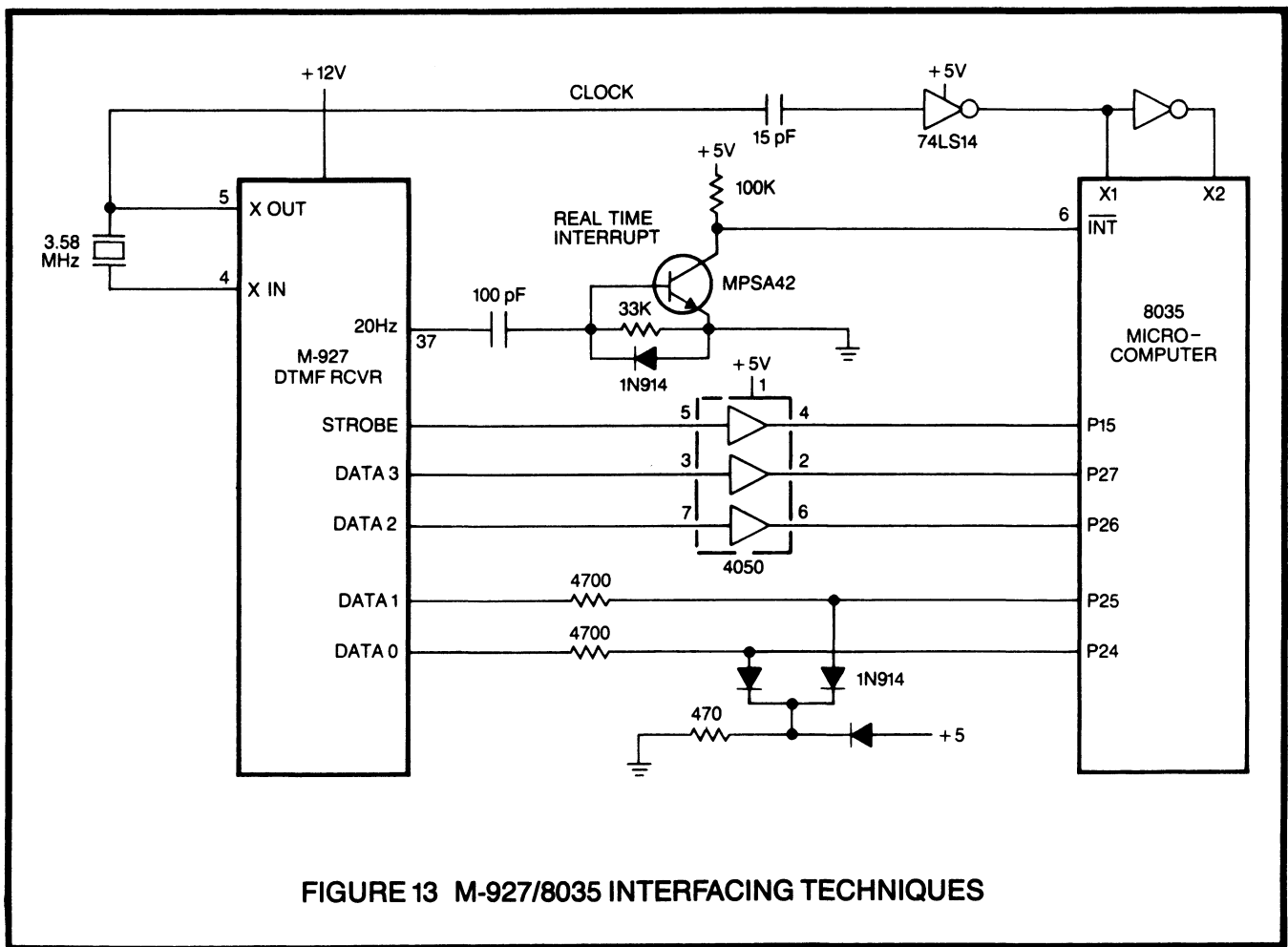
INTERFACING TO OTHER CIRCUITS

One of the challenges presented to digital designers is inexpensive interfacing to IC's outside the popular standard logic families. Problems are presented in the form of power supplies, inconvenient pinouts, or complex control functions. Fortunately for designers, the Teltone family of DTMF receivers was configured with flexibility and ease of use in mind. Here are some shortcuts and interfacing techniques that can simplify your design and help make it more cost-effective.

Figure 13 presents various ideas for interfacing a 12-volt M-927 receiver with a popular 5-volt, single-chip microcomputer, the 8035. The 3.58 MHz clock oscillator in the receiver can be used to drive the processor clock, once again eliminating a crystal. A "real-time" clock is also possible using one of the M-927's three clock outputs to provide a narrow INT pulse at each rising edge of the square wave. CMOS 4049 or 4050 IC's are a particularly inexpensive and easy way to

translate 12-volt logic to 5-volt logic, but diodes and resistors will also work.

Figure 14 shows how one crystal-connected M-927 or M-947 can be used to drive the time bases of additional receivers. Use of this technique reduces the parts count and increases system density in multi-receiver applications.

Figure 15 shows how a simple hardware DTMF digit repeater can be made using the 2-of-8 mode output of the M-927. Once again, CMOS 4049 and 4050 IC's provide cost-effective voltage translation. The M-927 "pushes the buttons" on the Mostek MK5087, regenerating the DTMF tones without the noise, frequency deviation, and twist they arrived with. The lower supply voltage of the 5087 is provided by a zener diode regulator. Other keyboard-compatible products like pulse dialers could be used similarly to provide DTMF-to-pulse translation very inexpensively.

FIGURE 13 M-927/8035 INTERFACING TECHNIQUES

FIGURE 14 CASCADING CLOCKS FOR M-927 AND M-947

FIGURE 15 PULSE TO DTMF CONVERTER AND DTMF REPEATER

SPECIAL APPLICATIONS

An interesting feature of sampled-data signal processors is that their characteristics change when their clock rates change. Applications of this phenomenon can be seen on this page.

In Figure 16, a Mostek 5087 DTMF generator and a Teltone M-947 DTMF receiver are operated with 4.43 MHz European color burst crystals instead of the specified 3.58 MHz North American color burst crystals. The higher clock rate causes the generator's output tones to be higher in frequency and the receiver's recognition frequencies to be shifted by about the same

proportion. The overall effect is to provide tone signalling at higher frequencies than the standard DTMF assignments, shifting the digits and yielding a private code.

Frequency shifts work in the other direction too, as shown in Figure 17. By lowering the basic clock rate to 1.315 MHz, an M-927 can be used to detect North American "precise" dial tone (350 Hz plus 440 Hz) which is decoded as "*" or a logic 0 on the DATA 10 pin. Similarly, a 1.315 MHz crystal attached to the MK 5087 yields a very close approximation of precise dial tone.
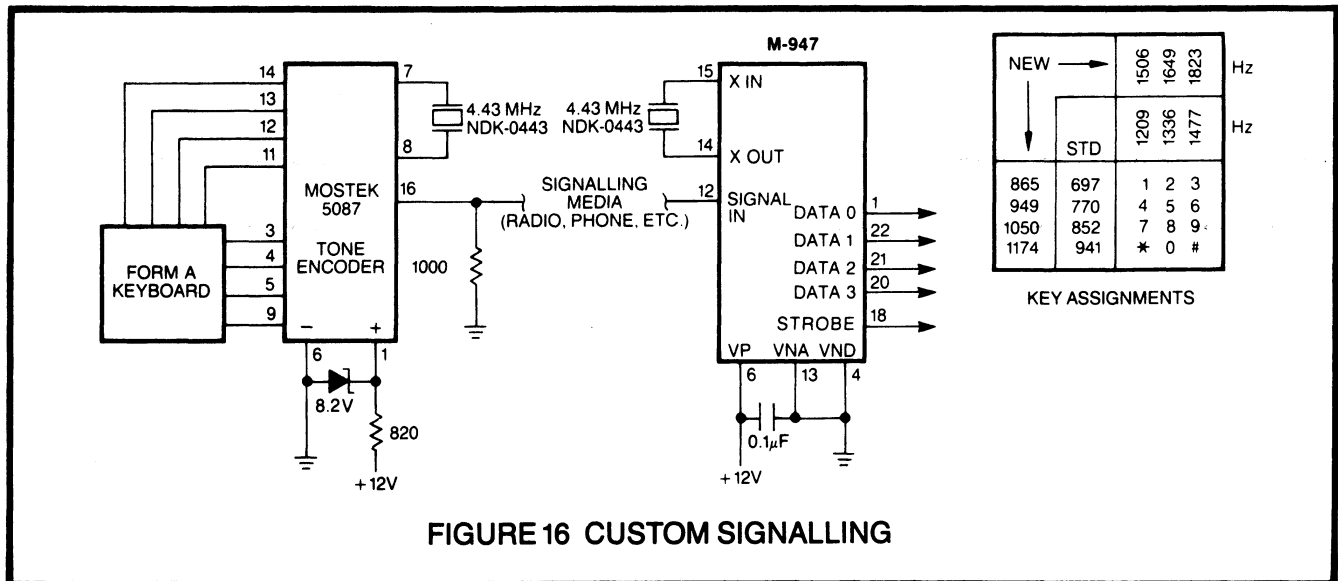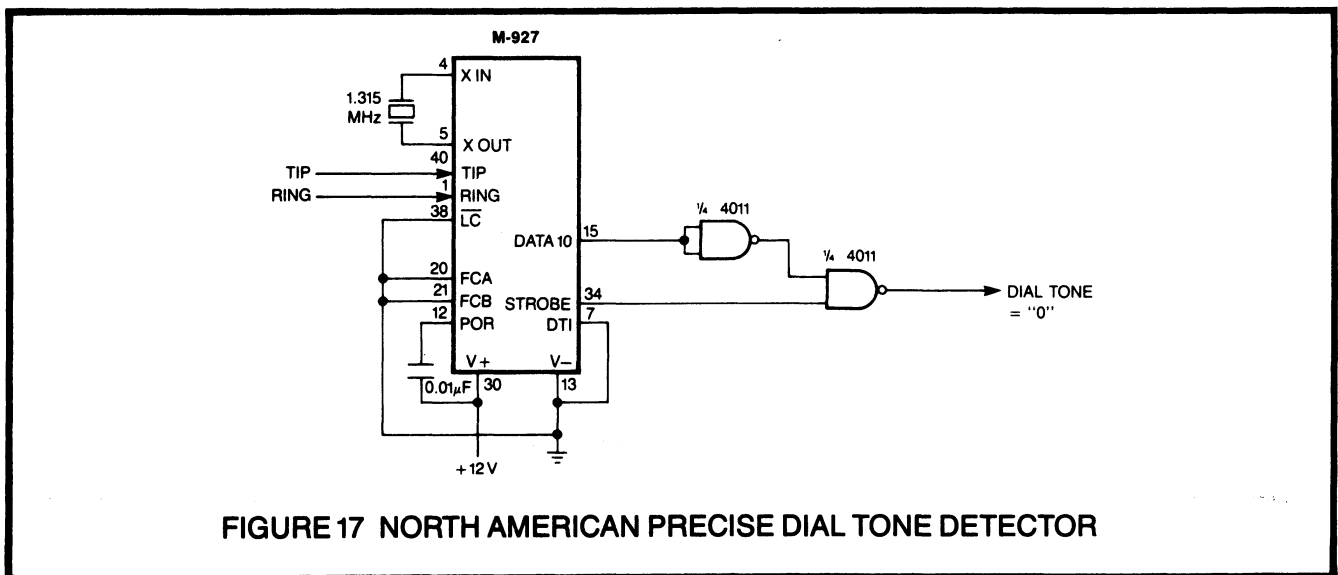

FIGURE 16 CUSTOM SIGNALLING

FIGURE 17 NORTH AMERICAN PRECISE DIAL TONE DETECTOR

REGULATORY AGENCY REQUIREMENTS

Most countries have agencies whose purpose is to regulate the use of the public telephone network. These agencies require that certain technical specifications be met before equipment can be registered for connection to the network. In the United States, the regulatory agency is the Federal Communications Commission (FCC). Figure 18 shows the process used to secure registration under FCC Rules, Part 68.

Although requirements vary from country to country, and from one class of equipment to another, they have in common many elements which should be considered when designing telephone equipment. If your application is regulated, consider the specific requirements in each country from the list of parameters on the following page. Actual numbers for each requirement are supplied in documents available from British Telecom in the United Kingdom, Bundespost in West Germany, AT&T or the FCC in the United States, NTTPC in Japan, and the various Ministries of Transport, Posts, or Telephone and Telegraph in many other countries.
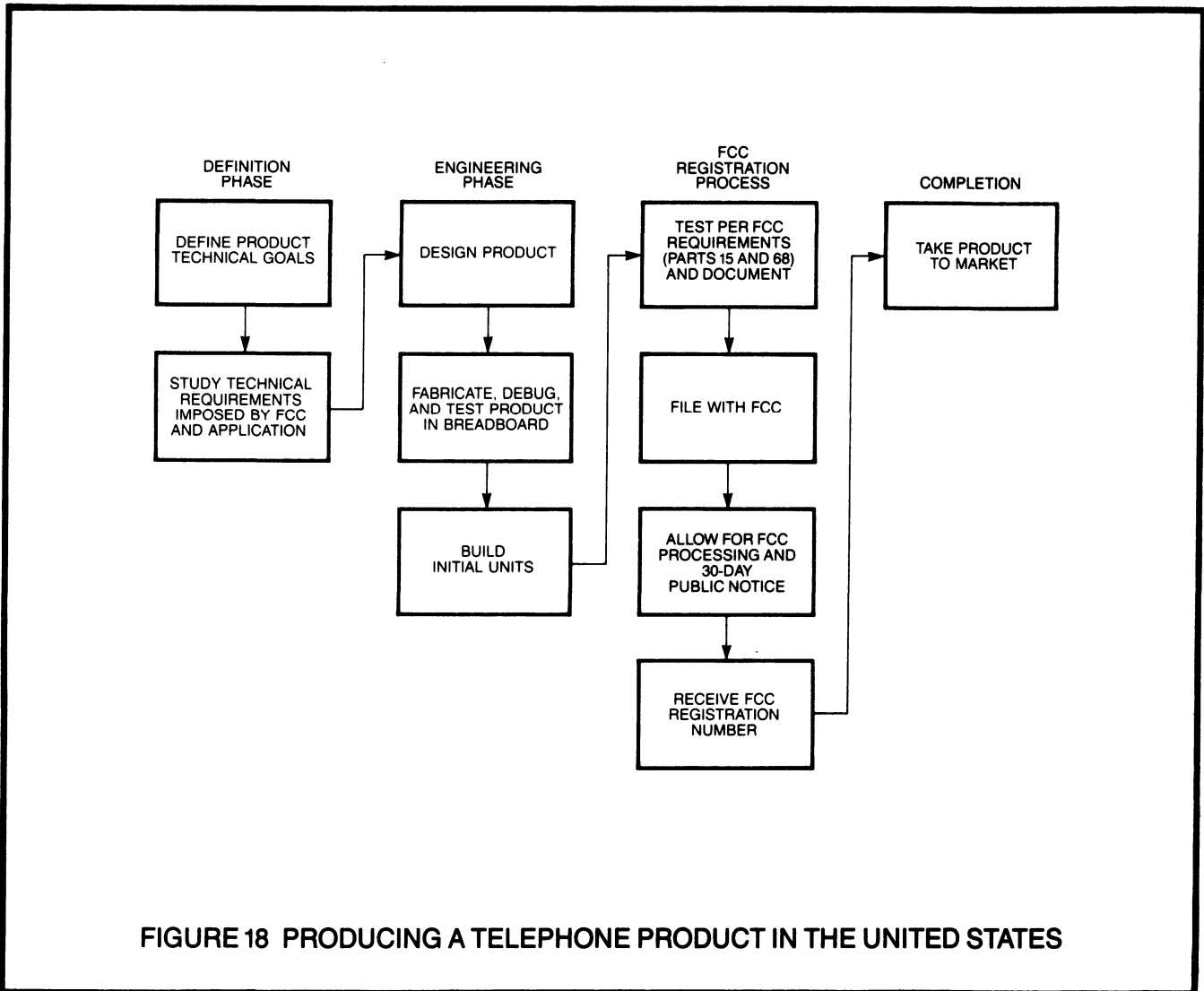
DEFINITION PHASE

DEFINE PRODUCT TECHNICAL GOALS

STUDY TECHNICAL REQUIREMENTS IMPOSED BY FCC AND APPLICATION

ENGINEERING PHASE

DESIGN PRODUCT

FABRICATE, DEBUG, AND TEST PRODUCT IN BREADBOARD

BUILD INITIAL UNITS

FCC REGISTRATION PROCESS

TEST PER FCC REQUIREMENTS (PARTS 15 AND 68) AND DOCUMENT

FILE WITH FCC

ALLOW FOR FCC PROCESSING AND 30-DAY PUBLIC NOTICE

RECEIVE FCC REGISTRATION NUMBER

COMPLETION

TAKE PRODUCT TO MARKET

FIGURE 18 PRODUCING A TELEPHONE PRODUCT IN THE UNITED STATES

REGULATED SYSTEM PARAMETERS

Line Isolation—For safety reasons, telephone equipment must endure application of high level DC, high-level low-frequency (50-60 Hz) AC, and impulse voltages to lines connected to the public network. The application of these voltages must not cause hazardous voltages or currents to appear where they can present a danger to people or to other equipment.

Longitudinal Balance—Telephone lines connected to equipment should not have impedance differences created by the equipment which will cause common mode or longitudinal voltages to produce undesired differential voltages. This usually results in "hum" or other forms of interference from nearby sources of electrical noise. Careful balancing of line components is usually required.

Critical AC Levels—Each type of telephone equipment will probably have limits or ranges specified for AC signal levels, both generated and received, when the circuit is active.

On-Hook Impedances—To prevent interference with equipment on the same circuit and to limit loads imposed on ringing generators, the "on-hook" or idle resistances to certain AC and DC voltages usually have minimum values.

Off-Hook Impedances—To meet transmission design goals and to prevent interference with equipment on the same circuit, most regulatory agencies require that AC and DC impedances fall in specific ranges when equipment is in the "off-hook" state.

Special Frequency Assignments—Many telephone systems generate signals that can interfere with your device, and your circuit may generate signals that have a negative effect on other equipment. These frequencies are listed in the pertinent specifications.

Critical Interface Timing—Circuit events in telephone systems are usually expected at specific times. Timing for events like signal delays, pulse widths, hold times, and control intervals are detailed by regulatory agencies when necessary.

EVALUATING DTMF RECEIVER PERFORMANCE

Deducing the performance of a DTMF receiver from its data sheet is no substitute for actual field trials or an in-depth evaluation in the laboratory. Figure 19 shows a test circuit similar to that used by Teltone for its own evaluations. This circuit allows the user to vary independently the level and frequency of each DTMF signal component, to control tone burst length and interval, and to inject different types of interfering signals.

Using this circuit, Teltone tests for errors in detection under worst-case conditions: the signal persisting for minimum duration, at extremes of frequency, twist, and dynamic range. For example, the Teltone M-947 was found to have an error rate of 1 in 10,000 when operated in the continuous presence of 0 dBm per tone precise dial tone, with the DTMF tone burst duration and interval 40 milliseconds, both DTMF frequencies offset in all possible combinations of ± (1.5% + 2 Hz),

10 dB twist, and the signal level at either −24 dBm or +6 dBm. This is similar to test methods used by the United States Independent Telephone Association (USITA), Electronic Industries Association (EIA), and American Telephone and Telegraph (AT&T).

The only detection tests used by Teltone that are not done under worst-case conditions are those related to tolerance to Gaussian or random noise. In these tests the DTMF tone burst duration and interval are 50 milliseconds, the frequencies are at nominal, twist is zero, and the signal level is A plus 5 dB.

To test speech immunity, Teltone uses side two of the Mitel CM 7291 test tape. The results should be used for comparative purposes only, and should consist of ten plays of the test, throwing out the highest and the lowest numbers of detections and averaging the other eight. Teltone cannot recommend the other tests on the Mitel tape for use in evaluation of receiver designs.
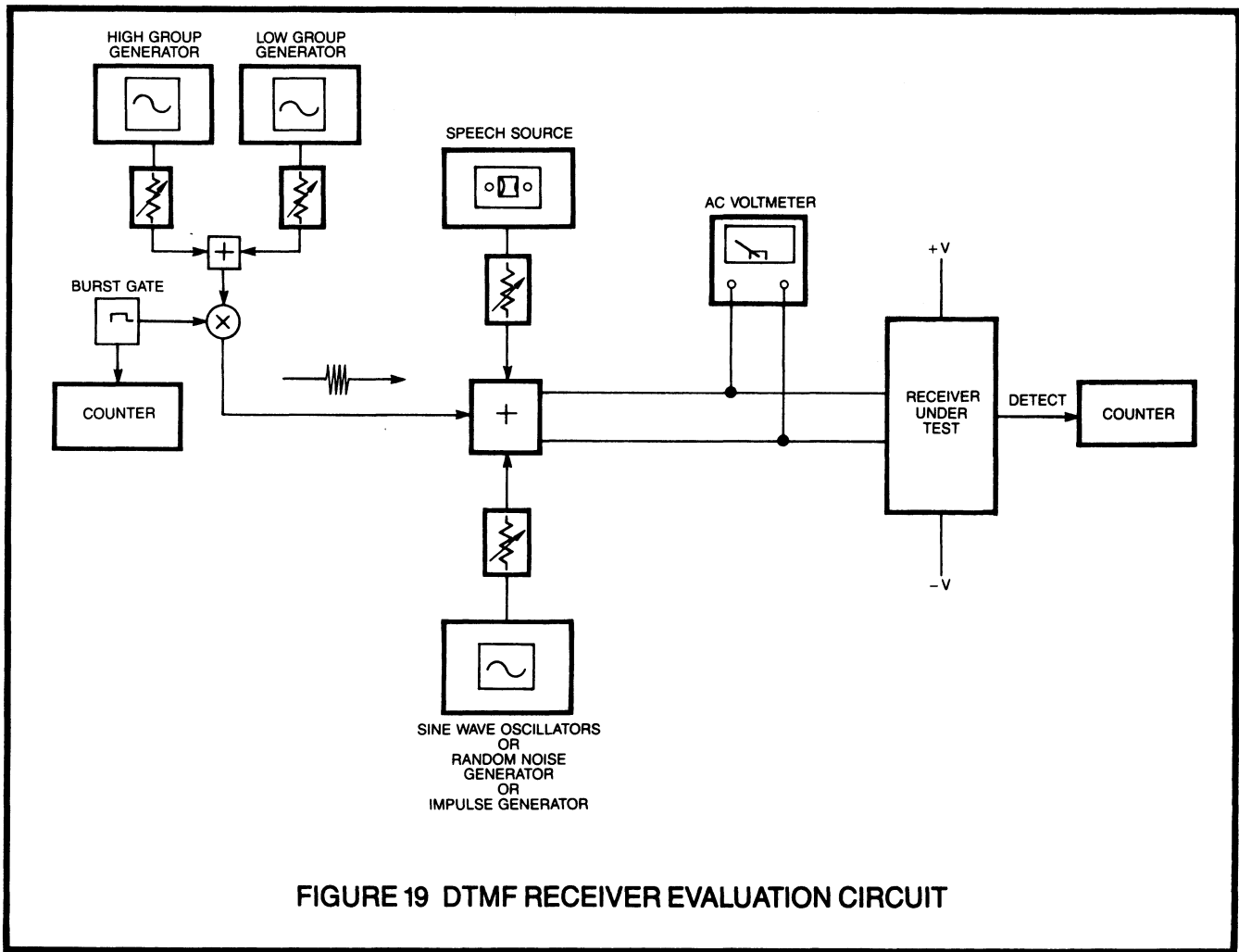
FIGURE 19 DTMF RECEIVER EVALUATION CIRCUIT

TABLE 1 TELTONE STANDARD DTMF FREQUENCY SKEW VALUES

−3.5%	−1.5% −2 Hz	NOMINAL	+1.5% +2 Hz	+3.5%
673	685	697	709	721
743	757	770	784	797
822	837	852	867	882
908	925	941	957	974
1167	1189	1209	1229	1251
1289	1314	1336	1358	1383
1425	1453	1477	1501	1529
1576	1607	1633	1659	1690

SOURCES OF INFORMATION

Teltone DTMF receivers have been used in central office, PBX, and subscriber telephone equipment for over ten years. In designing our receivers to meet the stringent signalling requirements imposed by these applications, we have found the following to be particularly valuable sources of information on telephony and telecommunications.

NORTH AMERICA

- *AT&T Publications Catalog PUB 10000*

   Publisher's Data Center Inc.
   PO Box C738
   Pratt Street Station
   Brooklyn, New York 11205

- *GTE Technical Interface Manual for Customer Equipment CHB-500*

   Engineering Practices and Support
   GTE Automatic Electric
   400 N. Wolf Road
   Northlake, Illinois 60164

- *Private Branch Exchange Switching Equipment for Voiceband Applications RS-464*

   Electronics Industries Association
   Engineering Department
   Standards Orders
   2001 Eye Street, NW
   Washington, DC 20006

- *Certification Standard*

   Telecommunications Regulatory Service
   Department of Communications
   Terminal Attachment Program
   300 Slater Street
   Ottawa, Ontario K1A 0C8
   Canada

WORLDWIDE

- *The Orange Book*

   International Telegraph and Telephone Consultative Committee (CCITT)
   International Telecommunication Union
   1211 Geneva 20
   Switzerland

- *Various Standards*

   Conference of European Postal Telecommunications Administrations (CEPT)

PHYSICAL UNITS IN TELEPHONY

In telecommunications engineering it is useful to express signal power as a ratio of the power to some reference. The units are decibels (dB) determinined by the formula

$$dB = 10 \, LOG_{10} \, (P/P_R)$$

where P_R is the reference power. This reference power varies from use to use and is indicated by a letter appended to *dB*. The most common form is *dBm*, where *m* indicates that the reference power is one milliwatt. Another common form is *dBrn*, which indicates that the ratio is calculated using reference noise of -90 dBm at 1000 Hz.

Because most electronic test equipment measures voltage, and because voltage is the key parameter for high-impedance signal processing circuits, it is necessary to relate voltage to power and voltages to one another. Ratios of voltages are expressed in dB according to the formula

$$dB = 20 \, LOG_{10} \, (V/V_R)$$

where V_R is the reference voltage. The form *dBv* is reserved to indicate a reference of one volt, while *dBV* is used for any other voltage.

When power is shown in dBm it is customary to include a load impedance, usually 600 ohms, which allows the power to be interpreted in volts. The graph in Figure 20 facilitates conversion between powers and voltages, assuming a load impedance of 600 ohms.
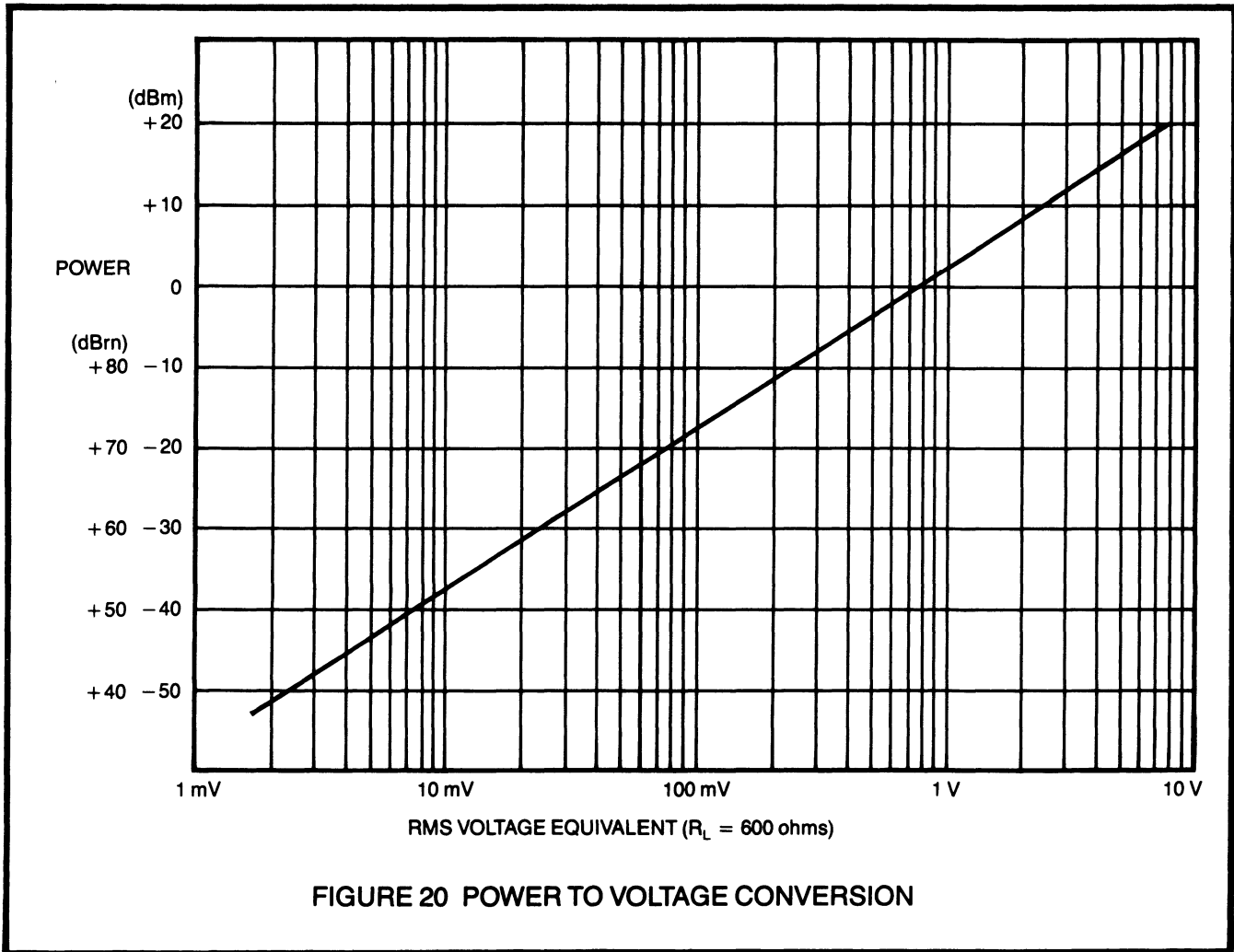

FIGURE 20 POWER TO VOLTAGE CONVERSION

GLOSSARY

a wire—see line +.

b wire—see line –.

CO—central office. A local switching center to which telephones are connected by means of telephone lines. See Figure 2.

dB—decibels.

dBm—decibels above or below a reference power of 0.001 watt in a 600-ohm resistance (0 dBm equals 0.78 volts).

dial tone—a signal sent to a calling telephone indicating that digit dialing may begin. It usually consists of one or two tones between 350 Hz and 480 Hz. See precise dial tone.

DTMF—dual tone multifrequency. A signalling system used with pushbutton telephones in which the two frequencies composing each signal are taken from two mutually exclusive frequency groups of four frequencies each. See Figure 6.

end-to-end signalling—the use of DTMF signals to perform access and control operations from a remote location.

F—farads of capacitance.

FCC—Federal Communications Commission. The United States government agency which regulates the connection of equipment to the public telephone network.

hookswitch—the switch controlled by the telephone handset, which closes its contacts when the handset is lifted from its mounting and opens its contacts when the handset is replaced on its mounting.

Hz—Hertz.

line – —one of the wires constituting the voice pair of the telephone line, so called because of its connection to the negative side of the battery supply. Also called b or Ring.

line + —one of the wires constituting the voice pair of the telephone line, so called because of its connection to the positive side of the battery supply. Also called a or Tip.

max—maximum.

min—minimum.

off-hook—the condition which results when the telephone handset is lifted from its mounting, which causes the hookswitch to close its contacts and allows loop current to flow. See Figure 2.

on-hook—the condition which results when the hookswitch contacts are opened (for example, by replacing the telephone handset on its mounting) and loop current is prevented from flowing. See Figure 2.

precise dial tone—a North American standard tone consisting of 350 Hz plus 440 Hz. See dial tone.

PSTN—Public Switched Telephone Network.

pulse—a signalling system used with pushbutton or rotary dial telephones in which each digit consists of serial makes (connections) and breaks (disconnections) in the line connecting the telephone to the central office.

Ring—see line –.

rotary dialing—see pulse dialing.

telephone line—the wire loop which connects a telephone to a central office.

Tip—see line +.

toll network—the system of long-distance telephone lines available for use at a charge.

APPLICATIONS FOR THE M-980 CALL PROGRESS TONE DETECTOR

The Teltone M-980 is an 8-pin DIP IC signal detector that operates on energy in the frequency band of about 300 to 650 Hz. Its primary use is in the detection of status tones encountered during dial telephone calls.These tones include dial tone, circuits busy, audible ringing, station busy, and others. Call status is derived by examining the cadence of those tones—some of which are illustrated in Table 1.

Typical uses are shown in Figures 1, 2, and 3. Figure 4 shows a simple scheme for connecting the M-980 to a balanced telephone line.
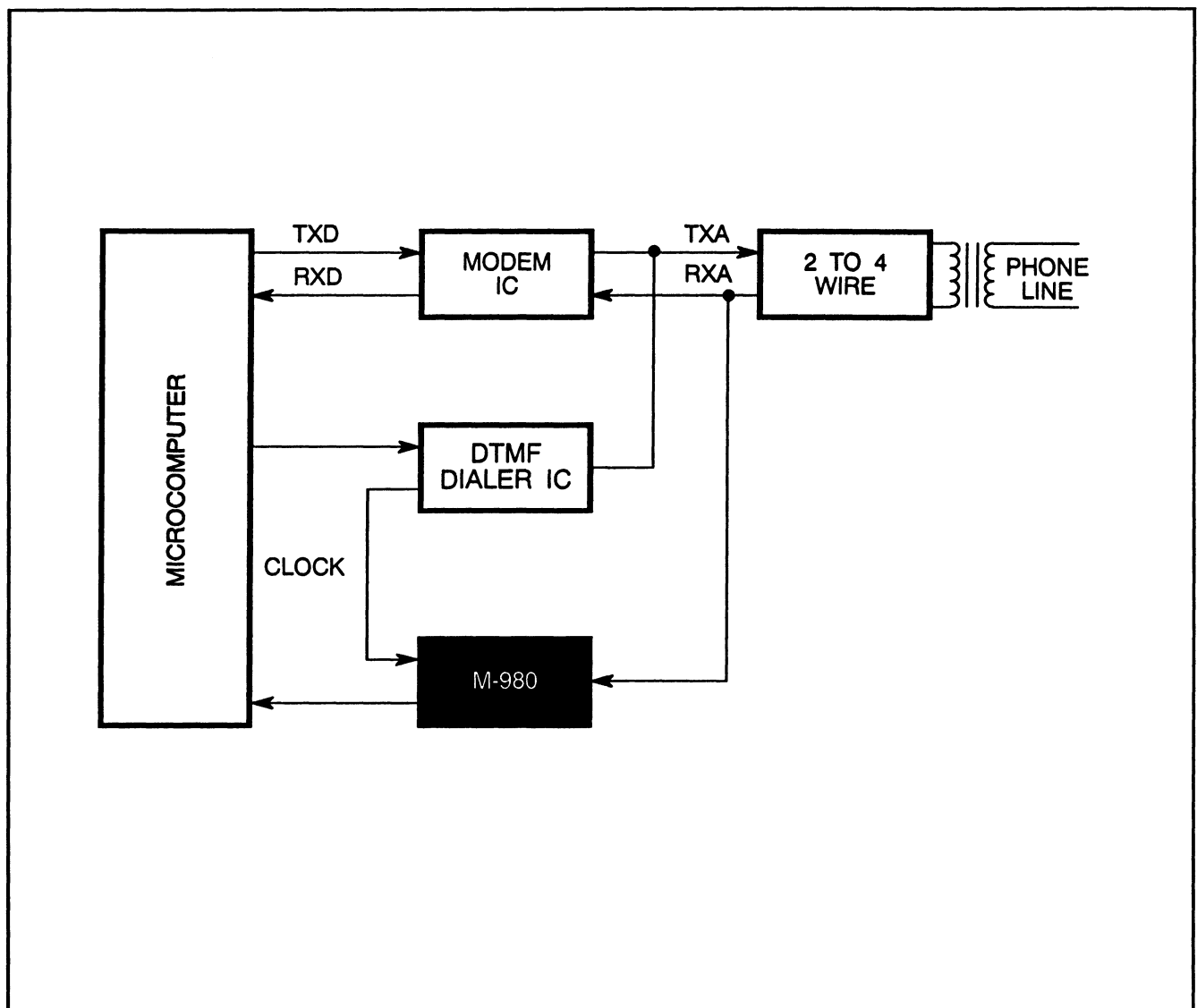
Figure 1   Detecting Dial Tone and Secondary Dial Tones in an Automatic Dialing Data Modem
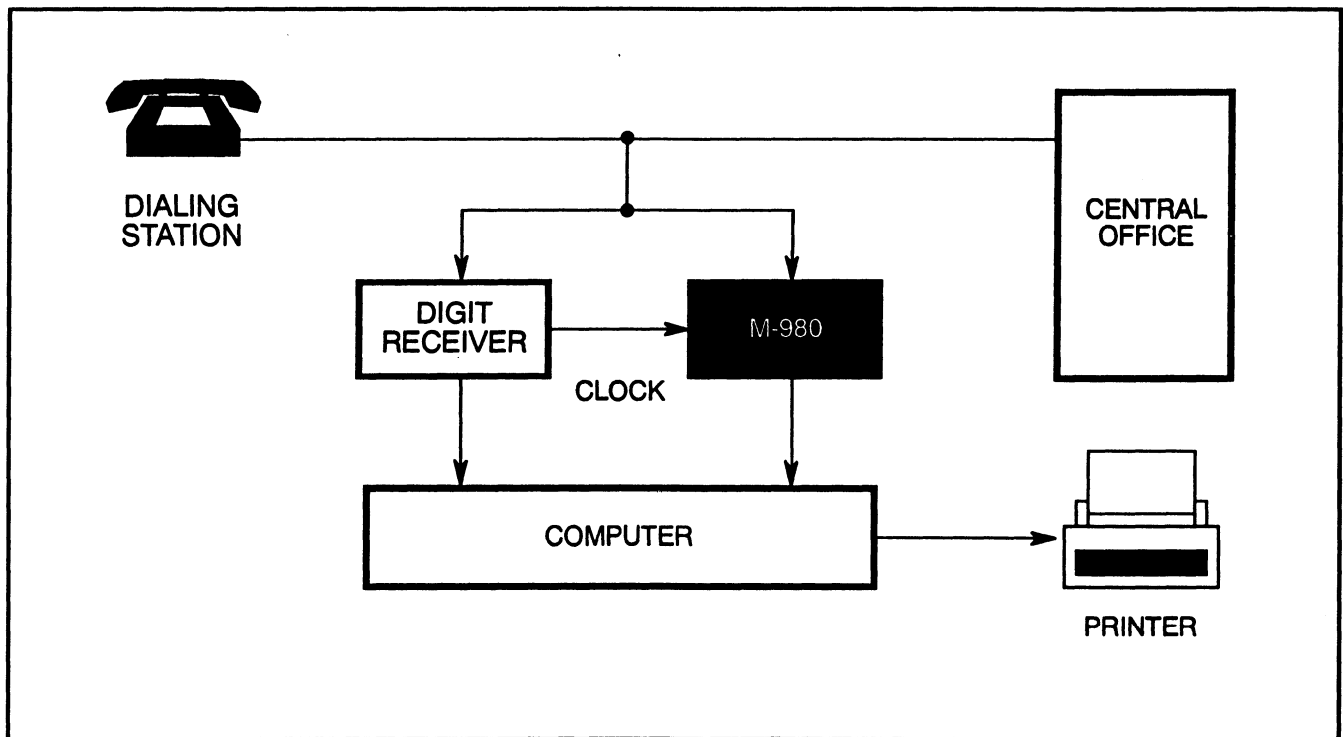
Teltone Corporation / 10801-120th Avenue NE, Kirkland, WA 98033   Phone: 1-800-426-3926 or 206-827-9626   Fax: 206-827-6050   TWX: 910-449-2862
Teltone Limited / 3375-14th Avenue, Markham, Ontario, Canada L3R 2L6   Phone: 416-475-0837   Fax: 416-474-9151   Envoy User Name: TTL.HQ

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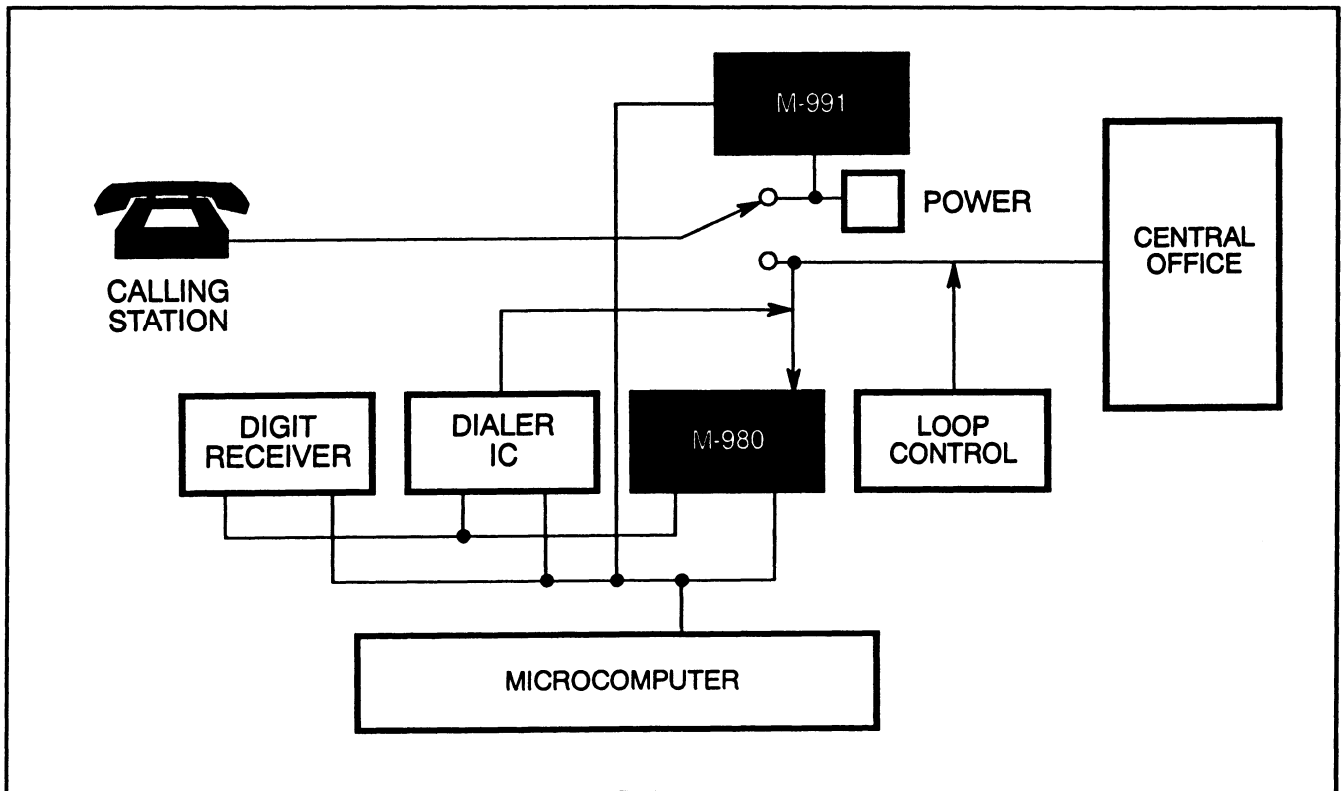**Figure 2 Call Detail and Completion Monitor in a Billing System**

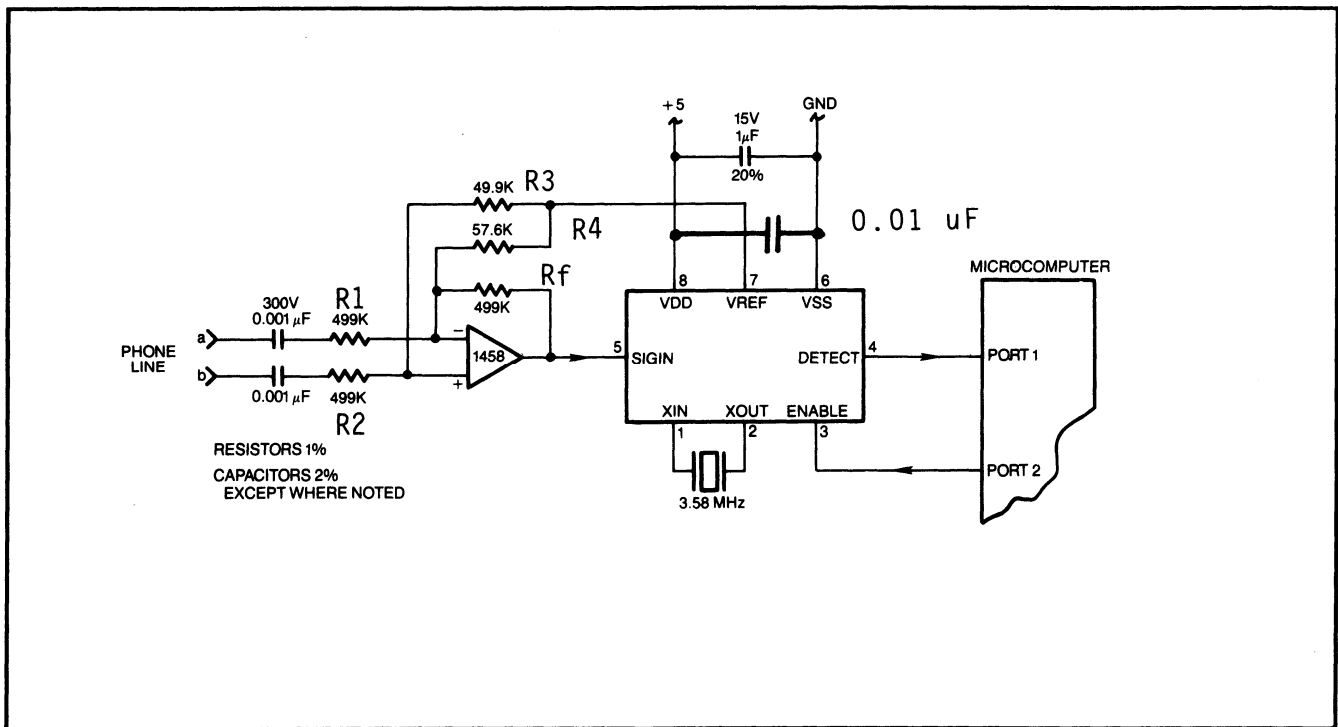**Figure 3 Call Routing in a Speed Dialing System**

Figure 4 Monitoring Signals from a Balanced Phone Line

NOTES: Rejection of common mode signals is enhanced by keeping the input network balanced—this means 1% resistors and capacitor values as closely matched as possible.

The dynamic range of the M-980 is very wide, making it very sensitive to power supply noise. Good high frequency bypassing is recommended.
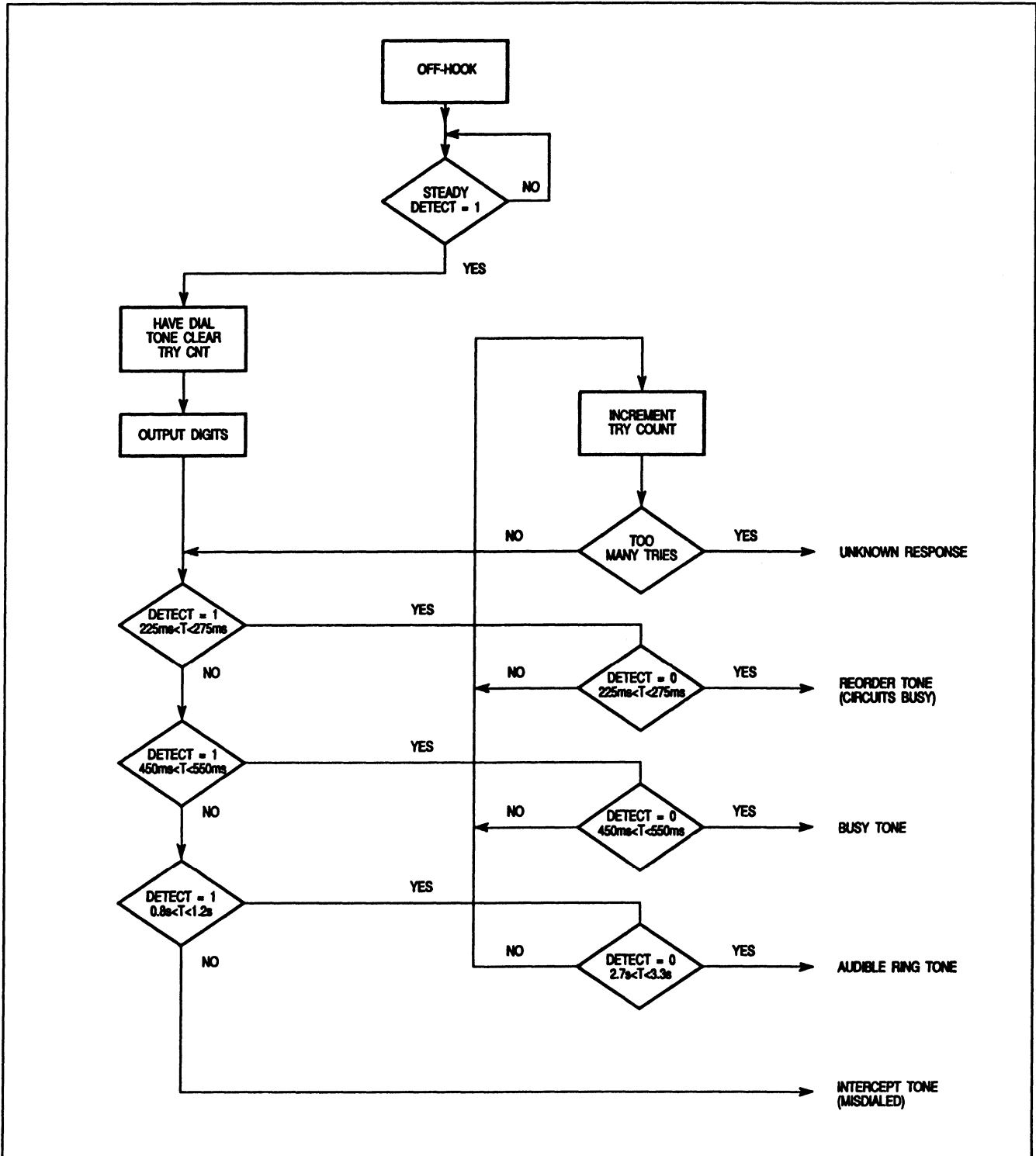
The basic sensitivity of the M-980 is -40 dBm, but in general it is best to use the least sensitive configuration possible to optimize transient response and to limit spurious DETECTs. The gain of the buffer stage shown above may be varied to obtain the sensitivity required for a given application. The gain of this stage is equal to the ratio of Rf to R1. When the value of Rf is changed from that shown above, R4 must be changed to keep the parallel combination of Rf and R4 equal to R3.

Table 1	Some Common Call Progress Tone Cadences and Frequencies
DIAL TONE	
Cadence	On, steady
Frequencies	400, 425, 350 + 440, 600 x 120, 33 Hz
AUDIBLE RING	
Cadence	2 sec on, 4 sec off, . . ., or 1/3 sec on, 1/3 sec off, 1/3 sec on, 2 sec off, . . .
Frequencies	400, 425, 440 + 480, 420 x 40, 450, 400 x 25 Hz
BUSY STATION	
Cadence	1/2 sec on, 1/2 sec off, . . .
Frequencies	400, 425, 480 + 620, 600 x 120, 450 Hz
REORDER (busy circuits)	
Cadence	1/4 sec on, 1/4 sec off, . . ., or 1/2 sec on, 1 sec off, . . .
Frequencies	400, 425, 480 + 620, 600 x 120, 450 Hz

Teltone Corporation / 10801-120th Avenue NE, Kirkland, WA 98033   Phone: 1-800-426-3926 or 206-827-9626   Fax: 206-827-6050   TWX: 910-449-2862
Teltone Limited / 3375-14th Avenue, Markham, Ontario, Canada L3R 2L6   Phone: 416-475-0837   Fax: 416-474-9151   Envoy User Name: TTL.HQ

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AN ALGORITHM FOR CALL PROGRESS FOLLOWING WITH THE M-980

The M-980 is a broad-band, general purpose call progress detector packaged in an 8-pin, monolithic integrated circuit. This application brief presents an example flow chart for determining the specific call progress signal encountered on the switched network by using period measurements.

Teltone Corporation / 10801-120th Avenue NE, Kirkland, WA 98033   Phone: 1-800-426-3926 or 206-827-9626   Fax: 206-827-6050   TWX: 910-449-2862
Teltone Limited / 3375-14th Avenue, Markham, Ontario, Canada L3R 2L6   Phone: 416-475-0837   Fax: 416-474-9151   Envoy User Name: TTL.HQ

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HANDLING MOS DEVICES

Static Discharge

Metal Oxide Semiconductor (MOS) devices have gained broad acceptance in telecommunications. This includes use of n-channel (NMOS) and p-channel (PMOS) transistors or both (complementary or CMOS)—most Teltone devices are fabricated using CMOS techniques but some use PMOS. In any case, MOS circuits require special attention in design and handling because of their susceptibility to damage through buildup of static charges and the currents that occur during discharge.

Whether alone or mounted in circuit boards, MOS ICs are subject to buildups of static charges and damaging discharges. Voltage of several hundred volts can affect these devices, while one or two thousand volts will certainly cause harm. Five hundred volts can easily be generated by a person walking around or moving in a chair, and thousands of volts can be generated by the simple act of pulling out and tearing off a piece of transparent tape.
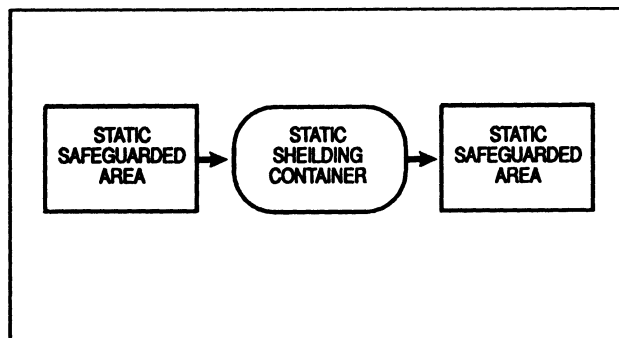
Under these circumstances, precautions must be taken to limit the potential for damage to costly IC devices. MOS ICs should be handled in static-protected or "safeguarded" areas. Such areas include ionized air flow over nonconducting surfaces. When not in these areas, ICs should be kept in static shielded containers. ICs must be handled in safeguarded areas (receiving inspection, stores, assembly, and test) and, when moved from area to area, should be protected by shielded containers.

Failure to implement procedures of this sort or relaxation of procedures can result in loss of valuable parts, increased production fallout, and higher repair costs.

CMOS Latchup

Though all ICs are subject to static discharge damage, CMOS ICs can experience another kind of damaging event known as "latchup" or "SCR". In this case, large currents can flow through the part from the power supply, damaging transistors and interconnections. This occurs when currents are injected into the chip where they weren't intended, usually through an I/O pin which has been driven to a voltage outside the supply range by some external device or event. This phenomenon is equivalent to four-layer conduction as used in SCRs, where a semiconductor device is "turned on" by injecting a current into a trigger layer. The device stays "on" until voltage is removed. This is useful in SCR control circuits, but in the case of CMOS ICs they may (1) recover completely after power has been cycled, (2) recover but act very strangely, or (3) blow up completely.

Causes can be inadequate power supply filtering, transient protection, or coincidences of PWB track layout. Static discharge may also trigger latchup.

```
STATIC            STATIC            STATIC
SAFEGUARDED  →  SHEILDING  →  SAFEGUARDED
AREA            CONTAINER          AREA
```

THIRD TONE IMMUNITY AND THE M-957

The Teltone M-957 DTMF receiver is a monolithic CMOS IC that offers high-performance detection of DTMF tone symbols. In complex electronic designs of this type, certain performance criteria are established to match the needs of the user, such as rejection of interference and signaling level. The M-957 specifications were tailored to suit the great bulk of uses foreseen, but there are instances, of course, where additional circuitry can be added to change some characteristics of the device to better suit special requirements.

The M-957 has been designed with limited high-frequency reject filtering, making it possible for tones above the DTMF tone band to interfere with perfect transmission of DTMF tone symbols. While such tones are not normally encountered, there are situations where regulation or application demand increased immunity. Such an application is that found in some equipment used by CEPT (in the European Economic Community) members where specifications require specific signal-to-noise ratios as a function of interfering tone (third tone) frequency. An illustration of such a requirement can be seen in Figure 1. The typical performance of the M-957 is shown in overlay to illustrate the area targeted in this application, above 1800 Hz.

There are several approaches possible in this design, involving cost and degree of effectiveness. We will illustrate two here, one passive and one active circuit. Each technique has benefits and drawbacks—the passive circuit is cheap and simple but is a performance compromise, while the active filter approach provides good rejection but with a cost/complexity increase.
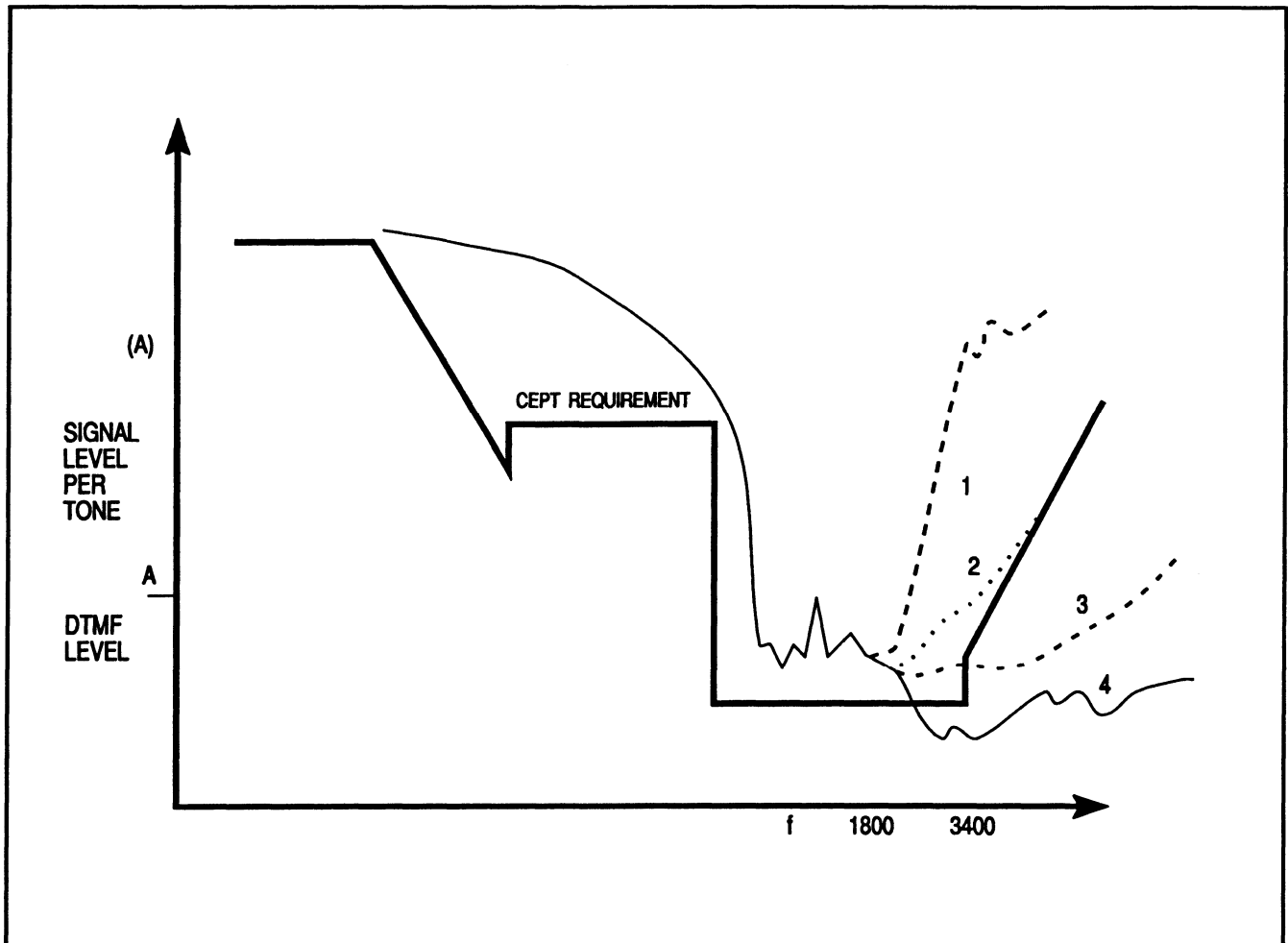

Figure 1   Tolerance to Interfering Third Tones

Circuit Techniques

Figure 2 shows schematic diagrams for both active and passive design, presenting two levels of complexity for the passive network. The curves of Figure 1 represent tolerance of a DTMF receiver to an interfering tone generally referred to as the third tone (beyond the two DTMF tones present). The goal established by the CEPT for some equipment types is shown along with the worst-case performance of the M-957, the signal being injected at point 4 of Figure 2. Tolerance to high-frequency interference is improved progressively as the test signal is injected at points 3 and 2, as can be seen. The passive RC network used is effective, but has some drawbacks in that the simple attenuation is 6 to 12 dB across the DTMF band. This adds 6 dB of twist and reduces the receiver's effective sensitivity, but the M-957 is highly twist tolerant, giving plenty of margin, and gain can be used to adjust for loss, either with the A and B pins or through external amplification.

The second approach shown uses the AMI S3528 Programmable Low Pass Filter IC to reject high frequencies. As seen in Figure 1, test signals injected at point 1 are filtered in such a way as to allow the M-957 to easily tolerate the tones as specified. Some IC connections to the S3528 are not shown for clarity (see the AMI MOS Products Data Book). Both schemes improve immunity to third tone interference, but do so with some reduction in speech immunity, though this part of the performance is still good.
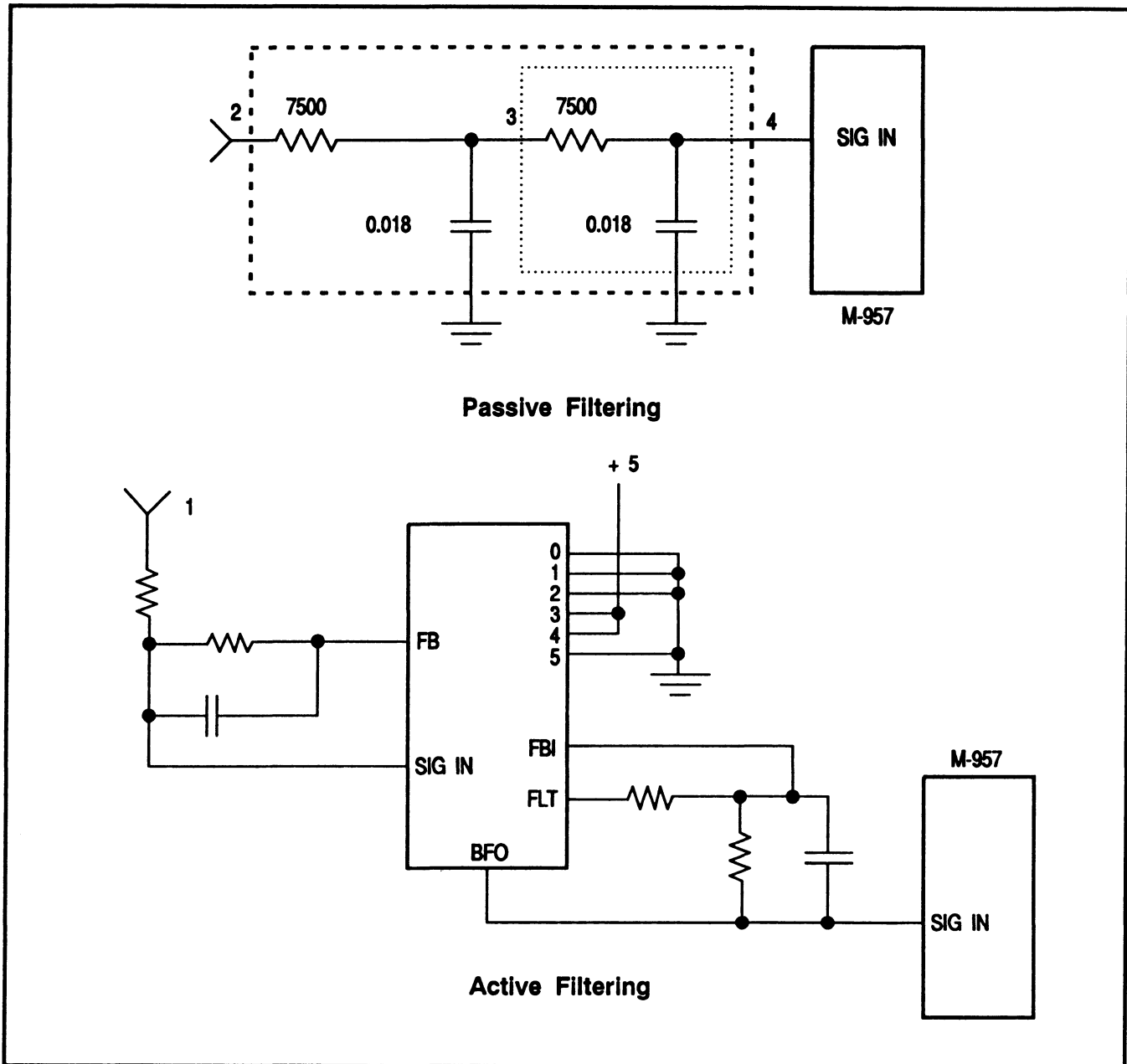

Passive Filtering

Active Filtering

Figure 2 Active and Passive Circuit Designs

COMPARING THE M-949 LINE SENSE RELAY TO OPTOCOUPLERS FOR LOOP CURRENT SENDING

An important function in telephone equipment designs is the sensing of "loop" current or current drawn from switching equipment by off-hook telephones. Presence of loop current alerts the switching equipment to the fact that the telephone is busy or requires service, and short interruptions or "pulses" are often used to signal dialed digits. Many schemes have been employed to do this current sensing, from Hall Effect and simple transistor circuits to relays and optocouplers. Each technique has advantages and drawbacks.

Loop sensing is part of quite a number of applications, both in the switching equipment and at the subscriber or station end. In the case of switching, as in central office or PABX, the classic service alerting and dialing functions are served. For station equipment like speed dialers or call accounting systems, loop sensing is important for monitoring lines and retrieving dial pulse digits. For either application, there are some basic characteristics required for any design solution. These are:

* Sense currrent from about 20 mA to about 125 mA
* Display line balance of 55 dB or better
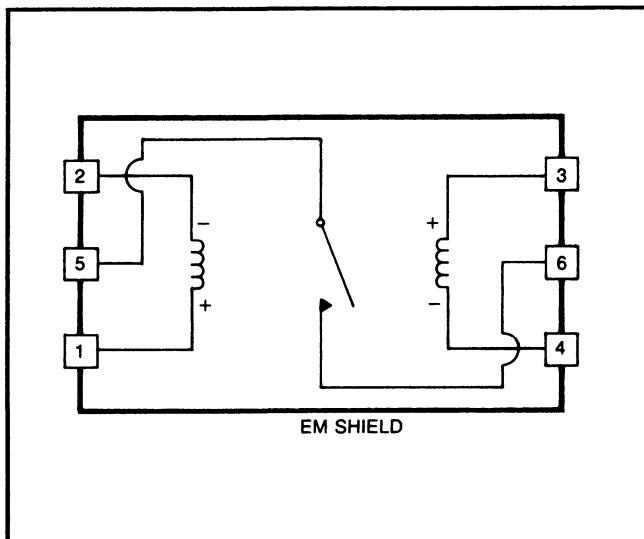* Provide isolation of the line from other circuitry

Solid-state optoisolators are often considered for such use, because the current requirement is at least as large as that needed for LEDs, and they generally offer electrical isolation enough for many applications. Teltone has developed an alternative to optoisolators for use in its own equipment that is now available for general use: the M-949 Line Sense Relay. The M-949 is a reed relay with some very special characteristics. The relay's two windings are used in series with the tip and ring (or a and b) wires and are wound in a way that puts one winding in aid of the field of the other when current flows in the loop. See Figure 1 for a schematic of the M-949, in comparison with an optoisolator. The windings are constructed in such a way that they provide the balance (63 dB minimum, over 70 dB typical), sensitivity (18 mA minimum), and isolation (1500 V for -01 and 3750 VAC for -02) demanded by telephone system applications. The 1FA or SPST contacts of the M-949 have current and voltage ratings far in excess of optical isolator output transistors.

Though optical couplers can be used in many applications, it is worth looking at the list of advantages and disadvantages shown below.

M-949 Advantages over Optoisolator

* The relay offers a continuous or "metallic" path through the device, a reliability factor over a semiconductor junction in series with the line.

* The relay doesn't suffer from the same voltage drop encountered with the opto, making it less likely to starve out line-powered equipment connected through the same line.

* The relay has a smaller hysteresis, causing less dial pulse distortion on long lines.

* Relays aren't subject to wide variations in current transfer ratios like optical semiconductors.

* No external components are required to set sensitivity limit current, or protect polarity.

Figure 1 M-949 Electrical Configuration

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- This relay can tolerate the high voltages and currents associated with use in series with coin phones.

- The relay can switch and withstand much higher voltages and currents at its output, with a life in the tens of millions of cycles.

- The relay is available in configurations difficult to emulate with optos—such as high voltage isolation, or creepage and clearance per IEC or VDE requirements.

- The relay is carefully specified for differential as well as common mode voltage withstand.

Advantages of Optoisolators over the M-949

- Optos are smaller.

- Different relay models are required for different sensitivities and voltage isolation ranges.

- Optos are sometimes cheaper.

CURRENT SOURCES OF INFORMATION ON BELL TECHNICAL STANDARDS

The continuing reorganization of the Bell System in the U.S. has caused some confusion about who is doing what, including technical standards and publications. A new organization has been formed by the Bell Operating Companies to provide the special skills and information they used to get from AT&T. This organization is known as Bell Communications Research (Bellcore), is located in New Jersey, and employs a number of former Western Electric, Bell Labs, and Long Lines people, among others.

Since designers and manufacturers in the telecommunications industry have lots of uses for the excellent information from this group, we thought we would bring you up to date on the whats and wheres of keeping current with Bellcore.

- Bellcore publishes a "Digest of Technical Information" monthly. Included are Bell Operating Company Purchasing contacts (part of the goal is to improve BOC/supplier communications), new technical publication titles, Technical Advisories open for comment, future releases, and noteworthy events from Bellcore or the ROC/BOCs. $35/year from:

    > Bell Communications Research
    > Information Operations Center
    > 60 New England Avenue
    > Piscataway, NJ 08854

- The Bellcore Documentation Hotline for the Digest, Catalogs, or information is (201) 699-5800. They take credit cards.

- The Catalog of Technical Information is a must. Number and address are the same as above. (Directory of listings)

- "Notes on the Network", 1986 release. T.R. (Technical Release) NPL-000275.

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TYPICAL CONNECTIONS FOR THE M-957 DTMF RECEIVER

The M-957 DTMF Receiver IC is a sophisticated signal processing device, but is relatively easy to use. As with most LSI devices, when first attempting to use it, it helps to have a cookbook circuit to get started.

Figure 1 illustrates a simple operating circuit for +5V supply (the M-957-01 may be used at up to 12V, while the -02 is designed for 5V only). Under the conditions shown, the receiver is sensitive from -2 dBm to -32 dBm, detects the 12 digits on a standard keypad, and gives a binary output that is active (not 3-stated). You will find that the sensitivity of the receiver is greater than that specified, particularly if the input

spectrum has little noise in it. If the sensitivity appears to be less than specified, it is probably because of noise, either on the power supply or in the input, because signal detectors with large dynamic ranges can be susceptible. A simple RC low-pass filter can be used to knock the interference down if necessary—and good high-frequency bypassing is recommended (a 0.01 µF as shown is usually OK.

As with any CMOS device, observe static handling precautions.
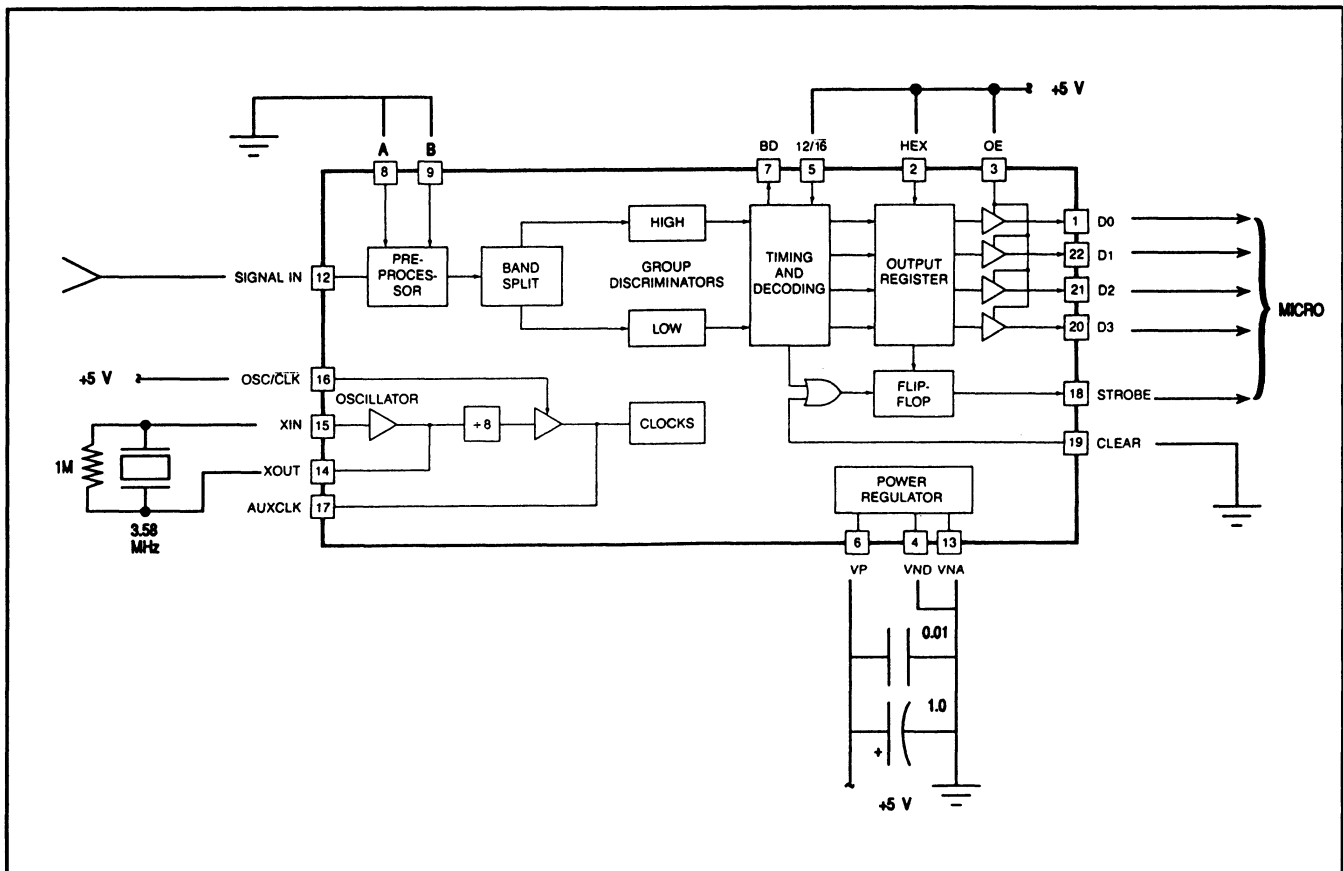
Figure 1 Simple Operating Circuit for +5V Supply

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ROTARY DIAL OR PULSE DIALING IN PHONE SYSTEMS

Over the years, a number of schemes have been used to make calls in telephone systems, from the operators and plugboards of early years to digital signaling. For the most part though, there are only two ways of placing calls in our phone system today—pulse (rotary) dial, and tone (DTMF) dial. Telephone sets in the U.S. today are about evenly divided as to which form is used, but tone dialing is replacing pulse gradually. Outside the U.S., pulse is found most often, with a few national telephone systems being converted to tone. In this application brief we will limit discussion to pulse.

Pulse dialing is a DC signaling standard developed to operate the old style automatic telephone switching equipment, which required pulses of current to operate relay-type selector gear. The pulses are created by breaking the current loop from the telephone switching center (central office or PBX) a number of times corresponding with the digit being dialed. An illustration of the loop from the CO or PBX is shown in Figure 1. Most pulse phones are of the rotary type with a round dial—the dial is rotated counterclockwise to the digit desired and released, causing a small cam to break the loop the right number of times. This type of dialing is also known as "loop disconnect" for obvious reasons, and can be implemented from keyboards or microprocessors as well, as we will show.

The pulses are specified from 8 to 12 pulses per second (PPS) with a duty cycle of 60 percent break. The interval between digit pulse trains is around 700 milliseconds minimum. There are a few systems that use 20 PPS signaling, principally on lines between switching systems. A little quick calculation shows that it can take almost two seconds to dial a "0" which is ten pulses—ten pulses take about a second plus the requisite

interval of 700 milliseconds. Compare that with the same digit dialed using DTMF tones, which use a 400 millisecond burst plus the interval of 40 milliseconds, for a total of less than 100 milliseconds. Of course, special tone receiving equipment must be used, but you can see why DTMF phones are becoming more common.

The CO or PBX also uses the DC current to "supervise" the telephone lines for their status, on-hook (idle) or off-hook (in use), distinguishing dial pulsing by timing windows. For instance, loss of loop current for 60 milliseconds is a digit "1" but loss for 300 milliseconds is recognized as "on-hook". This was done by special relay design and circuit engineering but is accomplished using fast digital techniques today. Figure 2 illustrates dial timing.

Pulse dialing is accommodated worldwide, and in many places is the only form available. New designs in telephone systems generally make provision for both types, mostly because there are millions of rotary dial phones in service including most of the inexpensive one-piece pushbutton phones which are actually pulse dialers.

Teltone offers a number of component products that are designed to simplify and reduce cost in circuit designs using dial pulsing. These are:

    M-927 DTMF and Rotary Dial Receiver
    M-959 Dial Pulse Counter and Hook Status Monitor IC
    M-969 Binary Input Pulse Dialer IC
    M-949 Line Sense Relay (Two Versions)

The best way to display the uses and advantages of devices like these is to provide some practical applications. The most obvious use of a dial pulse receiver is as a primary digit receiver in a switching system—a variation of this use is
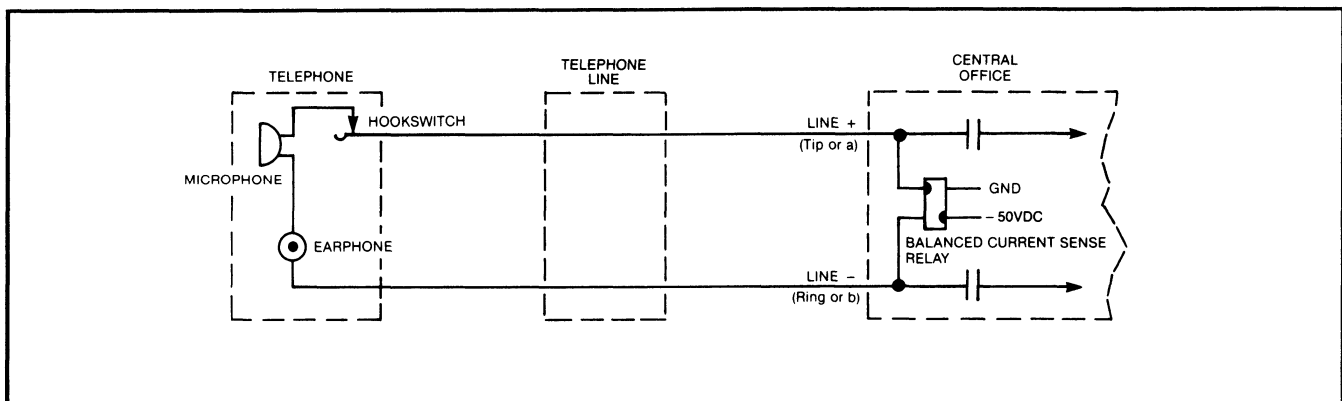

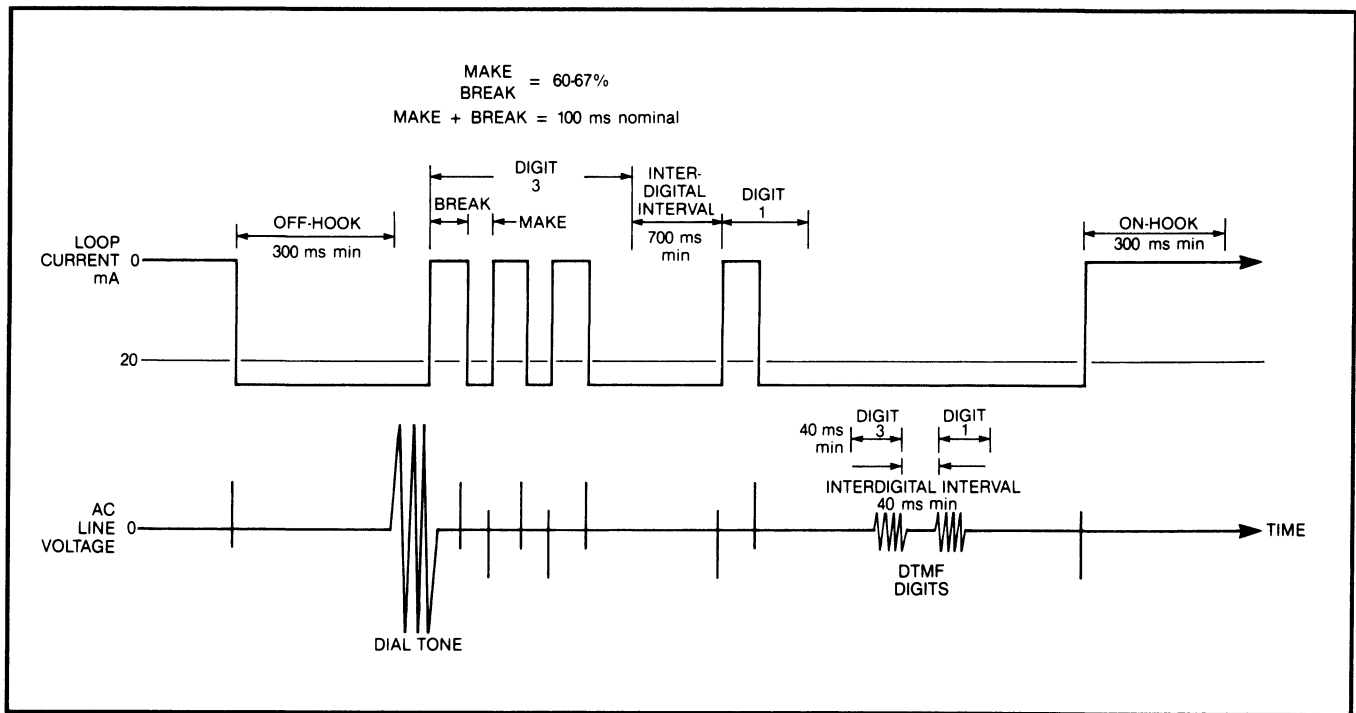**Figure 1   The Current Loop from Telephone Switching Equipment**

Figure 2   Tone and Pulse Dial Signal Comparison

shown in Figure 3. In this case, the M-927 is providing DTMF and pulse reception, and doing hook status monitoring for a key system intercom. One of the most notable things about this circuit is its simplicity. The M-949 picks up loop current for the M-927, which ties directly to the line for DTMF tones. Excluding the crystal, the part count is two for the signaling part of the product. This arrangement carries the bonus of being compatible with FCC Part 68 requirements including isolation, balance, and voltage withstand.

Figure 4 shows a solution to a common problem: using tone dialing with a pulse dial central office, as often happens as PBX systems are upgraded or when tone service is desired in older style systems. This tone-to-pulse conversion circuit recognizes that a line has been "seized" for use and intercepts tone digits, converting them to their equivalent detection to prevent tones from leaking through. Should dial pulses appear, the M-969 will restore the split line to permit straight-through dialing. The M-949 permits the control logic in the M-969 to make decisions about line condition, while the M-957 provides the time base and the digit detection. Line

splitting is done with a 2 Form C, and hold or dial pulsing is done using a 1 Form A relay or solid-state network.

There are a great number of uses for automatic dialing: alarm systems, modems, control systems, pollers, and trunk circuits are just a few. In such applications the binary input format of the M-969 is particularly useful because of the ease of interface to microprocessors and other binary devices. Figure 5 contains an example of such an interface, a "dumb" or processor-less polling dialer. In this use, the M-969 receives dial digits from a list in ROM, provided by the control logic. When signaled to start by the raising of the Data Terminal Ready (DTR) line, the circuit fetches the first number, dials it, waits for carrier, then connects. When carrier is dropped a disconnect is executed and the next number is dialed, and so on until the sequence is complete, at which time the process may be restarted if desired. Using the internal 16-digit buffer, an entire dialing string can be spilled from ROM to the M-969, eliminating the need for digit-by-digit control. Call progress indication is done by checking for dial tone before pulsing, then waiting for a modem carrier detect signal after pulsing.
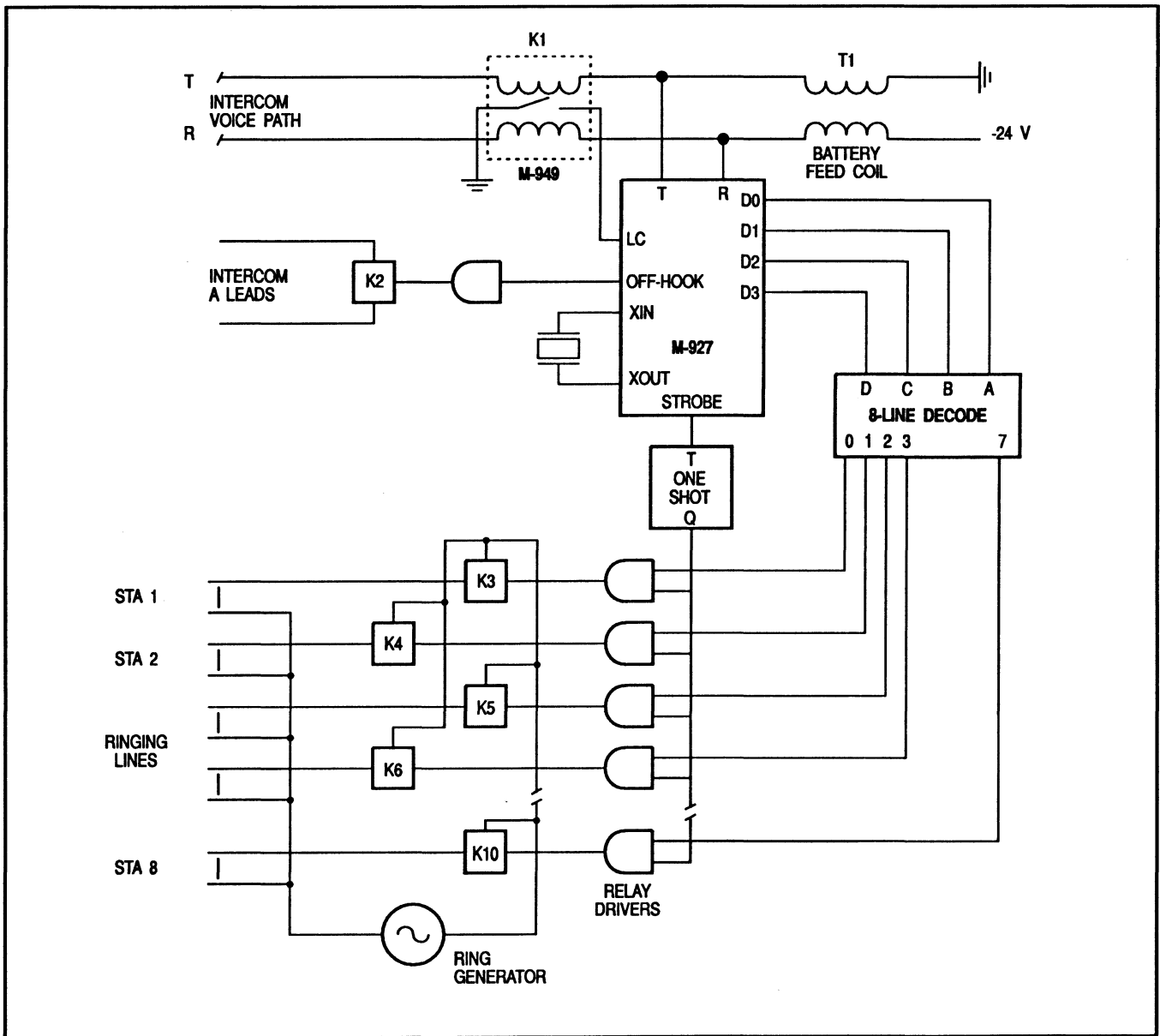
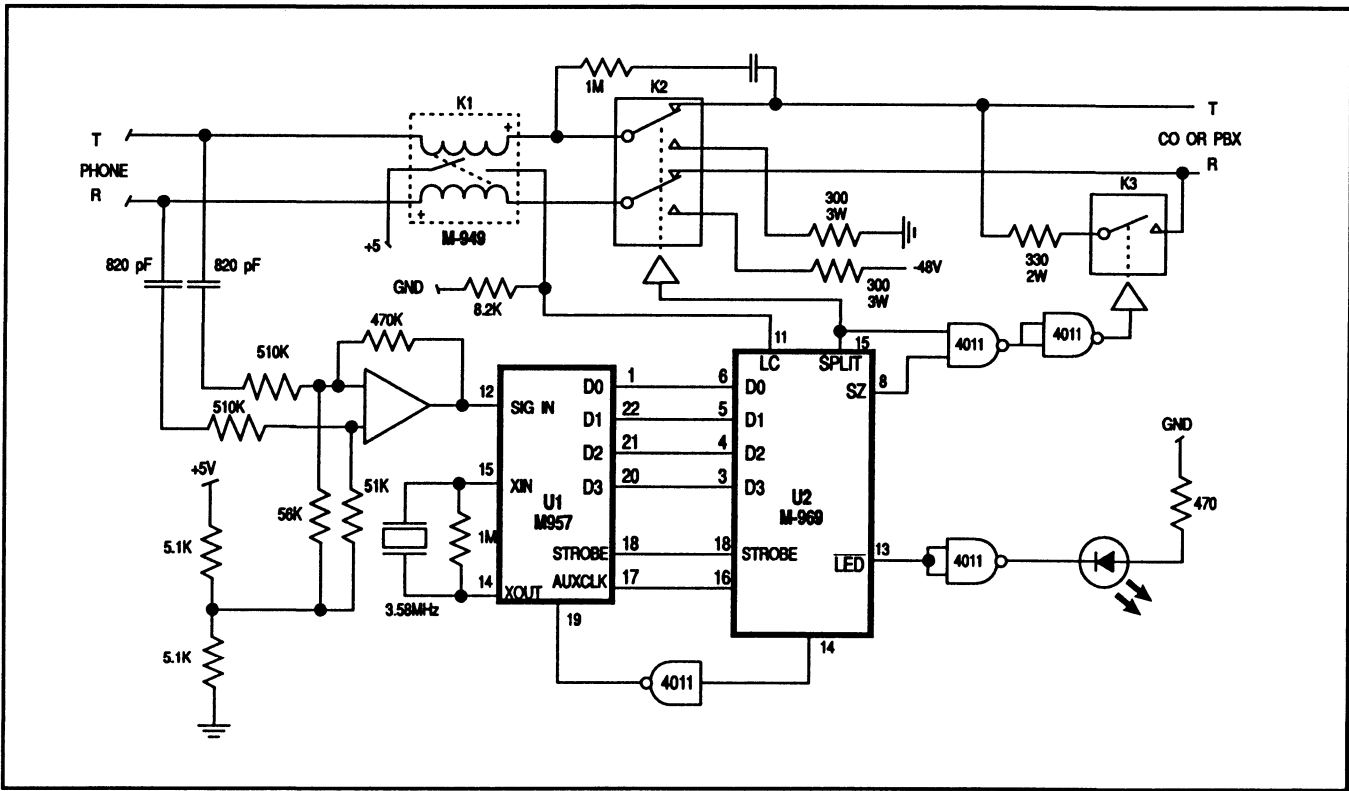Figure 3 Intercom Station Alerter for Electromechanical Key Systems

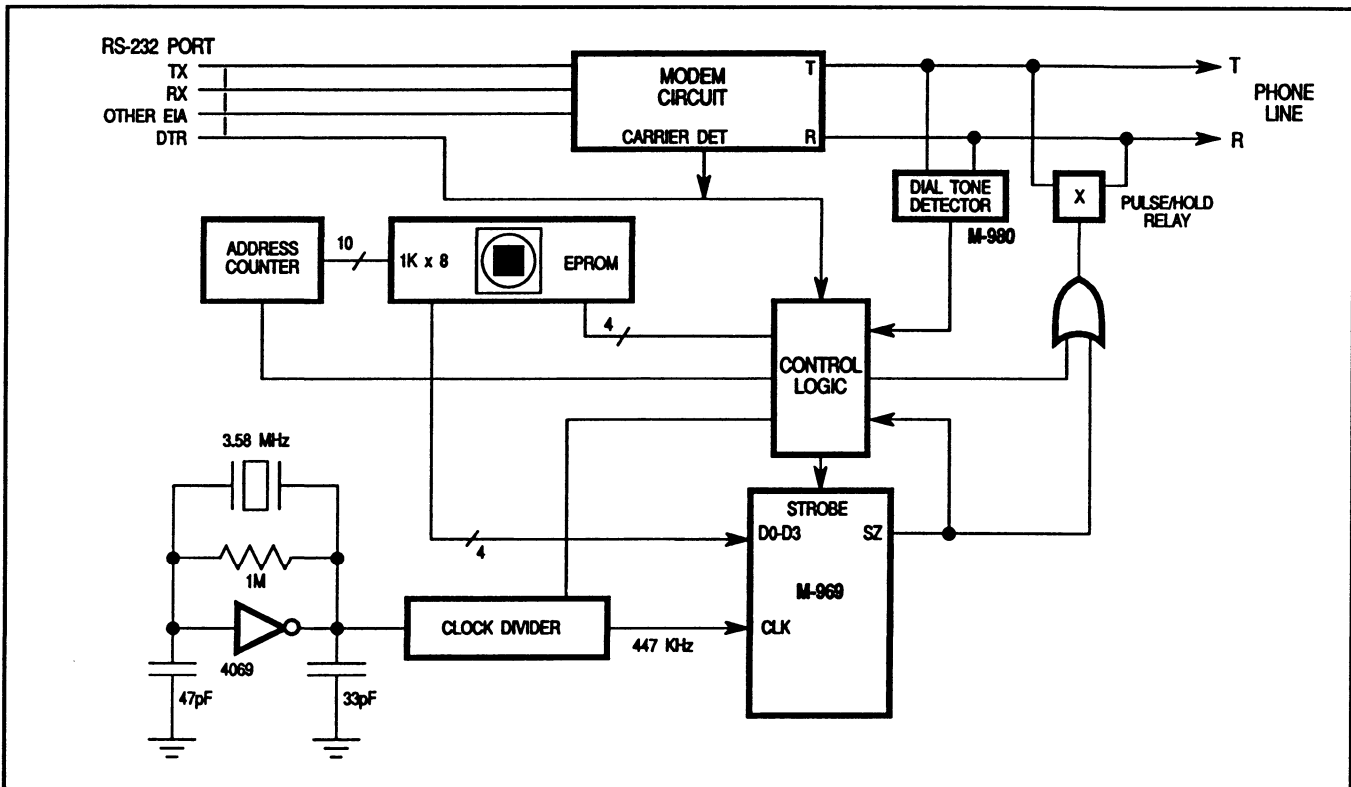**Figure 4 Tone to Pulse Conversion on a Phone Line**

Figure 5 Automatic Dialing Poller Without Microprocessor Control

CALL PROGRESS TONE STANDARDS

Telephone systems provide users with feedback about what they are doing in order to simplify operation and reduce calling errors. This information can be in the form of lights, displays, or ringing, but is most often some sort of audible tone heard on the phone line. These tones are generally referred to as call progress tones, as they indicate what is happening to dialed phone calls. Conditions like busy line, ringing called party, bad number, and others each have distinctive tone frequencies and cadences assigned them for which some standards have been established.

Standards for call progress tones are unfortunately applied differently in different situations or countries. The main groups of standards could be considered to be :

(1) the United States
(2) everyone else

Information on most schemes in use is available, and which tones will be encountered can be predicted fairly well by reviewing a few references.

Most tone standards vary with the country of application. In the U.S., the tones for Network are defined in AT&T's "Notes on the Network", and for PBX in the EIA's RS-464 documentation. Outside the U.S., national Post, Telegraph, and Telephone (PTT) organizations set requirements for such signals, but they generally follow similar lines as regards frequency and cadence—the best reference in that case being the CCITT recommendations that cover member countries (Yellow Book, Volume II—Fascicle II.2, Supplements). The example pages from the Yellow Book in Figure 1 show the completeness of the CCITT documentation. The CCITT document also shows the U.S. tone plan, but doesn't provide the detail found in the AT&T publication (see Figure 2).

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	FREQUENCY (Hz)				

RINGING TONE

CONTINUOUS					CCITT - 30000
		IRAQ	400	TANZANIA	400

2 - 4					CCITT - 30050
BAHAMAS	440/480//	JAMAICA	440 x 480	TURKS & CAICOS	440 + 480
	420/20//400	NIGERIA	400 // 450	UNITED STATES	420 x 40$^{23)}$//
CANADA	440 + 480	S. LUCIA	420 + 40		440 + 480
CAYMAN ISLANDS	425/50				

1.85 - 4.15					CCITT - 30060
		ROUMANIA	16 2/3// 450/25		

1.66 - 3.33			28)		CCITT - 30066
CAMEROON	425	IVORY COAST	50	MOROCCO	425
FRANCE	400		425 x 50	NEW CALEDONIA	425
FRENCH POLYNESIA	450	MADAGASCAR	25		

1.5 - 3					CCITT - 30070
		SPAIN	425		

1.5 - 3.5					
ALGERIA					

| 1.5 |
| 1.2 |
| 1.2 |
| 1.2 |

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Fascicle II.2 — Suppl. No. 4

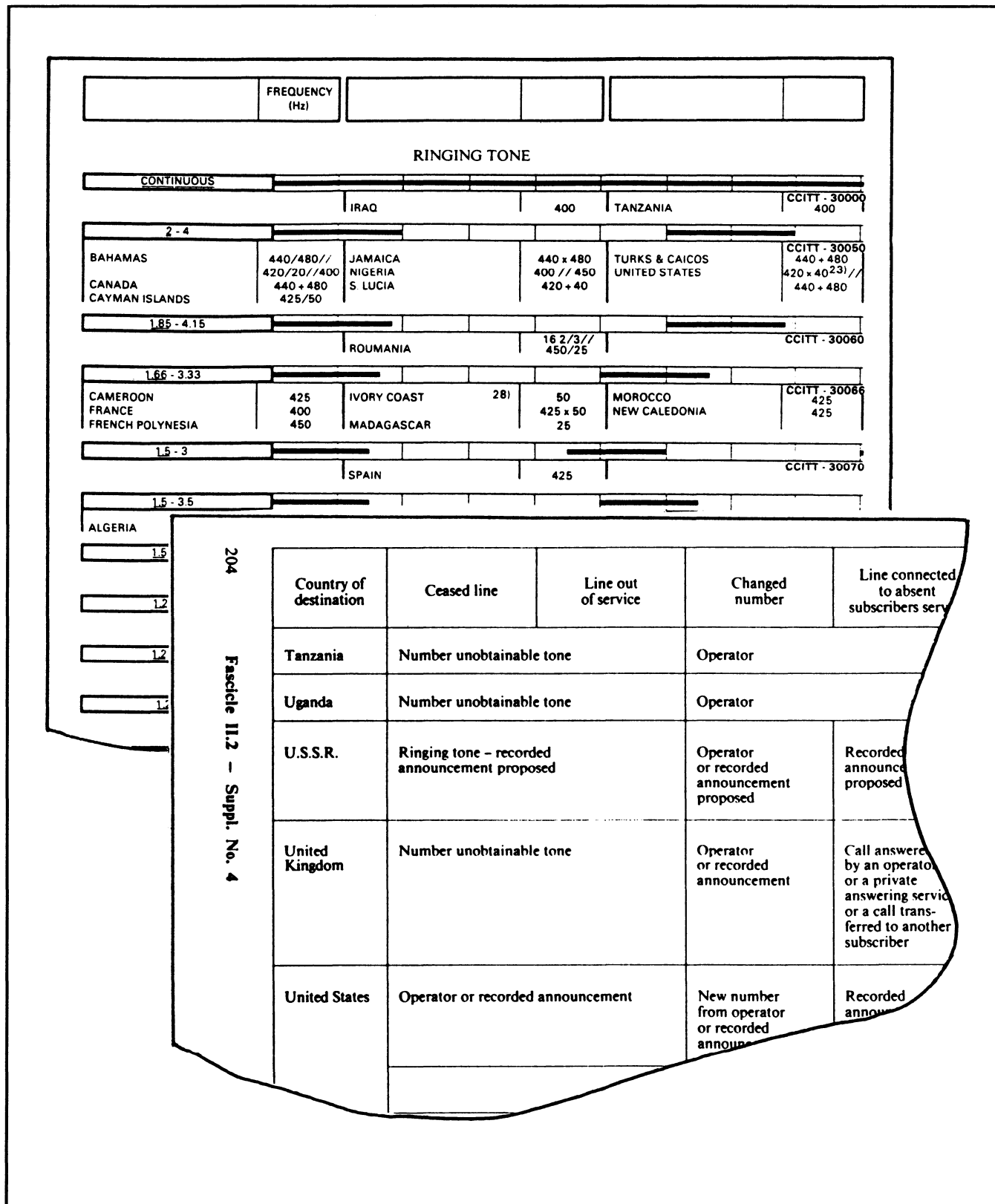| Country of destination	Ceased line	Line out of service	Changed number	Line connected to absent subscribers ser
Tanzania	Number unobtainable tone		Operator	
Uganda	Number unobtainable tone		Operator	
U.S.S.R.	Ringing tone – recorded announcement proposed		Operator or recorded announcement proposed	Recorded announce proposed
United Kingdom	Number unobtainable tone		Operator or recorded announcement	Call answere by an operato or a private answering servi or a call trans- ferred to another subscriber
United States	Operator or recorded announcement		New number from operator or recorded announ	Recorded anno

Figure 1 Examples from the Supplements of CCITT Fascicle II.2 (Yellow Book)

Tones	Frequencies[a] (HZ)				Power per frequency at exchange[b] where tone is applied[c]	Cadence
	350	440	480	620		
Dial tone	●	●			– 13 dBm0	Continuous tone
Dial tone-Modern PABX only	●	●			– 16 dBm0[d]	Continuous tone
Recall dial tone	●	●			– 13 dBm0	3 bursts of 0.1 s followed by a continuous tone[c]
Recall dial tone-Modern PABX only[a]	●	●			– 16 dBm0	3 bursts of 0.1 s followed by a continuous tone[c]
Busy tone			●	●	– 24 dBm0	Burst 0.5 s/silence 0.5 s
Busy tone-Modern PABX only			●	●	– 21 dBm0	Burst 0.5 s/silence 0.5 s
Reorder tone			●	●	– 24 dBm0	Burst 0.25 s/silence 0.25 s
Reorder tone-Modern PABX only			●	●	– 21 dBm0	Burst 0.25 s/silence 0.25 s
Audible ringing tone		●	●		– 19 dBm0	Burst 2 s/silence 4 s
Audible ringing tone-Modern PABX only		●	●		– 16 dBm0	Burst 1 s/silence 3 s
Call waiting tone		●			– 13 dBm0	Burst of 0.3 s every 10 s
Call waiting tone-Modern PABX only[a]		●			– 16 dBm0	A burst of 0.3 s / Station call waiting
					– 16 dBm0	2 bursts of 0.1 s[e] / Outside call waiting
					– 16 dBm0	3 bursts of 0.1 s[e] / Urgent call waiting
Busy verification		●			– 13 dBm0	A 2.0 s burst followed by 0.5 s bursts every 10 s
Busy verification – Modern PABX only[a]		●			– 14 dBm0	Burst of 1.5 to 2.0 s followed by...[f]
Executive override – Modern PABX only[a]		●			– 14 dBm0	Burst of 3.0 s
Confirmation tone	●	●			– 13 dBm0	Burst 0.1 s/silence 0.1 s/Burst 0.3 s
Confirmation tone-Modern PABX only[a]	●	●			– 16 dBm0	3 bursts 0.1 s[e]

a) Frequency limits are ± 0.5% of the nominal frequency.
b) PABX tone levels are measured at the PABX interfaces (typically at customer premises). Power levels are 2 dB lower for private line interfaces.
c) Power level tolerances are + 1.5 dB.
d) Tolerance level for PABX dial tone is + 0.75 dB.
e) Bursts are separated by 0.1 s.
f) Burst of 1.5 to 2.0 s before attendant intervenes, followed by repeated bursts of 0.5 to 0.8 s, 8 to 20 s apart.
g) Tones applied at PABX station or private line interfaces and not at the exchange interfaces.

Figure 2 U.S. Tone Plan as Listed in CCITT Fascicle 11.2

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USING A PBX TO IMPLEMENT A MANUFACTURING TRACKING SYSTEM

Manufacturing systems are carefully designed for efficient control of the production process. Whether used to produce complex aircraft or plastic piece parts, these systems have some common goals:

(1) Efficient collection of material as needed
(2) Monitoring flow times and work efficiency
(3) Ready availability of production line information (WIP, trouble spots, shortages, etc.)

Manufacturing systems also have some common problems; different department reporting channels, physical separation of production areas, personnel skill variations, budget limitations, and others. We often look to technology to help us with these things, but frequently encounter complex, expensive collections of hardware and software that aren't well suited to manufacturing. As usual though, with a little awareness of what you already have and some ingenuity you can solve your problem with a minimum of expense and a maximum of usability.

For example, consider the small manufacturer who is building an electronic product based on a printed circuit board. The bare boards are received at a contractor's site where they have a number of components automatically inserted. When they have been soldered and inspected, they are trucked across town to the main site where special or unusual components are added and the basic board tested. Bad boards are reworked and tested while good boards proceed through assembly stages that involve attachment of wire assemblies and enclosure in a housing. After passing final test the finished units are placed in stores and shipped from there as sales orders call for them.

This is a pretty common process and often involves production of several types of finished items. The needs are also common: did the contractor get his material, how much, is he ready to send over his latest batch, how many units made it through test today, what percentage were turnup problems, does stores have enough housings for the batch ready for final assembly, is there a quality hold on boards, does the floor supervisor know of any shortages? A good manufacturing
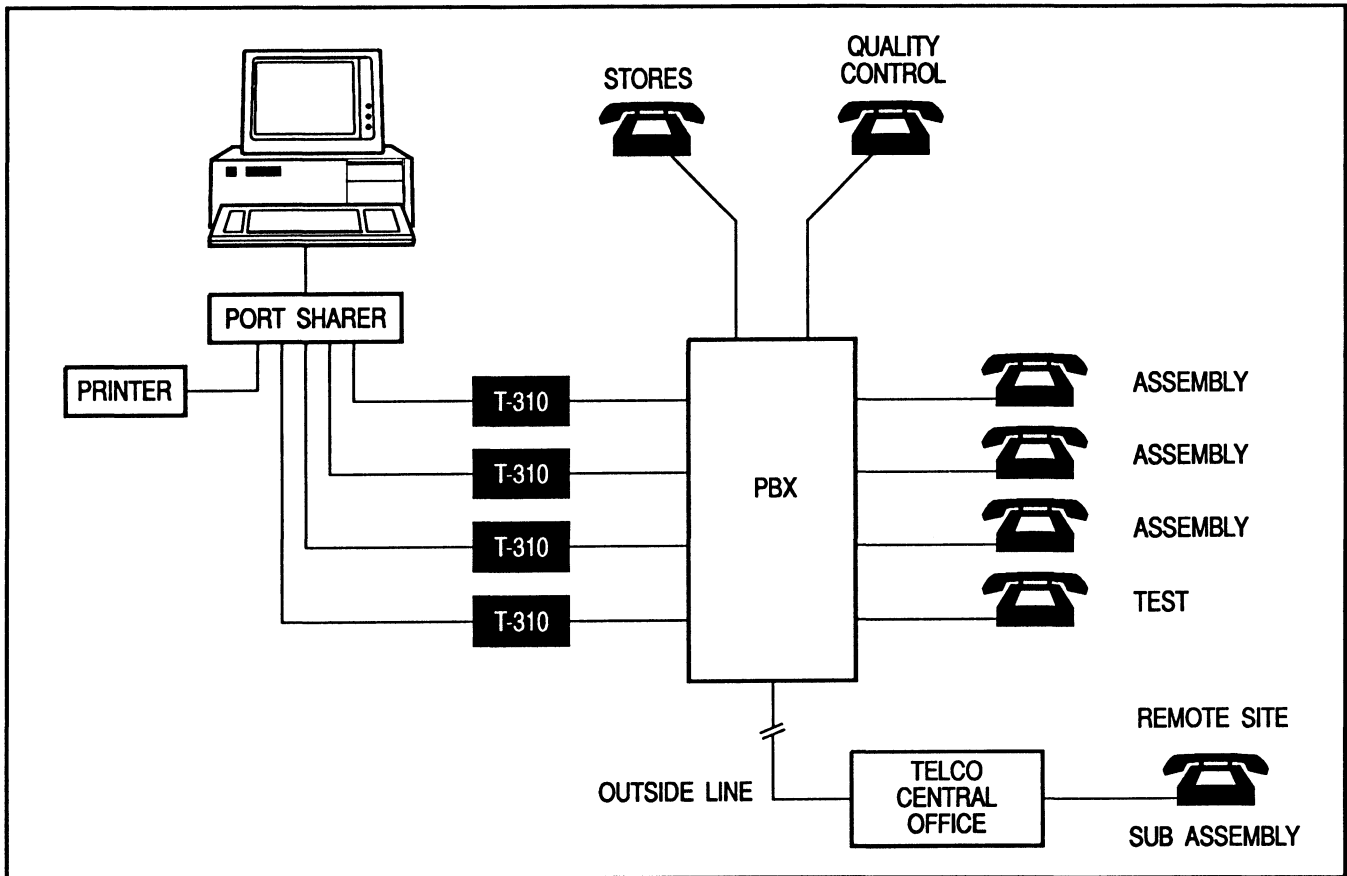

Figure 1   A Manufacturing Tracking System Using Regular Telephones for Collecting Information

manager has ready answers to questions like these, or isn't far from the answers. How can the manager do this without putting on another person to handle phone calls and play phone tag, or without putting in a costly control system? Most of the needed tools are on hand—in the form of a telephone system. The telephone system in any business allows any phone line to connect to another for information exchange. Usually this requires people at both ends, but there are some alternatives. Figure 1 illustrates the use of a microcomputer and some inexpensive peripheral devices to provide an information gathering and reporting system that doesn't need remote terminals any more sophisticated than DTMF (Touch-Tone®) telephones.

Buying the microcomputer and peripherals off-the-shelf, the manufacturing manager modifies a spreadsheet program to allow entry of data from Teltone's T-310s. The program listens to several T-310s connected to PBX extensisons, gathering short messages sent from the Touch-Tone phones in other parts of the building and at the contractor's site. Status of the operation is recorded on the printer as desired and is accessible through the screen of the microcomputer. The use of several T-310 devices keeps incoming messages from

being delayed (causing frustration and consuming time) by busy signals.

As part of the normal flow, the handler of material and units dials an extension, enters a short ID code, status digit, and a quantity for each operation—the format can be adjusted to any kind of action. The program in the microcomputer assimilates the information and sorts it into meaningful form for printing or for the master status display screen. Data accumulated over weeks and days can give visibility to productivity, quality problems, production rates, and running inventory.

By adapting existing software and using all standard hardware, a manufacturing control system can be created inexpensively. It has the added advantage of simplicity, and it can be expanded to include voice prompting, additional ports, and reporting of other types of information from inside and outside the main plant. Wherever voice capability and Touch-Tone telephones exist, useful information-gathering systems can be created.

AN APPLICATION FOR THE M-991 CALL PROGRESS TONE GENERATOR

The M-991 is a 14-pin DIP IC that is capable of generating precise, low-distortion tones for use in dial telephone systems as status indicators. The tones described in the North American Precise Tone Plan and in various other international standards can be selected easily using latching binary inputs.

The M-991 can drive AC loads as low as 580 ohms (within 600 ohms ±10%) directly at high levels compatible with the strongest tone generally specified (dial tone). Other levels can be selected by simple external circuits. Distortion is a minimum of 35 dB down. An example application is shown in Figure 1.
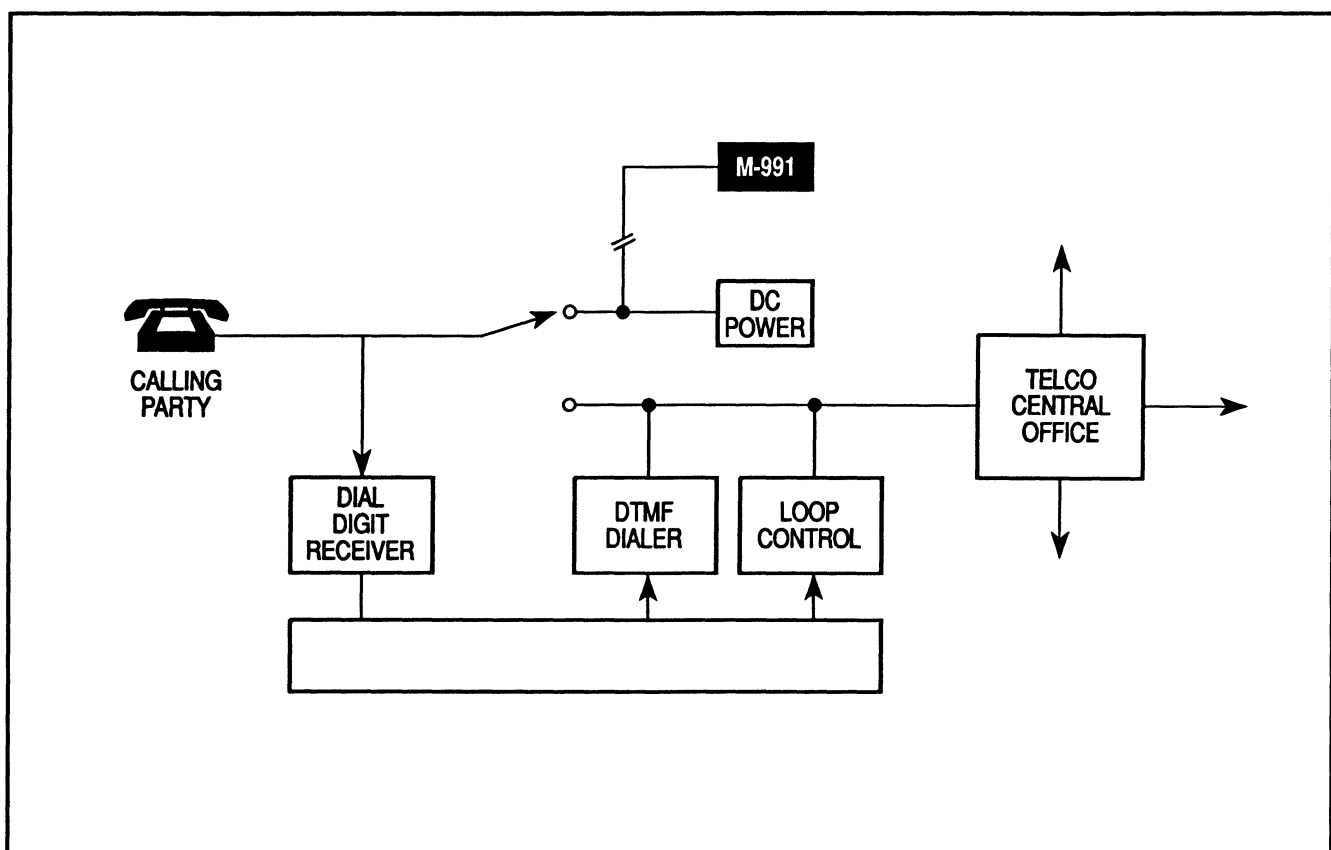

Figure 1 Generating Dial and Error Tones in a Dial Digit Translator or Automatic Dialer

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9-48

INTERCHANGEABILITY OF THE TELTONE M-956 AND M-957

Teltone provides a broad family of devices for tone detection and generation, for a variety of applications and requirements. Among these are the M-956 and M-957 DTMF receivers, similar products generally used in different applications. These two ICs have an area of overlap in function that can allow them to be used interchangeably: when a 5-volt power source is used, and when there is no need for high-performance dial tone rejection. The alternative use of the two devices can provide a number of advantages including flexible use of part stock for different products.

Both the M-956 and M-957 use a 22-pin DIP package, in ceramic or plastic. The only pin assignment differences are at pins 8 and 9, where the A and B control lines for M-957 sensitivity adjust are found. The M-957 has the same sensitivity as the M-956 when A and B are at logical "0", or most commonly, grounded. If accommodation is made for this on the circuit board, either device may be inserted. See Figure 1 for an illustration.

The dynamic difference between the two devices is in the fact that the M-957 has additional dial tone filtering (rejection of signals below 480 Hz). This will have no significant effect on DTMF signal detect performance.
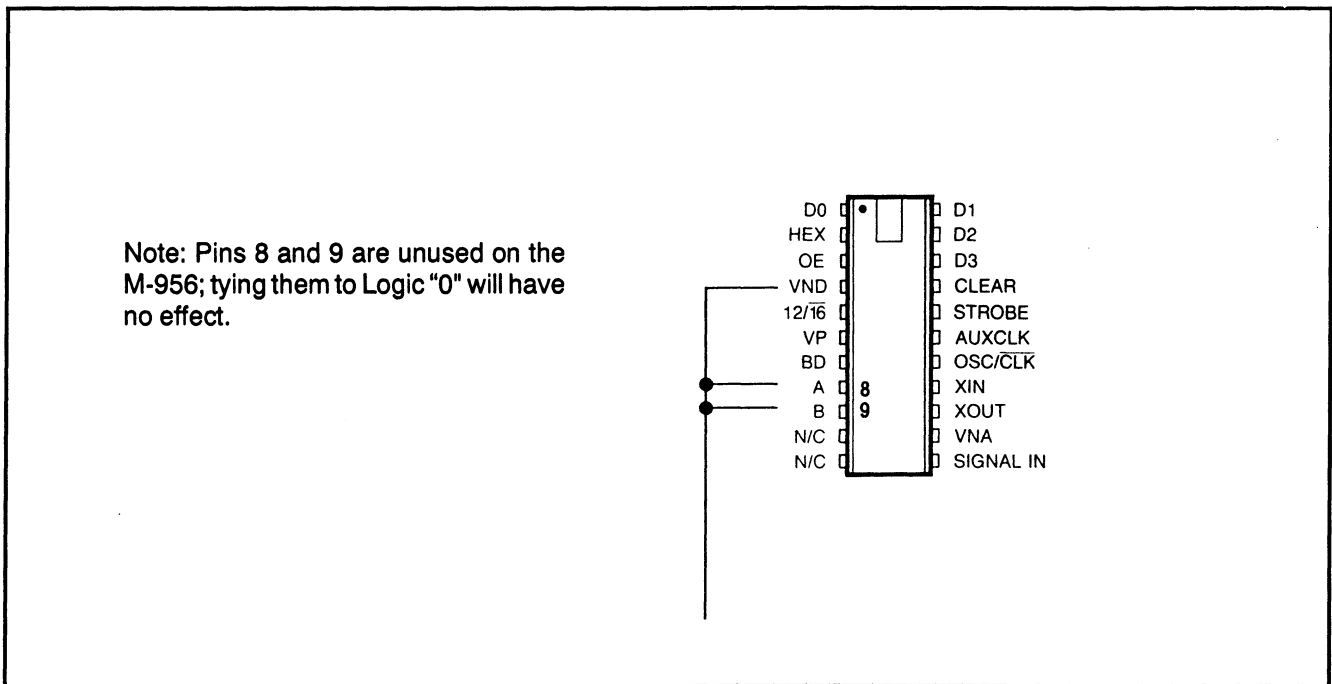
Note: Pins 8 and 9 are unused on the M-956; tying them to Logic "0" will have no effect.

Figure 1 Pin Assignment for M-957

APPLICATIONS FOR TELTONE COMPONENTS IN PRIVATE PAY STATIONS

The following describes some suggested applications of Teltone components in private pay station systems. It is intended only as a guide for designers of pay station systems and other telecommunications products, and Teltone assumes no responsibility for the use of its products on the basis of the information supplied here.

How Well Does Your Pay Phone Do the Following?

- Detect precise or non-precise call progress tones?*
- Detect and prevent fraud?
- Detect special information tones (S.I.T.) or O.C.C. connect?
- Detect voice—calling or called party?
- Generate call progress tones or rotary dialing?
- Monitor loop current?

*All central offices provide information tones to the calling party. These tones are referred to as "call progress" or "call following" tones. The terms are generally interchangeable.

Teltone Solutions

Detecting Precise Call Progress Tones: The call progress tones (dial tone, busy tone, ringback tone, reorder tone and others) provided by central offices are not completely standardized. The "precise tone" standards in some publications are CCITT** recommendations for signal frequency and cadence. These standards are implemented and maintained only in modern or upgraded central offices. The **Teltone M-981 or M-982 Precise Call Progress Tone Detectors** are excellent receivers for these signals.

CCITT is the International Telegraph and Telephone Consultative Committee, a specialized agency of the United Nations which recommends telecommunications standards for use worldwide.

Detecting "Non-Precise" Call Progress Tones: Call progress tones which do not conform to the CCITT-recommended standards are called "non-precise". In systems to be served by central offices that supply non-precise tones, a broadband low-frequency energy detector like the **Teltone M-980 Call Progress Tone Detector** is required. Fortunately, the cadence for call progress is relatively consistent throughout the industry, and with the M-980 non-precise tone detection is easily achieved.

Detecting and Preventing Fraud: Different central offices provide different network characteristics. As a result, fraud

attempts that work in one area will often not work in another. In some areas, if a pay station user calls a local number and establishes a legitimate completed call, then instructs the "called" party to hang up and waits for a second dial tone, the central office will provide a new dial tone and hence a free call.

Using a Teltone M-981 or M-982 to detect a second dial tone will prevent this if the second dial tone is precise.

If the dial tone is not precise, a non-precise tone receiver like the M-980 would have to be used. However, if the background noise is sufficient to cause the receiver to detect a continuous signal, e.g., audio alarm, jet noise at airports, honking horns, music, etc., the M-980 will interpret it as dial tone. You would then run the risk of cutting off more legitimate calls than preventing fraud calls. Muting the tone pad after the original call is established will prevent some illegal calls, unless the calling party has an acoustical DTMF coupler (available from most data product suppliers).

Probably the best way to prevent multiple fraud calls is to monitor for DTMF signals occurring after one call has been completed (i.e., after answer by the called party). However, some people orally produce DTMF tones when talking; this phenomenon is called "talk-off", "talk-down", or "hits". Since false digits due to talk-off are usually the same number, fraudulent attempts to dial more digits can be distinguished from talk-off by monitoring for a series of alternating DTMF numbers (at least three different numbers in a string of hits within a specific time window) before restricting the call. About the only exception is that if a 0 is detected, restrict the call! Fortunately, 0 is rarely "talked off". The **Teltone M-957 DTMF Receiver** offers excellent dial tone and speech immunity.

Detecting Special Information Tones (S.I.T.): Many pay station calls are answered by an intercept recording, which requires a coin return. Most intercept recordings are preceded by special information tones (S.I.T.) and pay stations must be able to detect these tones to minimize false collections. The **Teltone M-984 Special Tone and Call Progress Tone Detector IC** can provide this capability.

Detecting O.C.C. Connect Tone: If your pay station is intended to access other common carriers (O.C.C.) such as MCI and Sprint, you need to be able to detect the 400-Hz O.C.C. connect tone. The **Teltone M-981 and M-984** are ideal components for this.

Detecting Voice: Your pay station must be equipped with a voice detector. **Either the Teltone M-980 or the M-984** (using the det pin) can be used to provide input to a voice

detect module. Ideally you should provide two voice detect modules, one to monitor the central office line side of the pay station and one to monitor the handset microphone, to enable your processor to identify the calling party and called party separately. The sensitivity of the handset microphone voice detector should be adjusted so that background noise is generally not detected. You should also null the audio on the line voice detector from the audio signal induced by the microphone.

Generating Call Progress Tones: Some pay stations store and forward the originating dialed number to minimize direct user access to the telephone line. Where this is done, the pay station must provide call progress tones (dial tone, busy, reorder, ringback, error, and possibly others) to the calling party. This provides the pay station with first analysis capability for rate determination, restriction, number translation, automatic O.C.C. access, or whatever is desired. The Teltone M-991 Call Progress Tone Generator can produce all the tones needed for call progress or call following.

Generating Rotary Dialing: Most central offices will accept rotary dial signaling, but not all are equipped to receive DTMF tones. If your pay station uses a DTMF tone pad for signaling, you might need the Teltone M-969 Rotary Generator.

Monitoring Loop Current: Almost all telephone lines will accept rotary dialing, and since rotary dialing consists of makes and breaks of loop current, it is possible for a caller to toggle the switchhook and generate acceptable numbers. This can be prevented either by not allowing loop current to be controlled directly by the switchhook or by monitoring loop current for any switchhook breaks. The Teltone M-949 Line Sense Relay is an ideal device for loop current monitoring.

Collect or Return? Some Common Problems

1. A call to a business is answered on the first ring and transferred to an extension which does not answer, and after a few rings from the extension the calling party hangs up. How can answer be verified so that a coin can be collected for this call?

If only one ringback tone burst is detected, an M-980 would not provide enough information to determine that an answer has occurred. If your pay station uses the M-981 or M-982 and ringback is precise, the first ringback will be detected, so if a second ringback is not detected within 5 or 6 seconds, answer could be assumed. If any call following tones are detected after 6 seconds from the last ringback detection, answer is verified. Collect.

2. The calling party dials a valid number, no call progress tones occur, no S.I.T. tones occur, and the call is answered and immediately put on hold. How can coin collect/return be handled?

Pay stations require some internal timing to prevent false coin collections or coin returns. When busy, reorder, error, or S.I.T. are detected (via the M-980, M-981, or M-982 and M-984), the pay station should return the coin after hangup. But when no terminating signals are detected, coin collect or return must be based on timeout-programming.

3. The calling party dials a valid number, no call progress tones or S.I.T. tones occur, and the call is connected to an intercept recording. How is this distinguished from an answered call so that coin return can be provided?

Because voice is detected primarily on the line side, sufficient time should be provided for the calling party to hang up and activate the coin return circuit.

4. The calling party dials local time and hangs up after a 10-second message. Can this type of completed call be collected?

Your software should have a free call table which will allow certain "free" numbers to be dialed. You can just as easily have a table to expedite collection when other numbers, like 555-TIME or O.C.C. access numbers, are dialed.

5. A number is dialed, no call following signals are detected, and no voice is detected on the line side. How long do you wait before collecting?

Your choice: there is no regulation or established standard for this. You could collect after 60 seconds from the last digit dialed. Or you could restrict and return the coin.

Timing Guidelines

"When to collect" is probably the biggest variable in pay station design. There are no universal "best" answers to problems posed by the above questions, but the following are suggested:

- After a number has been dialed, your pay station should enter into a call following mode and establish a collect timing interval. Different timing intervals need to be established any time new call progress tones are detected.
- Once a call is originated, if no call progress tones are detected your pay station must collect after a period of time (1.5 to 2 minutes?).
- If ringback is detected, collect timing should be stopped and the station should monitor for additional ringbacks or other signals. If ringback stops (ringback lost), you assume an answer occurred and establish a new collect timing interval (45 seconds to collect?).
- Continue to monitor. If ringback resumes, collect; it's probable that a business answered and forwarded the call to an extension (Question 1 above).

- Back to "ringback lost": you have assumed answer and are now monitoring for voice. Voice is detected on the line side, which starts a new collect timing counter. Because the voice could be a called party or an intercept recording without S.I.T., this time-to-collect interval needs to be very carefully considered (Question 3). It should be long enough to allow the calling party to hang up and get a coin return (if it is an intercept call), yet short enough to ensure collection of chargeable calls (20 to 30 seconds?).

- During that 20-30 second interval, if voice is detected on the handset microphone, assume conversation is occurring and establish a new collect timing interval. This interval can just as well be on the short side (5 seconds?) to cover the now less likely possibility of its being an intercept call: 5 seconds will give the calling party time to tell a recording where to go while hanging up!

- Call incomplete signals (reorder, busy, S.I.T.) should activate coin return on hangup. If these signals are detected, but if the caller remains off-hook, you have two choices:

Collect if off-hook exists for more than (90 seconds?), or

- Have the pay station terminate the connection after (60 seconds?) and return the coin.
- Hangup prior to verification of call completion should activate coin return.
 If your software does not recognize the "time" number, time calls will usually be coin return calls unless the recording is a long one. (Question 4.)
- **REMEMBER:** The best pay stations identify call progress tones in the shortest time. The use of precise and non-precise tone receivers is essential. Pay stations with dialed number analysis will also have an advantage in being able to provide services like least cost routing (O.C.C.), number translation, and rate analysis.

Useful Information

The Bell Communications Research (Bellcore) Information Operations Center catalog of technical information is a must for designers of telecommunication equipment. Its1986 issue of "Notes on the Network," TR NPL-000275, is available at $150. The address is:

Bellcore
60 New England Avenue
Piscataway, NJ 08854
1-800-521-2673

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A TWO-IC ALTERNATIVE TO THE M-958 PCM DTMF RECEIVER

The Teltone® M-958 PCM DTMF Receiver is a microcircuit designed to provide DTMF detection functions for digital switching systems. A hybrid circuit, the M-958 uses two integrated circuits and a number of passive electronic components to do the digital highway interface and tone processing functions.

Unfortunately, before the M-958 entered production use, one of the ICs was discontinued by its manufacturer (not Teltone). This made it impossible to produce the PCM DTMF Receiver design, and it was deleted from Teltone's product offering.

The function of the M-958 can be easily reproduced using other devices, however, as can be seen in Figure 1. In this case a commonly used PCM coder/decoder (codec) provides the digital highway interface for the M-957 DTMF Receiver. The components required beyond the ICs are limited to a few resistors and capacitors, whose role is mostly to set gain and limit high frequencies in the analog output of the codec. The exact performance of the Gould Semiconductor S3506 codec can be found in the literature of that manufacturer, and Teltone's M-957 is documented in the 957-100 data sheet.
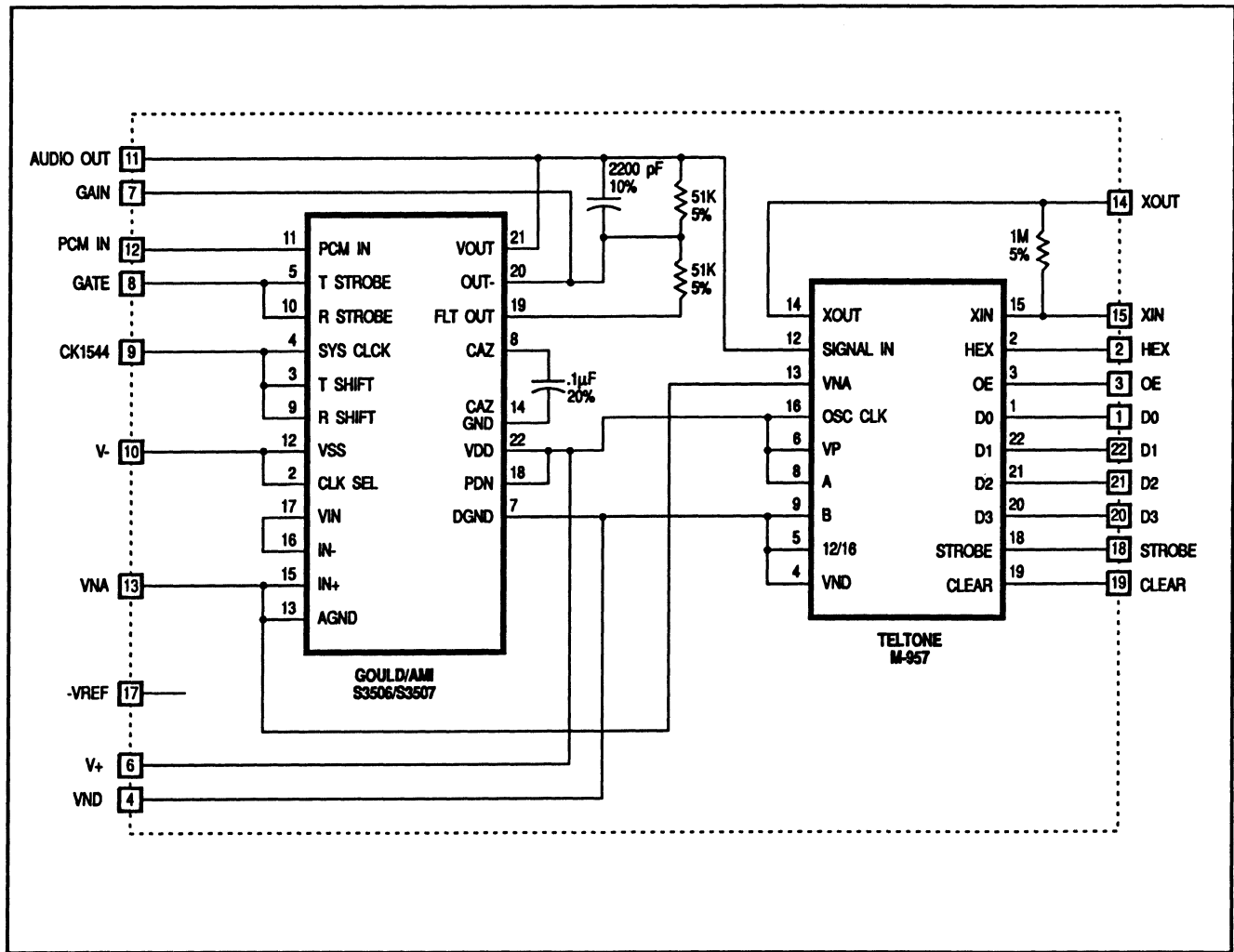

Figure 1 M-958 Equivalent Circuit

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USE OF THE TELTONE TLS-3 IN FAX DEALERSHIP/PHONE STORE APPLICATIONS

The Teltone TLS-3 Telephone Line Simulator is proving to be a very useful tool for FAX and/or telephone sales. Advantages include:

- Ability to provide "live" demos for store customers
- No telephone line charges to provide these demos
- Easy transportability of the TLS-3 to trade shows, customer sites, etc., for demos (no need to pay labor/line charges at shows; no need to rely on customers to provide live lines for demos).

One more desirable feature for a telephone line simulator has finally been addressed. Teltone had received many requests for a multi-line simulator, so that recabling when demonstrating more than one device could be avoided. (The TLS-3 provides one line for an outgoing call and one line for receiving the call.) The addition of a rotary switch box (made by Black Box Corp.) provides a simple, inexpensive solution. Figure 1 shows the Teltone TLS-3 configured with a Black Box switch.

There are several versions of the Black Box device available:

- 6-to-1 concentration Model GR-SW076A $109.00
- 4-to-1 concentration Model GR SW066A $ 99.00
- 2-to-1 concentration Model GR-SW065A $ 79.00

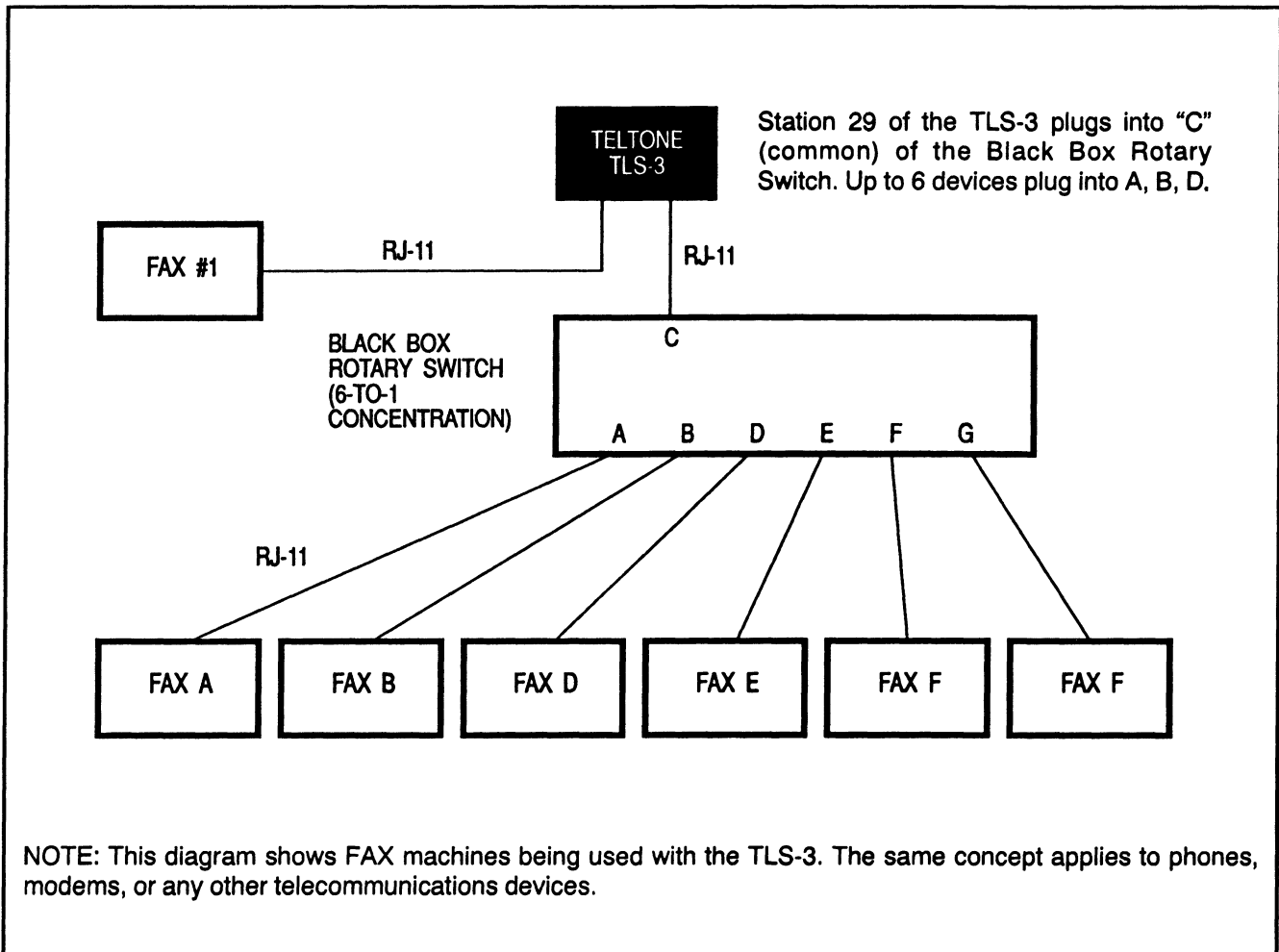Prices are from the September 1990 Black Box Catalog, Black Box Corporation, (412) 746-5530.

Figure 1 TLS-3 Configured as a Multi-Line Simulator Using Black Box Switch

BAUD RATE ADJUSTMENT FOR THE T-310

The standard Teltone T-310 Telephone Access Unit, which runs at 300 baud, can be made to run at other fixed speeds. This is accomplished by changing a single location in the EPROM that holds the program for the internal 8031 chip.

To remove the EPROM:

- Detach the covers from the unit

- Separate the two circuit boards

- Carefully lever the 2732 IC from its socket

- Reinstall the EPROM by reversing the process.

The location contains a value as shown below for each baud rate:

Memory location	Contents
0826	75
0827	8D
0828	NN (where NN is one of the location values listed below)
0829	75
082A	98

Baud rate	Location value
300	A0 (default value)
600	D0
1200	E8
2400	F4
4800	FA
9600	FD

TELTONE®